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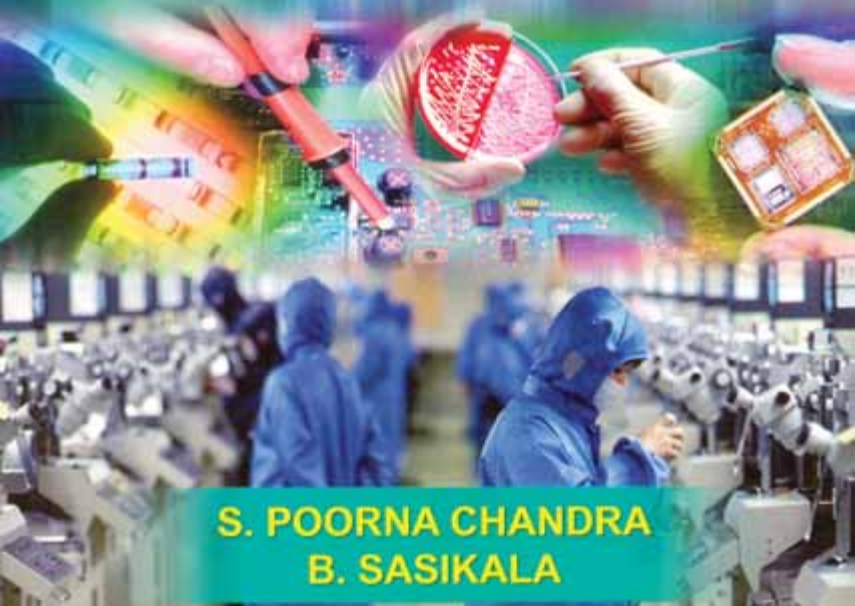

S. POORNA CHANDRA
B. SASIKALA

S. CHAND

VISIT…

ELECTRONICS LABORATORY PRIMER

ELECTRONICS LABORATORY PRIMER

(For B.E./B.Tech. Students of Electronics & Communication, Instrumentation & Control, Computer, Information Technology, Chemical, Mechanical and Marine Engineering)

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First Edition 1998
Seusequent Editions 2005, 2007, 2008, 2010, 2012
Reprint 2014

ISBN : 81-219-2459-6 **Code :** 10B 290

PRINTED IN INDIA

By Rajendra Ravindra Printers Pvt. Ltd., 7361, Ram Nagar, New Delhi -110 055
and published by S. Chand & Company Ltd., 7361, Ram Nagar, New Delhi -110 055.

PREFACE TO THE SECOND EDITION

This book is designed to meet the needs of students following curricula at various universities. It is intended not only for engineering students, but can also be used by polytechnic and science students.

The book has been broadly divided into Six major areas. It is well equipped to meet the basic concepts for network and devices lab, basic devices lab, solid-state electronics (with design), integrated circuits lab, digital electronics (with design) lab, and Basic Communication Circuits Lab. Though this book is designed for **electronics and communication students**, it also caters to other students such as those belonging to **computer engineering, instrumentation and control engineering, information technology, chemical engineering, mechanical engineering and marine engineering.**

Throughout this book, the emphasis is on basic concepts for understanding and background theory for the relevant practical.

The first chapter deals with the basic concepts such as passive components and their configurations, implementation of various theorems with theoretical justifications, practical implementation of passive filters with mathematical support and experiments on attenuators.

The second chapter concentrates on the characteristic performance of various electronic circuits and also deals with various parameters to be calculated for these devices.

The third chapter is on small signal amplifiers, large signal amplifiers, feedback amplifiers and oscillators. Emphasis is on the design concepts and the general practical problems encountered. Design concepts are complemented with relevant theory and mathematics.

The fourth chapter deals mainly with the integrated circuits and their practical applications. In this chapter, characteristics and electrical parameters of operational amplifiers are thoroughly analyzed. Experiments are designed in linear and non-linear application areas. Experiments are also provided based on 555 timer. The fifth chapter deals with Digital Electronics and last sixth chapter deals with Basic Communication Circuits.

On completion of every chapter, students will be comfortable with basic theory and its practical implementation along with applications. Exercises are given at the end of each concept. Objective questions are also listed at the end of each chapter.

This book can be used as a ready reference for hardware projects. It deals only with relevant mathematics to avoid complexity. This would enable the students to understand the basic electronics concepts even without thorough knowledge of mathematics or a theoretical knowledge of electronics.

S. Poorna Chandra
B. Sasikala

ACKNOWLEDGEMENT

Any mission never concludes without cordial cooperation from the surroundings. It is our great pleasure to thank the following people for their support.

We are grateful to Dr. S. Sathik (Ex-Vice Chancellor, Madras University), Director, Crescent Engineering College, Prof. S. Peer Mohamed, correspondent and Dr. S. Armugan, Dean, Crescent Engineering College; Prof Muthukaruppan, Principal, Sri Venkateswara College of Engineering, Dr. M.J.S. Rangachar, (Ex-HOD/ECE Regional Engineering College, Trichy), HOD/ECE, SriVenkateswara College of Engineering and Prof R. Ramachandran, HOD/IT, Sri Venkateswara College of Engineering, for their support.

For technical assistance, we would like to thank Mr. S. Ganesh Vaidhyanathan, Senior Lecturer/ECE, SVCE, for his valuable contribution in the field of digital electronics; Mr. S.R. Balasubramanian, Lecturer/ECE, SVCE, for his valuable suggestions in the section on amplifiers, and Mrs. Chaya Kulkarni, Assistant Professor/EEE, SVCE, for her many suggestions in the section on networks.

Our special thanks to Mr. G.S. Mohan Ram, Lecturer/IT, SVCE, who has rendered the fullest help in the book documentation with valuable tips at every juncture. We would like to thank Mr. P. Jayakumar, Lecturer/ECE, and Mr. Shanmugan, Programmer/ECE of SVCE, who have extended their help during documentation.

Last, but not the least, our sincere thanks to our beloved parents for their blessings.

We thank our publisher, S. Chand & Company Ltd. and those who were involved, directly, or indirectly in bringing out this book with a great success.

Authors

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1 NETWORK THEOREMS

1.1 UNITS AND ITS RELATIONS

Admittance (Mho, $\mho$) = 1/Impedence (Ω)

Boltzman Constant (k) = 1.381×10^{-23} J/^{0}K

Capacitance (Farad, f) = Charge/Potential

Charge (Coulomb, C) = Current $\times$ Time

Charge Density (ρ) = Charge/Volume (C/m^3)

Conductance (G) = 1/Resistance (1/Ohm, Ω)

Current (Ampere, A) = Charge/Time

Current Density (J) = Current/Area (A/m^2)

Displacement = Charge $\times$ Length (C/m)

Electronic Charge = 1.602×10^{-19} C

Electronic Mass = 9.109×10^{-31} kg

Energy Density = Energy/Volume (J/m^3)

Permeability of Free Space (μ_0) = 1.257×10^{-6} (H/m)

Permittivity of Free Space (ε_0) = 8.854×10^{-12} (F/m)

Plank's Constant (h) = 6.626×10^{-31} Js

Velocity of Light (c) = $3 \times 10^{+8}$ m/s

Unit System

The international system of units (SI) is based on fundamental units.

Table 1.1

Quantity	Unit	Abbreviation
Length	Meter	m
Mass	Kilogram	kg
Time	Second	sec
Luminous Intensity	Candela	Cd

(*Contd*)

Quantity	Unit	Abbreviation
Temperature	Degree Kelvin	^{0}K
Charge	Coulomb	C
Current	Ampere	A
Energy	Joule	J
Force	Newton	N
Potential	Volt	V
Power	Watt	W
Frequency	Hertz	Hz
Capacitance	Farad	F
Inductance	Henry	H
Resistance	Ohm	Ω

Multiples

Prefix	Abbreviation	Multiplier
Tera	T	10^{12}
Giga	G	10^{9}
Mega	M	10^{6}
Kilo	K	10^{3}
Centi	C	10^{-2}
Milli	m	10^{-3}
Micro	μ	10^{-6}
Nano	n	10^{-9}
Pico	p	10^{-12}

Basic Definitions

Average Value **:** The average value of a waveform, which swings symmetrically across the zero reference, will be zero for a complete full-cycle.

RMS Value **:** The rms value of an alternating voltage or current is the value, which would produce the same heat in a resistance as a direct voltage or current of the same magnitude.

Peak Value (V_m) **:** The amplitude of a waveform is a measure of the extent of its voltage or current excursion from the zero reference.

Peak-to-peak value = 2 × peak value.

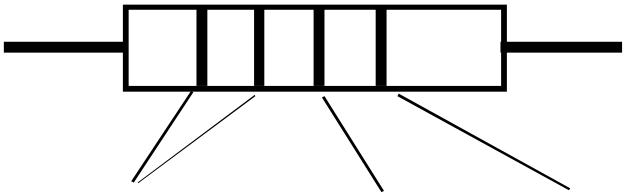
1.2 RESISTOR COLOUR CODE

Colour code is a means of identifying the value of the given resistor. There are two methods of colour-coding in use:

1. Four coloured band
2. Five coloured band

Four Coloured Band Coding

Table 1.2



Colour	Band	Colour	Multiplier	Colour	Tolerence
Black	0	Silver	10^{-2}	Red	±2%
Brown	1	Gold	10^{-1}	Gold	±5%
Red	2	Black	$10^{0}=1$	Silver	±10%
Orange	3	Brown	$10^{1}=10$	No colour	±20%
Yellow	4	Red	10^{2}		
Green	5	Orange	10^{3}		
Blue	6	Yellow	10^{4}		
Violet	7	Green	10^{5}		
Grey	8	Blue	10^{6}		
White	9				

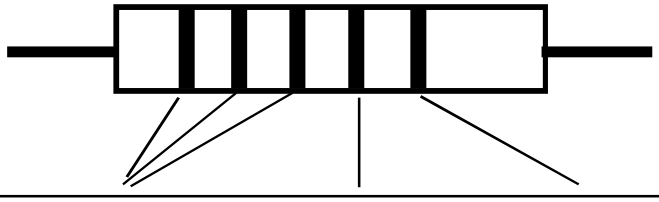
Example

Brown;	Black;	Red;	Gold
1	0	10^2	± 5%

Actual value = 1000 ± 5% Ω

Five Coloured Band Coding

Table 1.3



Colour	Band	Colour	Multiplier	Colour	Tolerence
Black	0	Silver	10^{-2}	Brown	± 1%
Brown	1	Gold	10^{-1}	Red	± 2%
Red	2	Black	$10^{0}=1$	Gold	± 5%
Orange	3	Brown	$10^{1}=10$	Silver	± 10%
Yellow	4	Red	10^{2}	No colour	± 20%
Green	5	Orange	10^{3}		
Blue	6	Yellow	10^{4}		
Violet	7	Green	10^{5}		
Grey	8	Blue	10^{6}		
White	9				

Example

Red; Yellow; Black; Black; Red
2 4 0 100 ± 2%
Actual value = 240 ± 2% Ω

1.3 DEVICE SYMBOLS

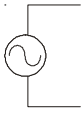
Earth:

Power supply:

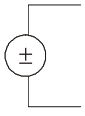
Battery (DC fixed power supply)

Variable DC power supply

AC source



DC source



Variable resistor:

Fixed resistor:

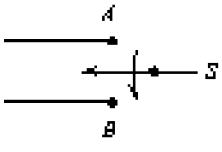
Fixed capacitor:

Variable capacitor

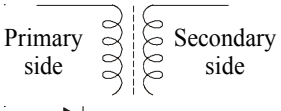
Fixed inductor:

Variable inductor:

Switch:



Transformer:

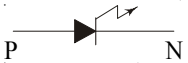


Diode:

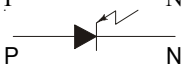
Tunnel diode

Zener diode:

Light emitting diode:

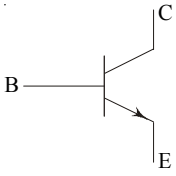


Light sensing diode:

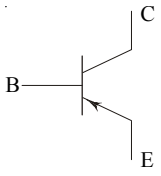


Transistor (BJT):

NPN

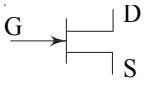


PNP

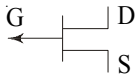


Junction Field effect transistor (JFET):

n-Channel



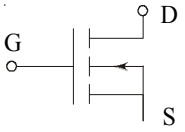
p-Channel



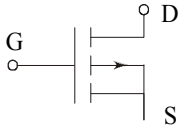
MOSFET:

Exhancement MOSFET:

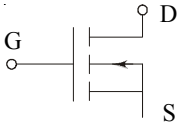
n-Channel

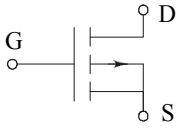


p-Channel

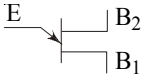


Depletion MOSFET:

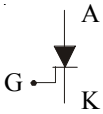




Uni-junction transistor:



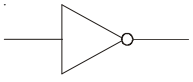
Silicon controlled rectifier:



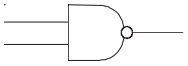
AND gate:

OR gate:

NOT gate:



NAND gate:



NOR gate:

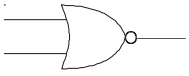
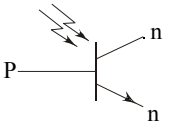
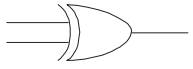


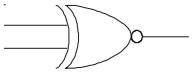
Photo transistor:



EX-OR gate:



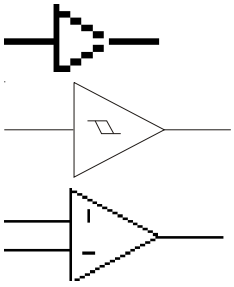
EX-NOR gate:



Buffer:

Schmitt trigger:

Op-amp:



1.4 POWER SUPPLY PRECAUTIONS AND MAINTENANCE

Power Supply: Specifications

Voltage supply: 230 V (± 10%), 50 Hz.

***Precautions* (CRO/ Function Generator/ Power Supply) :** The cover can be taken off after unplugging the power cord's trip contact connector. The case, chassis and all measuring terminals are to be connected to the protective earth contact of the inlet. The mains plug shall only be inserted in a socket outlet connected with a protective earth contact. The protective action must not be negated by the use of an extension cord without a protective conductor.

***Warning* :** *Any interruptions of the protection conductors inside or outside the instruments or disconnection of the protective earth terminals are likely to make the instrument dangerous. The mains plug should be inserted before connections are made to test circuits.*

Under certain conditions, 50 Hz hum voltage can occur in the circuit due to the instrumentation with other mains powered equipment or instrument. This can be avoided by using an insulation transformer between the mains outlet and power plug of the instrument.

It should be noted that generators always deliver an output but never take input and hence care should be taken that no input is given in any form to the output ports. If condensed water exists in the instrument, it should be acclimatized before switching on. The instruments should be kept in a clean and dry room and must not be operated in explosive, corrosive, dusty or moist environments. The ventilation holes must not be covered.

***Maintenance* :** The exterior of the instruments should be dusted with brushes. Dirt can be removed with moist cloth, spirit or washing benzene. The display can only be cleaned with water or washing benzene (not with spirit).

1.5 BASIC LAB INSTRUMENTS

***Ammeter* :** Ammeters are connected in series with the circuit whose current is to be measured. Therefore they should have a low electrical resistance. This is essential in order that they cause a small voltage drop and consequently absorb small power.

***Voltmeter* :** Voltmeters are connected in parallel with the circuit whose voltage is to be measured. They should have a high electrical resistance. This is essential in order that the current drawn by them is small and consequently the power absorbed is small.

***Ohmmeter* :** They are used for measurement of resistance. They incorporate a source of emf and a current measuring device.

Types of Instruments Used as Ammeters and Voltmeters

1. Permanent Magnet Moving Coil (PMMC) **:** This type can be used for DC measurements only. This is a more accurate type for DC measurement.

2. The Moving Iron and Moving Coil **:** Both these types depend upon the magnetic effect of current. It can be used for either DC or AC measurements.

3. Electrodynamic Meter **:** These types of instruments are used both for AC and DC measurement. Their calibrations for both DC and AC are the same and hence they are very useful as 'transfer instruments'.

4. Induction Type **:** These types of instruments are used for AC measurement alone. These induction principles are generally used for watt-hour meters than for ammeters and voltmeters owing to the comparatively high cost.

5. Electrostatic Type **:** As voltmeters, these have the advantage that their power consumption is exceedingly small. They can be made to cover a large range of voltage. Their main disadvantage is that the electrostatic principle is only directly applicable to voltage measurements.

CATHODE RAY OSCILLOSCOPE (CRO)

The cathode ray oscilloscope is the most versatile measuring instrument available. We can measure following parameters using the CRO:

1. AC or DC voltage
2. Time, $t = \frac{1}{f}$
3. Phase relationship
4. Waveform evaluation: Rise time; Fall time; On-time; Off-time; Distortion, etc.

We can also measure non-electrical physical quantities like pressure, strain, temperature, acceleration, etc., by converting into electrical quantity using a transducer.

Major Blocks

1. Cathode ray tube (CRT)
2. Vertical amplifier
3. Horizontal amplifier
4. Sweep generator
5. Trigger circuit

} = Signal synchronization unit.

6. Associated power supply

The Cathode Ray Tube The CRT is the heart of CRO. The CRT is enclosed in an evacuated glass envelope to permit the electron beam to traverse in the tube easily. The main functional units of CRO are as follows:

1. Electron gun assembly
2. Deflection plate unit
3. Screen

Electron Gun Assembly The electron gun assembly consists of an indirectly heated cathode and the necessary heater, a control grid, focussing anode and accelerating anode. The prime

purpose of the electron gun assembly is to provide a source of electron, converged and focussed into a narrow beam, which is accelerated toward the screen. The control grid is at negative potential which control the flow of electrons towards the screen. Due to focussing and accelerating anode, electrons are repelled away from the cylinder wall and therefore stream through the hole where they move into the electric field of the focussing and accelerating anodes. The accelerating anode exerts a force on the electron that will depend on the magnitude of the electric field and on the magnitude of the charge on the electrons.

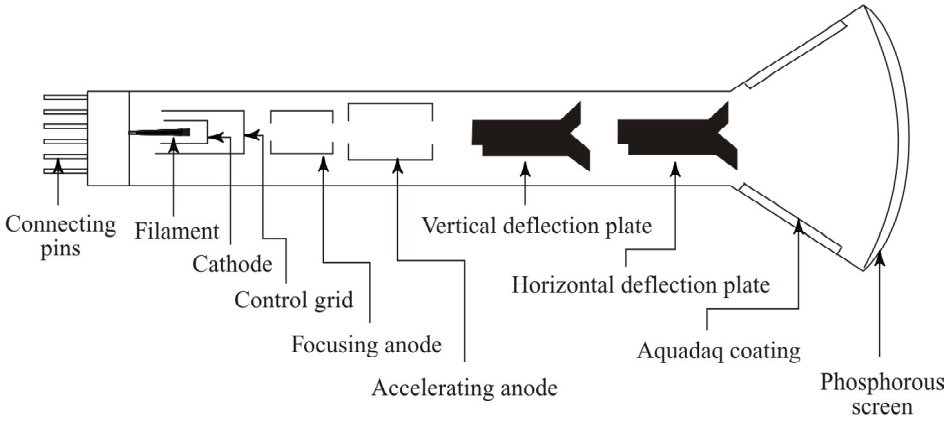


Fig. 1.1 Cathode ray tube

Deflection Plate Unit After the electrons leave the electron gun assembly, they enter and pass through the region controlled by the deflection plates. One pair of plates control the vertical motion of the beam while the other pair control the horizontal motion of the beam. The electron beam is deflected by a force exerted on each electron, but the beam must be deflected a considerable distance (e.g., TV). Electro-static deflection offers the advantages of higher frequency operation and the fact that the deflection plates are mounted inside the CRT saves space.

Screen When the electron beam strikes the phosphor-coated screen of the CRT, a spot of light is produced. When the electron strikes the phosphor-coated screen, it absorbs kinetic energy from the electrons and then gives up the energy in the form of light (fluorescence). The electrons that strike the screen are either repelled by the collision or cause secondary emission. To provide a return path to ground for these electrons, the inside surface of the CRT, except for the screen, is coated with a graphite substance called *Aquadag*.

The beam is deflected upward and to the right by the signal applied to the upper vertical deflection plate or to the right horizontal deflection plate. A signal to be displayed on the CRT screen is applied to the vertical input.

The purpose of the sweep generator is to develop a voltage at the horizontal deflection plate that increases linearly with time (ramp voltage). This ramp voltage causes the beam to be deflected equal distances horizontally per unit time.

In the normal operation, the switch is set to internal sweep. When the instrument is used in the X-Y mode (for phase measurement), the horizontal amplifier amplifies the signal that is applied to the horizontal input terminal.

Beam Deflection The amplitude of the deflecting voltages on both the horizontal and vertical deflection plates determines the position of the beam on the screen.

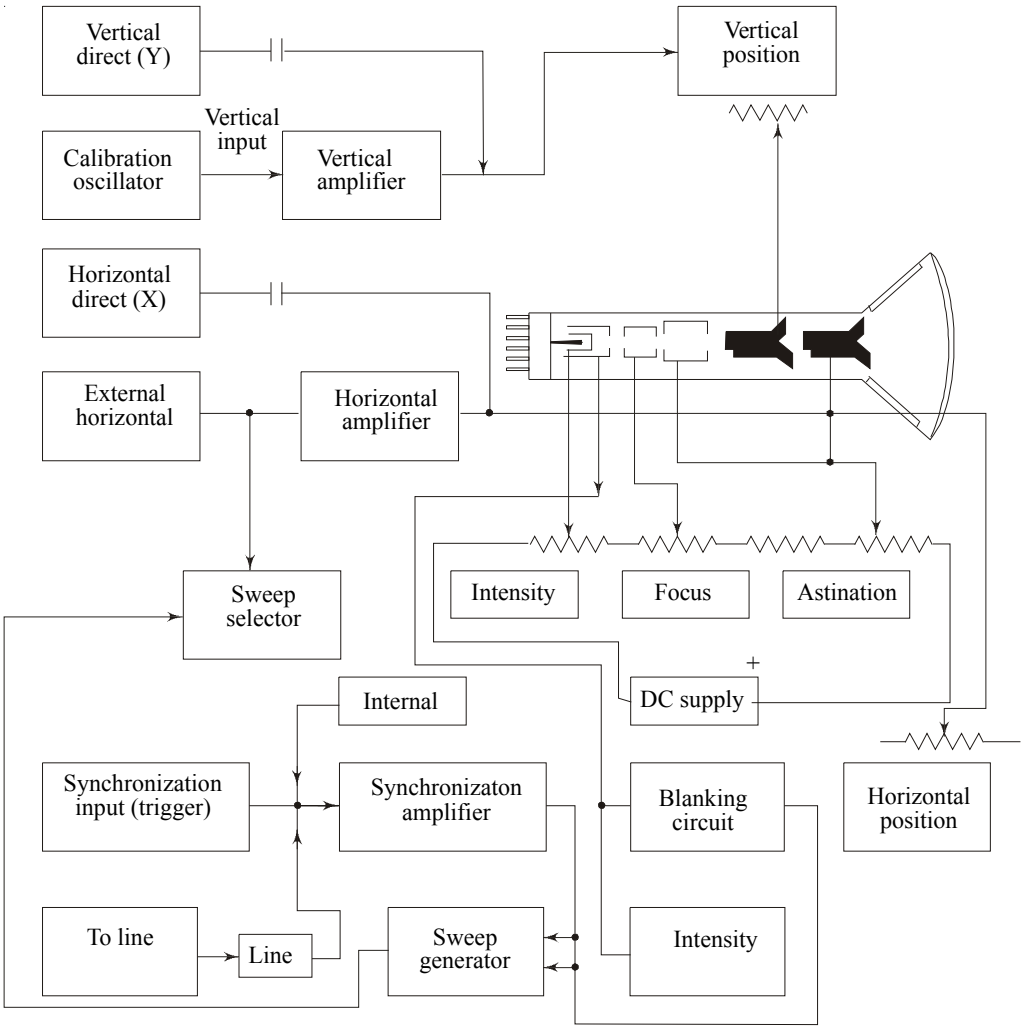


Fig. 1.2 Cathode ray oscilloscope

Vertical Amplifier The vertical amplifier is the main factor in determining the bandwidth and sensitivity of an oscilloscope. Vertical sensitivity is a measure of how much the electron beam will be deflected for a specified input signal. On the front panel of the oscilloscope, one can see a knob attached to a rotary switch labeled *volts/division*. The rotary switch is electrically connected to the input attenuation network. The setting of the rotary switch indicates what amplitude signal is required to deflect the beam vertically by one division.

Horizontal Amplifier Under normal mode of operation, the horizontal amplifier will amplify the sweep generator input. When the CRO is being used in the X-Y mode, the horizontal amplifier will amplify the signal applied to the horizontal input terminal. Although the vertical amplifier must be able to faithfully reproduce low-amplitude and high frequency signals with fast rise-time, the horizontal amplifier is only required to provide a faithful reproduction of the sweep signal which has a relatively high amplitude and slow rise time.

Sweep Generator If the waveform is to be accurately reproduced, the beam must have a constant horizontal velocity. Since the beam velocity is a function of the deflecting voltage, the

deflecting voltage must increase linearly with time. A voltage with this characteristic is called a ramp voltage.

During rise time of the sweep voltage, the beam moves from left to right across the CRT screen. The beam is deflected to the right by the increasing amplitude of the ramp voltage and the fact that the positive voltage attracts the negative electrons. During the fall time, the beam returns quickly to the left side of the screen. To prevent an undesirable retrace pattern from appearing on the screen during retrace, the control grid is generally *gated-off* which blanks out the beam during retrace.

Signal Synchronization Unit The beam will retrace the same pattern at a rapid rate if the vertical input signal and the sweep generator signal are synchronized. If the vertical input frequency is not exactly equal to, or an exact multiple of the sawtooth, the waveform will not be synchronized and the displays *run* across the screen. If the pattern moves towards the right, the frequency of the sawtooth waveform is too high, while movement of the pattern toward the left indicates that the frequency of the sawtooth is too low. When both signals are at the same frequency, an internal synchronous pulse will lock the sweep generator into the vertical input signal. Main limitation of this locking system is constant changes in the vertical input signal (frequency and amplitude). These limitations are overcome by incorporating a trigger circuit into the oscilloscope. The trigger circuit may receive input from one of three sources depending on the switch setting. The input signal may come from an external source when the trigger selector switch is set to EXT or from low amplitude AC voltage at line frequency when the switch is set to LINE or from the vertical amplifier when the switch is set to INT. When set for INT (internal triggering), the trigger circuit receives its inputs from the vertical amplifier.

Dual Trace Oscilloscope It has two vertical input channels and the electronic switch that alternately connects the two input channels to the vertical amplifier. There are generally atleast four modes of operations. They are *A, B, Alternate and Chopped*. When set in A or B only, the input at that channel is displayed. In the alternate mode, the inputs are displayed on alternate trace. The alternate mode of operation is generally preferred when displaying relatively high frequency signals. The switching rate is synchronized with the sweep generator. In the chopped mode, electronic switch occurs at a rate completely independent of the sweep rate and therefore each display has portions missing during which time the other signal is being displayed. The chopped mode is normally used at low sweep rate when the alternate mode would provide a display with appreciable flicker.

Phase Angle Computation (X–Y mode)

Phase angle, $$\theta = \text{Sin}^{-1}\left(\frac{Y_1}{Y_2}\right)$$

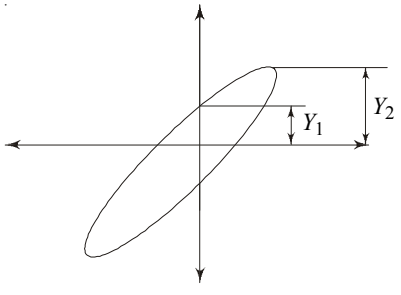


Fig. 1.3 Phase angle plot

Major Blocks in a Practical CRO

A CRO consists of a cathode ray tube (CRT) and additional control knobs. The main parts of a CRT are:

1. Electron gun assembly.
2. Deflection plate assembly.
3. Fluorescent screen.

Electron Gun Assembly The electron gun assembly produces a sharp beam of electrons, which are accelerated to high velocity. This focussed beam of electrons strikes the fluorescent screen with sufficient energy to cause a luminous spot on the screen.

Deflection Plate Assembly This part consists of two parallel plates in which one pair of plates is placed horizontally and other pair of plates is placed vertically. The signal under test is applied to vertical deflecting plates. The horizontal deflection plates are connected to a built-in ramp generator which moves the luminous spot periodically in a horizontal direction from left to right over the screen. These two deflection plates give the actual waveform. The rate at which it traces the waveform gives stationery appearance to the waveform on the screen. CRO operates on voltage. Since the deflection of the electron beam is directly proportional to the deflecting voltage, the CRT may be used as a linear measuring device.

The voltage being measured is applied to the vertical plates through an iterative network, whose propagation time corresponds to the velocity of electrons, thereby synchronizing the voltage applied to the vertical plate with the velocity of the beam.

Synchronization of Input Signal The sweep generator produces a sawtooth waveform, which is used to synchronize the applied signal to obtain a stationary–applied signal. This requires that the time base be operated at a submultiple frequency of the signal under measurement. If synchronization is not done, the pattern is not stationary, but appears to drift across the screen in a random fashion.

Internal Synchronization This trigger is obtained from the time base generator to synchronize the signal.

External Synchronization An external trigger source can also be used to synchronize the signal being measured.

Auto-Triggering Mode The time base used in this case in a self-oscillating condition, i.e., it gives an output even in the absence of any Y-input. The advantage of this mode is that the beam is visible on the screen under all conditions, including the zero input. When the input exceeds a certain magnitude then the internal free-running oscillator locks on to the frequency of the input signal and provides a stable synchronized display. This is so for all frequencies of the input higher than the free running frequency of the time base generator in the auto mode. When the frequency of the Y-input is less than this, synchronization is not assured and the 'AC trigger' mode has to be used. In the AC trigger mode, the time base generator is controlled by a monostable multivibrator, which in turn is triggered by a set level obtained from the Y-amplifier output. In HF trigger mode, triggering amplifier is bypassed internally, to avoid failure of triggering due to delays arising from the triggering amplifier. In this mode, the repetition rate of time base is higher as compared to that in the auto mode.

The bombarding electrons, striking the screen, release secondary emission electrons. These secondary electrons are collected by an aqueous solution of graphite.

The bandwidth of an oscilloscope normally refers to the 3dB bandwidth of the vertical amplifier in the normal sensitivity range.

Position Control Applying small independent internal DC voltage to the deflecting plates does the positioning of the trace and control can be done with the help of a potentiometer.

Focus Control The focussing electrode acts like a lens whose focal length can be changed using a potentiometer. It will align the beam without spreading outwards.

Intensity Control Varying the potentiometer connected to the grid voltage can vary the intensity of the beam. Intensity basically refers to the number of electrons ejected from the plate of the electron gun. This in turn depends upon the filament heating.

Z-Modualtion The voltage applied to the grid of the CRT in this case can be controlled by an external signal connected to the Z-mode input. This is used for brightening the display.

Calibration Circuit Square wave (generally) whose amplitude and frequency is calibrated to a definite value (say 0.2 V at 1 kHz) for calibration as well as testing purpose.

1.6 INTRODUCTION TO NETWORK

An electrical network is a combination of many electrical elements like resistors, capacitors, inductors, etc. Network analysis deals with the analysis of the response of the network for the given excitation.

Fig. 1.4 Two port network

If the relationship of response to excitation is linear, i.e., change in input results in a corresponding change in output, then the electrical network is said to be *linear*.

Active and Passive Elements

Active Elements An active element is one, which is capable of generating the energy on its own. Examples, transistor, current source, FET, etc.

Passive elements A passive element is one, which is incapable of generating energy on its own. But it is capable of storing and dissipating energy. It always needs some external source of power. Examples, resistor, capacitor, inductor, etc.

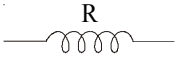
Network Elements

Resistor A resistor is a passive circuit element, which consumes energy. All electrical devices, which consume energy, must have resistance in their circuit model. The power consumed by a resistor is given by

Power, $P = I^2R$

where, I = current flowing through the resistor R.

- I = DC current (capital letter)
- i = AC current (small letter)



This resistance can be defined by ohm's law, i.e., *at a constant temperature, the voltage drop between ends of a conductor is directly proportional to the current flowing through it.*

Therefore, $I \propto V$

$$I = kV = \frac{1}{R} V$$

where, k = constant of proportionality = $\frac{1}{R}$

R = resistance of the conductor (ohm, Ω)

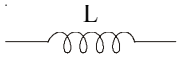
$V = IR$

Inductor An inductor is a circuit element, which is capable of storing energy in the form of current for some period of time, and delivers the same after this time. The average power for inductor is zero. Inductor plays a vital role in electric motor, transformer, etc.

They are usually made of many turns of fine wires wound in a coil form. For an ideal inductance, the voltage is proportional to the rate of change of the current, i.e.,

$$e(t) \propto \frac{di}{dt}$$

$$e(t) = L \frac{di}{dt}$$



where, L = inductance (Henry, H)

The current in the inductance can be found out by integrating above equation with respect to time. Therefore,

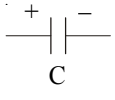
$$i(t) = \frac{1}{L} \int e(t)\ dt$$

energy stored, $P = 1/2\ LI^2$

Capacitor A capacitor is a circuit element, which is capable of storing energy in the form of voltage, during some period and returns during other time. Thus the average power for a capacitor is zero.

For an ideal capacitor, the voltage is proportional to the integral of current, i.e.,

$$e(t) = \frac{1}{C} \int i\, dt \qquad (1)$$



where, C = capacitor (Farad, F)

The voltage is proportional to the change in charge to the change in capacitance, i.e.,

$$e(t) = \frac{dQ}{dC} \qquad (2)$$

The current in the capacitance can be found out by differentiating equation (1) with respect to time, i.e.,

$$i = C\frac{dv}{dt} \qquad (3)$$

energy stored, $P = 1/2\ CV^2$

Energy Source

Ideal Current Source The ideal current source is one which produces a constant current irrespective of the voltage across it.

It is necessary to connect the current source to some external circuit to complete the path of the current. An ideal current must be capable of supplying infinite power.

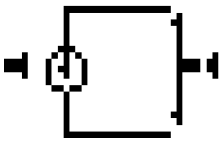


Fig. 1.5 Ideal current source

Ideal Voltage Source The ideal voltage source is one, which produces constant voltage irrespective of current through it. The voltage source can be symbolically represented by,

Fig. 1.6 (a) DC voltage source (b) AC voltage source

When the voltage source become open-circuited, it does not draw any current and hence power is zero. If the voltage source is short-circuited, then infinite amount of current flows through it and hence power is infinity.

Dependent and Independent Sources Ideal current and voltage sources are examples of independent sources. In case of dependent sources, the source voltage or current is not constant, but it depends on a voltage or current of some other source. They are broadly divided into following types:

1. Current controlled current source
2. Current controlled voltage source
3. Voltage controlled current source
4. Voltage controlled voltage source

Mutual Inductance Mutual inductance is due to mutual interaction of the magnetic field created by the inductance. Thus, when a magnetic field is produced by a changing current in one inductor, it induces a voltage in another inductor.

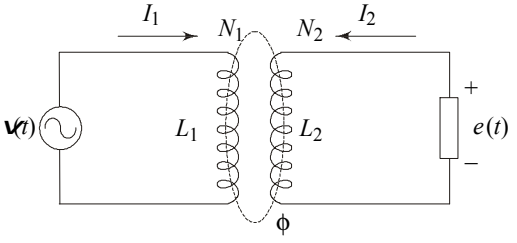


Fig. 1.7 Mutual inductance

The above principle is obtained from the *Faraday's law*. According to this law, *a coil containing N turns, with a magnitude of flux, ϕ, linking each turn, has an induced emf*,

$$e = -N \frac{d\phi}{dt}$$

A negative sign is frequently included in this equation to signal that the voltage polarity is established according to *Lenz's law*.

By definition of self inductance, the voltage is given by

$$L\frac{di}{dt} = N\frac{d\phi}{dt}$$

or, $$L = N\frac{d\phi}{dt}$$

where, ϕ = flux (Weber, Wb)

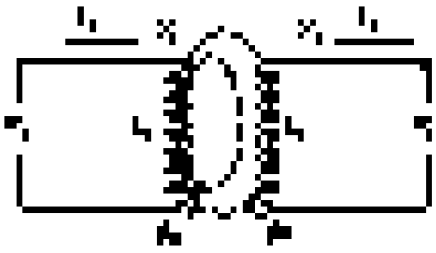


Fig. 1.8 Flux linkage in a transformer

Coupling Co-efficient The total fluxes ϕ, resulting from current i_1 through the N_1 consist of leakage flux ϕ_{11} and coupling flux ϕ_{12}. The induced emf in coupled coils is given by,

$$e = M\frac{di}{dt} = N_2\frac{d\phi_{12}}{dt}$$

Therefore, $$M = N_2\frac{d\phi_{12}}{dt_1}$$

where, M = mutual inductance

As the coupling is bilateral, $M = N_1\dfrac{d\phi_{21}}{dt_2}$

The coupling co-efficient k, is defined as the ratio of linking flux to the total flux,

$$k = \frac{\phi_{12}}{\phi_1} = \frac{\phi_{21}}{\phi_2} \quad [0 \le k \le 1]$$

Therefore, $$M = k\sqrt{L_1L_2}$$

If $k = 1$, then all the flux from one coil is transferred to other without any leakage in flux (close coupling). For $k = 0$, no flux from one coil induces a voltage in the other.

Transformer An ideal transformer is a hypothetical transformer in which there are no losses and the core has infinite permeability, resulting in perfect coupling with no leakage flux. In large power transformer, the losses are small relative to the power transferred.

Passive Element Configuration

Resistors in Series

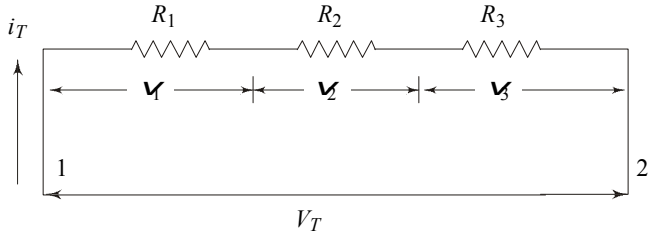


Fig. 1.9(a) Resistors in series

$$v_T = v_1 + v_2 + v_3$$

where v_T = total voltage and v_1, v_2 and v_3 are the voltage drops across the resistors R_1, R_2 and R_3 respectively.

We know from ohm's law, $v = iR$.

Therefore, $$i_T R_{eq} = i_T R_1 + i_T R_2 + i_T R_3$$

where R_{eq} = equivalent (effective) resistance.

When resistors are connected in series, the total voltage across two terminals, (say, 1 and 2) is equal to the algebraic sum of individual voltages across each resistance. The current flowing through all resistors is the same. Therefore,

$$R_{eq} = R_1 + R_2 + R_3$$

When resistors are connected in series, the equivalent resistance is the addition of all the resistors connected in series.

Resistors in Parallel

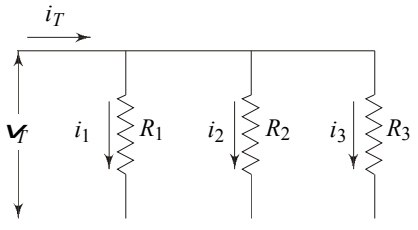


Fig. 1.9(b) Resistors in parallel

$$i_T = i_1 + i_2 + i_3$$

where i_T = Total current and i_1, i_2 and i_3 are the currents flowing through the resistors R_1, R_2 and R_3 respectively.

But we know from ohm's law, $v = iR$.

Therefore, $$\frac{V_T}{R_{eq}} = \frac{V_t}{R_1} + \frac{V_t}{R_2} + \frac{V_t}{R_3}$$

where R_{eq} = equivalent (effective) resistance

When resistors are connected in parallel, the total current is equal to the algebraic sum of individual current flowing through each resistor. The voltage across each resistor is the same (all are connected in parallel with source). Therefore,

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$$

Inductors in Series

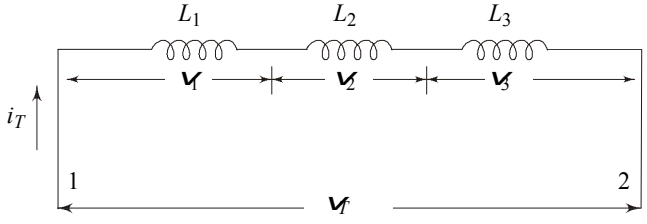


Fig. 1.10(a) Inductors in series

If inductors are connected in series, the total voltage drop is equal to the algebraic sum of the voltage drop across each inductor. The current flow remains the same in all inductors.

$$v_T = v_1 + v_2 + v_3$$

where v_T = total voltage and v_1, v_2 and v_3 are the voltage drops across the inductors L_1, L_2 and L_3, respectively.

But we know from ohm's law, $v = L\dfrac{di}{dt}$

Therefore, $$L_{eq}\frac{di}{dt} = L_1\frac{di}{dt} + L_2\frac{di}{dt} + L_3\frac{di}{dt}$$

where L_{eq} = equivalent (effective) inductance.

When inductors are connected in series, the total voltage across two terminals (say, 1 and 2) is equal to the algebraic sum of individual voltages across each inductor. The current flowing through all inductors is the same. Therefore,

$$L_{eq} = L_1 + L_2 + L_3$$

When inductors are connected in series, the equivalent inductance is the addition of all the inductors connected in series.

Inductors in Parallel If inductors are connected in parallel, the total current is equal to the algebraic sum of currents in each inductor. The voltage drop across all the inductors remains the same.

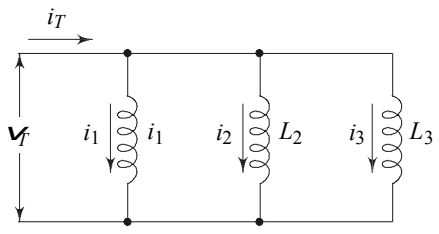


Fig. 1.10(b) Inductors in parallel

$$i_T = i_1 + i_2 + i_3$$

Where i_T = total current and i_1, i_2 and i_3 are the currents flowing through the inductors L_1, L_2 and L_3, respectively.

But we know, $$i = \frac{1}{L}\int v\,dt$$

Therefore, $$\frac{1}{L_{eq}}\int v\,dt = \frac{1}{L_1}\int v\,dt + \frac{1}{L_2}\int v\,dt + \frac{1}{L_3}\int v\,dt$$

where L_{eq}= equivalent (effective) inductance.

If inductors are connected in parallel, the total current (i_T) is equal to the algebraic sum of the individual current flowing through each inductor. The voltage drop across each inductor remains the same.

$$\frac{1}{L_{eq}} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3}$$

Capacitors in Series

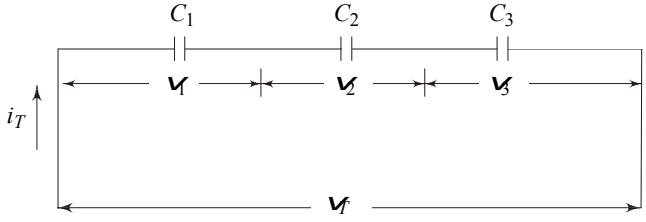


Fig. 1.11(a) Capacitors in series

If capacitors are connected in series, the total voltage drop is equal to the algebraic sum of the voltage drop across each capacitor. The current flow remains the same in all capacitors.

$$v_T = v_1 + v_2 + v_3$$

where v_T = total voltage and v_1, v_2 and v_3 are the voltage drops across capacitors C_1, C_2 and C_3, respectively.

But we know from ohm's law, $v = \frac{1}{C}\int i\,dt$

Therefore, $$\frac{1}{C_{eq}}\int i dt = \frac{1}{C_1}\int i dt + \frac{1}{C_2}\int i dt + \frac{1}{C_3}\int i dt$$

where C_{eq} = equivalent (effective) capacitance.

When capacitor are connected in series, the total voltage across two terminals (say, 1 and 2) is equal to the algebraic sum of the individual voltages across each capacitor. The current flowing through all the capacitors is same. Therefore,

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$

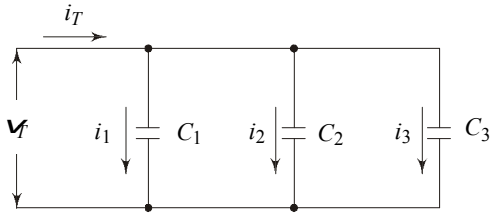


Fig. 1.11(b) Capacitors in parallel

Capacitors in Parallel If capacitors are connected in parallel, the total current is equal to the algebraic sum of currents in each capacitor. The voltage drop across all capacitors remains the same.

$$i_T = i_1 + i_2 + i_3$$

where i_T = total current and i_1, i_2 and i_3 are the currents flowing through the capacitors C_1, C_2 and C_3, respectively.

But we know that, $$i = C\frac{dv}{dt}$$

Therefore, $$C_{eq}\frac{dv}{dt} = C_1\frac{dv}{dt} + C_2\frac{dv}{dt} + C_3\frac{dv}{dt}$$

where C_{eq} = equivalent (effective) capacitance.

$$C_{eq} = C_1 + C_2 + C_3$$

When capacitors are connected in parallel, the equivalent capacitance is the addition of all parallel connected capacitors.

Network Simplification

1. Delta (Δ) to Star (γ) Conversion

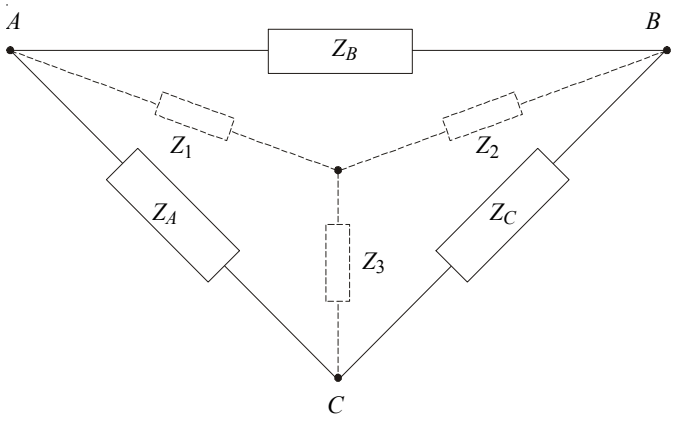


Fig. 1.12(a) Delta to star conversion

$$Z_1 = Z_A\, Z_B/(Z_A + Z_B + Z_C)$$
$$Z_2 = Z_B\, Z_C/(Z_A + Z_B + Z_C)$$
$$Z_3 = Z_C\, Z_A/(Z_A + Z_B + Z_C)$$

2. Star (γ) to Delta (Δ) Conversion

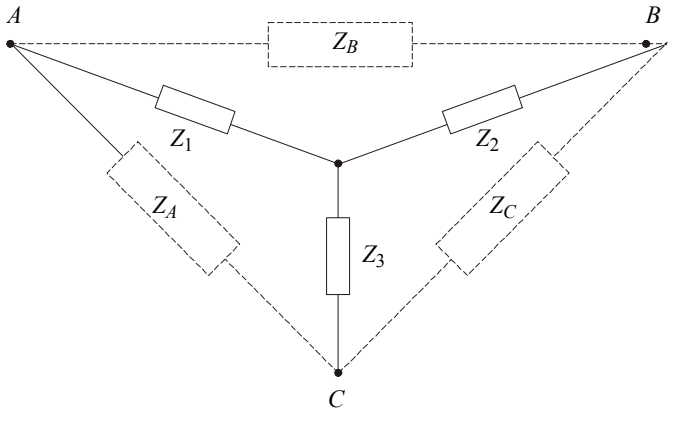


Fig. 1.12(b) Star to delta conversion

$$Z_A = (Z_1Z_2 + Z_2Z_3 + Z_3Z_1)/Z_2$$
$$Z_B = (Z_1Z_2 + Z_2Z_3 + Z_3Z_1)/Z_3$$
$$Z_C = (Z_1Z_2 + Z_2Z_3 + Z_3Z_1)/Z_1$$

1.7 OHM'S LAW

At a constant temperature, the current flowing through a conductor is directly proportional to the voltage difference across the conductor. The proportionality constant is given by $1/R$.

$$V \propto I$$
$$V = \left(\frac{1}{R}\right)I$$

where, R = resistance of the conductor (Ohm, Ω).

1.8 KIRCHHOFF'S LAW

Kirchhoff's Current Law (KCL) The connection of two or more circuit elements (branches) creates a junction called a *node*.

It states that at any node, the sum of the currents entering is equal to the sum of the currents leaving.

Current entering a node (N): I_A, I_B

Current leaving a node (N): I_C, I_D, I_E

According to KCL, $I_A + I_B = I_C + I_D + I_E$

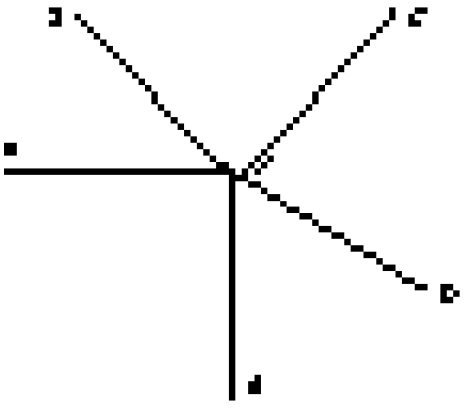


Fig. 1.13 Kirchhoff's current law

Kirchhoff's Voltage Law (KVL) *For any closed path in any network, the algebraic sum of the emfs is equal to the algebraic sum of the IR drops.*

Emfs are V_1 and V_2

IR drops are $V_{R1} = IR_1$, $V_{R2} = IR_2$,

$V_{R3} = IR_3$.

According to KVL,

$$V_1 + (-V_2) = IR_1 + IR_2 + IR_3$$

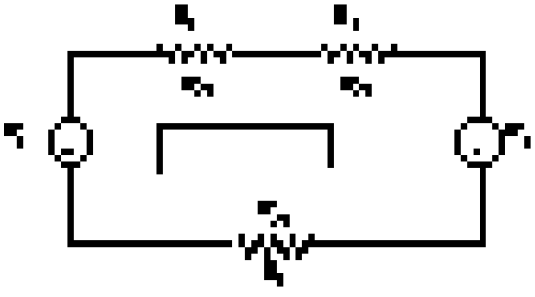


Fig. 1.14 Kirchhoff's voltage law

1.9 SUPERPOSITION THEOREM

Statement *In a linear bilateral network containing more than one generator, the current flowing through any branch is the algebraic sum of the currents flowing through that branch when generators are considered one at a time and replacing other generators by their internal impedance.*

Let us consider a general network,

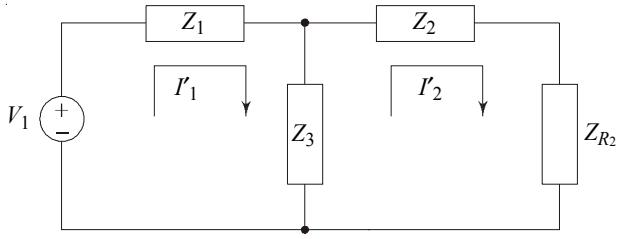


Fig. 1.15(a) General T-network with two DC source

Current through Z_3 is $(I_1 - I_2)$ due to source V_1 and V_2.

According to superposition theorem, let us consider source V_1 alone as shown in figure below.

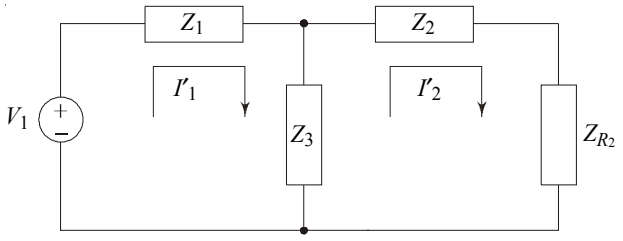


Fig. 1.15(b) T-network with one DC source

Z_{R2} = internal impedance of the source V_2.

Current through Z_3 is $(I'_1 - I'_2)$ due to source V_1 alone.

Now, let us consider source V_2.

V_1 is replaced by its internal impedance Z_{R1}. Current through Z_3 is $(I''_1 - I''_2)$ due to source V_2 alone.

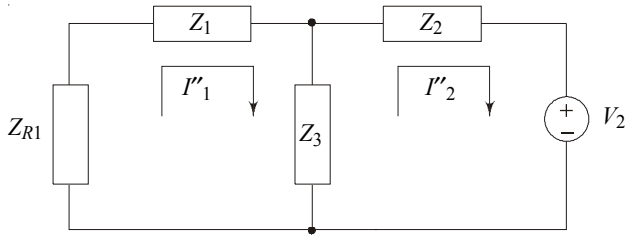


Fig. 1.15(c) T-network with one DC source

According to superposition theorem, the current (actual) flowing through the impedance Z_3 is given by,

$$(I_1 - I_2) = (I'_1 - I'_2) + (I''_1 - I''_2)$$

Experiment (Superposition Theorem)

Aim: ***To Verify the Superposition Theorem***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30)V	2
Ammeter	(0-10) mA	1

Circuit Diagram:

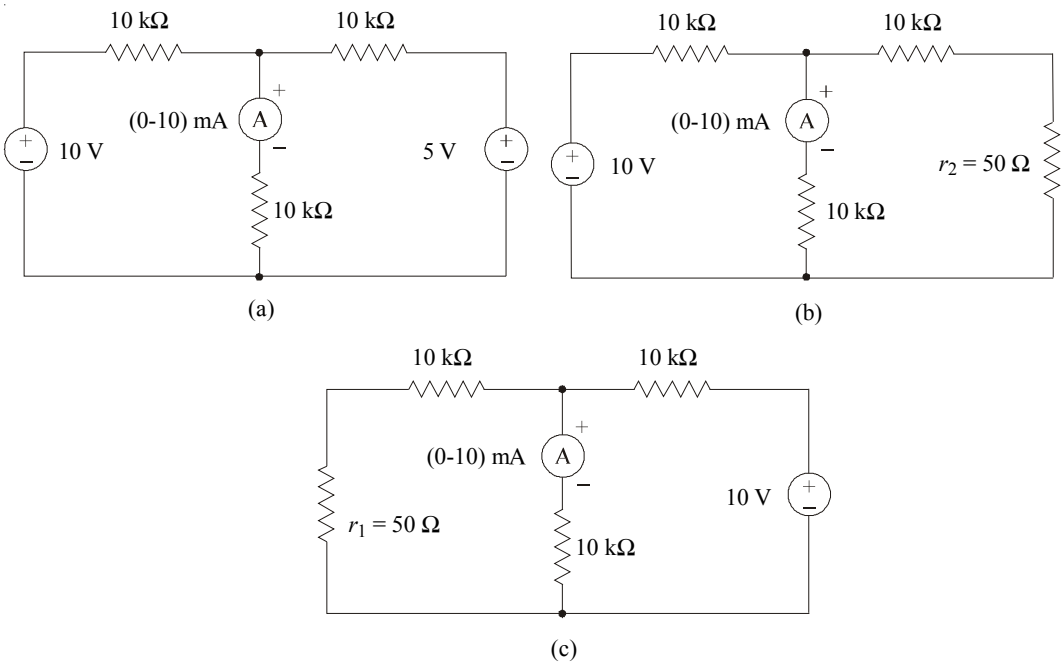


Fig. 1.16

Procedure:

1. Connect the circuit as per the circuit diagram [Fig. 1.16 (a)].
2. Switch on the DC power supplies (10 V and 5 V) and note down the corresponding ammeter readings (say I).
3. Replace the second power supply by its internal resistance [Fig. 1.16 (b)].
4. Switch on the power supply (10 V) and note down the corresponding ammeter reading (say I_1).
5. Connect back the second power supply (5 V) and replace the first power supply by its internal resistance [Fig. 1.16 (c)].
6. Switch on the power supply (5 V) and note down the corresponding ammeter reading (say I_2).
7. Verify the following condition:

$$I = I_1 + I_2$$

Tabular Column:

I_1(mA)	I_2(mA)	$I_1 + I_2$ (mA)	I (mA)

Exercise:

1. Repeat the above-mentioned procedure for asymmetrical network and compare with the symmetrical network.
2. Verify superposition theorem for π-network.

1.10 MAXIMUM POWER TRANSFER THEOREM

Statement: *Maximum power will be delivered by a network to the load, if the impedance of the network (Z_N) is a complex conjugate of load impedance (Z_L) and vice versa.*

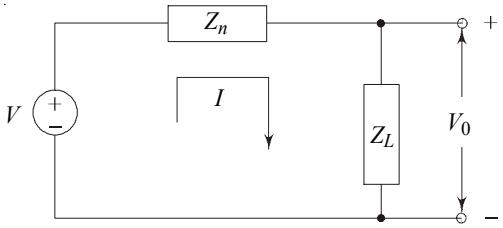


Fig. 1.17 General network

Current through the network is,

$$I = V / (Z_N + Z_L) \qquad (1)$$

where, $Z_N = R_N + jX_N$; $Z_L = R_L + jX_L$.

Therefore, $$I = \left[\frac{V}{(R_N + jX_N)(R_L + jX_L)}\right]^2 \qquad (2)$$

The power delivered by the load is given by,

$$P = I^2 R_L$$

or, $$P = \left[\frac{V}{(R_N + jX_N)(R_L + jX_L)}\right]^2 \times R_L \qquad (3)$$

For maximum power, $$\frac{dP}{dX_L} = 0$$

or, $$\frac{dP}{dX_L} = (X_L + X_N) = 0$$

or, $$X_L = -X_N \qquad (4)$$

The reactance of the load impedance (X_L) is of opposite sign to the reactance of the network (X_N). Substitute equation (4) in equation (3), then the equation for power (P) reduces to,

$$P_L = \frac{V^2 R_L}{(R_L + R_N)^2}$$

For maximum power, $$\frac{dP}{dR_L} = 0$$

$$\frac{dP}{dR_L} = -R_L^2 + R_N^2 = 0$$

Therefore, $$R_L = R_N$$

If we make $X_L = -X_N$ and $R_L = R_N$, maximum power will be transformed from the network to load. For maximum power transfer, load impedance (Z_L) should be complex conjugate of the network impedance (Z_N).

Experiment (Maximum Power Transfer Theorem)

Aim: ***Verification of Maximum Power Transfer Theorem***

Equipment required:

Equipment	Range	Quantity
Signal generator	(0 – 1)MHz	1
AC Ammeter	(0 – 100M)A	1
AC Voltmeter	0 – 10V	1

Circuit Diagram:

$$P = \frac{V^2}{4\,R_L} \text{ watts}$$

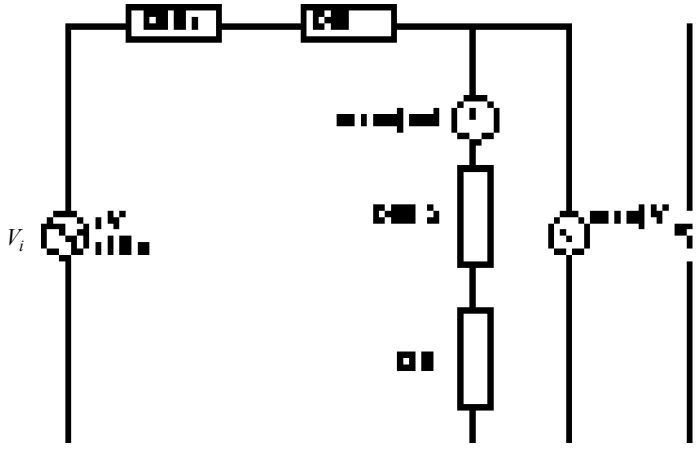


Fig. 1.18 (a)

* DRB: Decade Resistance Box
DIB: Decade Inductance Box
DCB: Decade Capacitance Box

Procedure:

1. Connect the circuit as per the circuit diagram.
   Set the input signal (say IV, 1KHz)
2. Set the network DRB and DIB at some random value (say 1k Ω & 1 mH).
3. Set the load DRB to the value equal to the network DRB (1k Ω) and vary the DCB of the load in regular steps.
4. Note down the corresponding voltmeter and ammeter readings.
5. Plot the graph: Power vs capacitance reactance.
6. Now set the load reactance equal to the network reactance.
7. Vary the DRB of the load in regular steps.
8. Note down the corresponding voltmeter and ammeter readings.
9. Plot the graph: Power vs load resistance.
10. Compare the peak power of both the cases.

Tabular Column:

Case (A): $R_L = R_N = 1\text{k}\,\Omega$;

X_C (Ω)	V (Volts)	I (mA)	$P = VI$

Case (B): $X_L = -X_C = 1$ mH/1mF

R_L (Ω)	V (Volts)	I (mA)	$P = VI$

Model Graphs:

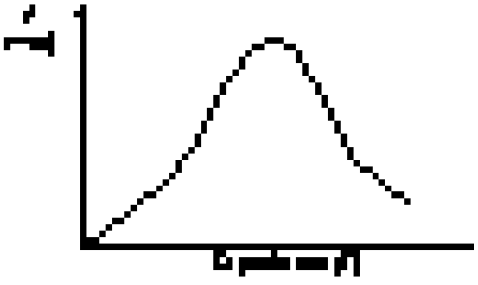


Fig. 1.18(b)

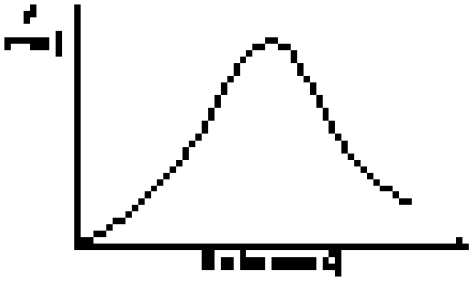


Fig. 1.18(c)

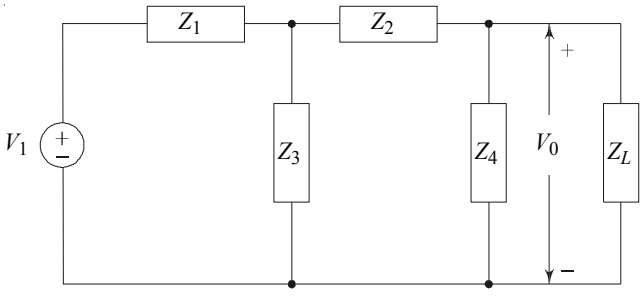
Exercise:

1. Give some practical examples for maximum power transfer theorem.

1.11 THEVENIN'S THEOREM

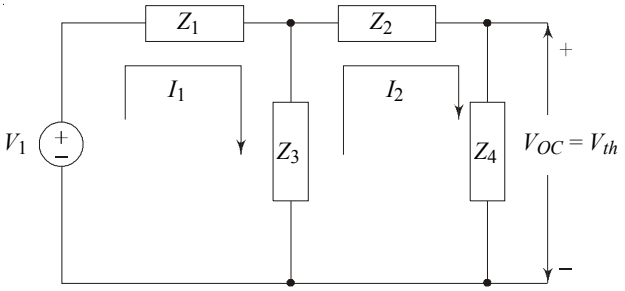
Statement: *Any linear bilateral network containing one or more voltage sources can be replaced by a single voltage source whose value is equal to the open circuit voltage at output terminal with a series Thevenin's resistance. The Thevenin's resistance is equal to the effective resistance looking back from the output terminal by removing the load resistance.*

Let us consider a general circuit,



(a)

Fig. 1.19 (a) General network



(b)

Fig. 1.19 (b) Network for open-circuit voltage calculation

Open circuit voltage (V_{th}) calculation:

$$V_{oc} = V_{th} = I_2 Z_4$$

Apply KVL to the given network,

$$V_1 = I_1 Z_1 + (I_1 - I_2) Z_3 \quad (1)$$

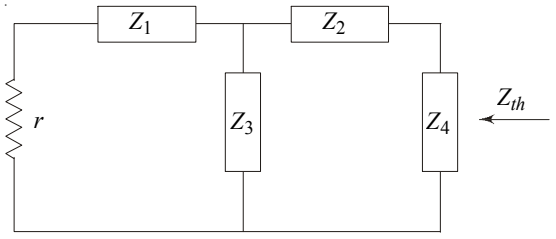
$$0 = (I_2 - I_1) Z_3 + Z_2 I_2 + Z_4 I_2 \quad (2)$$

On simplifying equation (1) and (2), we get

$$I_2 = \frac{V_1 Z_2}{(Z_2 + Z_3 + Z_4)(Z_1 + Z_2) + Z_2^2}$$

$$V_{oc} = V_{th} = I_2 Z_4$$

$$V_{oc} = \frac{V_1 Z_2 Z_4}{(Z_2 + Z_3 + Z_4)(Z_1 + Z_2) + Z_2^2}$$



(c)

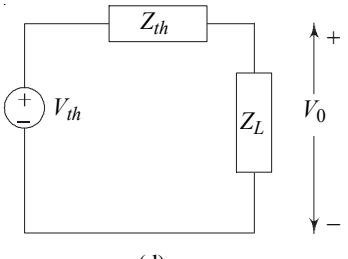
Fig. 1.19 (c) Network for Thevenin's resistance calculation

Thevenin's resistance calculation:

Short the voltage source and replace it by its internal resistance, r.

$$Z_{in} = Z_{th} = \{[(r + Z_1) \parallel Z_3] + Z_2\} \parallel Z_4$$

The Thevenin's network is given by,



(d)

Fig. 1.19 (d) Thevenin's network

Experiment (Thevenin's Theorem)

Aim: ***Verification of Thevenin's Theorem***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0–10)V	1
Voltmeter	(0–10)V	1
Multimeter		1

Circuit Diagram:

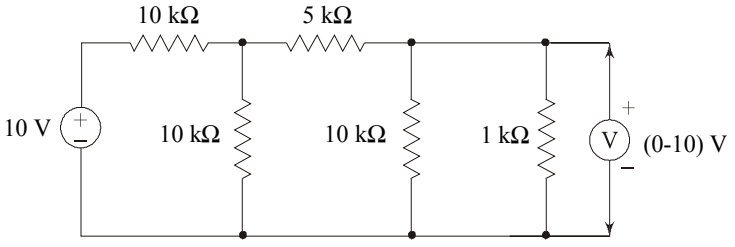


Fig. 1.20(a)

Thevenin's Voltage Experiment Set Up:

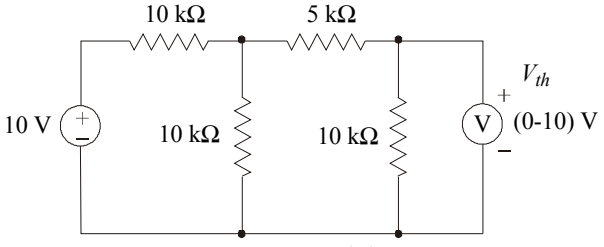


Fig. 1.20(b)

Thevenin's Resistance Experimental Set Up:

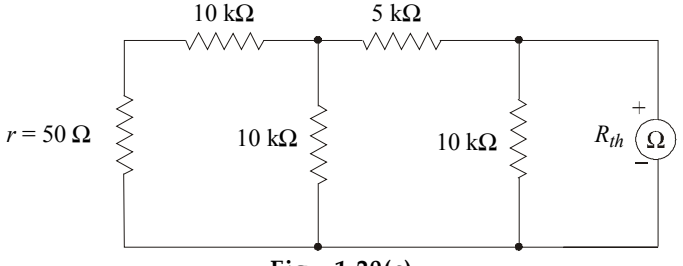


Fig. 1.20(c)

Thevenin's Circuit:

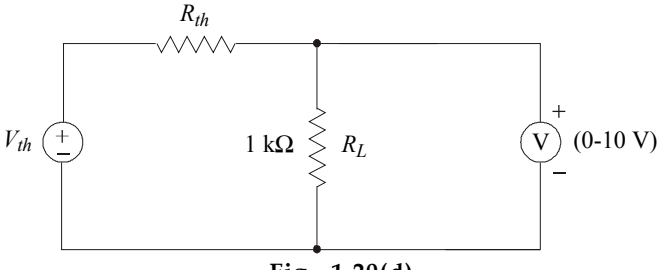


Fig. 1.20(d)

Procedure:

1. Connect the circuit as per the circuit diagram [Fig. 1.20 (a)]
2. Measure the voltage across the load using proper voltmeter.

To Find Thevenin's Voltage:

1. Connect the circuit as per the circuit diagram [Fig. 1.20 (b)]
2. Remove the load resistance and measure the open circuited voltage across the output terminal using voltmeter (V_{th}).

To Find Thevenin's Resistance:

1. Connect the circuit as per the circuit diagram [Fig. 1.20 (c)]
2. Replace the supply by its internal resistance and open circuit the load.
3. Using multimeter in resistance mode measure the resistance across the output terminal (R_{th}).

Thevenin's Circuit:

1. Connect the power supply (V_{th}) and resistance (R_{th}) in series as shown in the circuit diagram [Fig. 1.20 (d)].
2. Connect the load resistance (1 kΩ).
3. Switch on the power supply and measure the voltage drop across load resistance using voltmeter.
4. Voltage measured at figure are 1.20 (a) should be equal to the voltage measured at Fig. 1.20 (d).

Tabular Column:

Voltage (Fig.) (Volts)	Open circuit voltage (Volts)	Thevenin's resistance (Ω)	Voltage (Fig.) (Volts)

Exercise:

1. Conduct the experiment using two DC power supplies connected at any two branches.

1.12 NORTON'S THEOREM

Statement *Any linear bilateral network containing one or more generators can be replaced by an equivalent circuit consisting of current source (I_{nor}) in parallel with admittance (Y_{nor}). The I_{nor} is the short-circuited current flowing through the output terminals and Y_{nor} is the admittance measured across the output terminals with all the sources replaced by its internal impedance.*

Let us consider a general network,

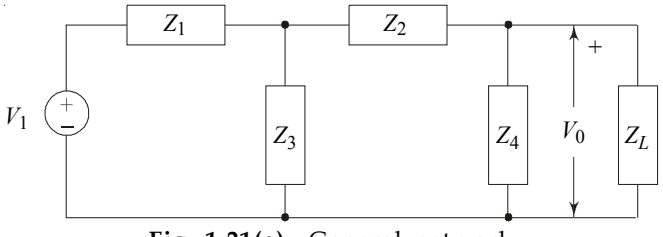


Fig. 1.21(a) General network

Short-circuited current ($I_{SC} = I_{NOR}$) calculation:

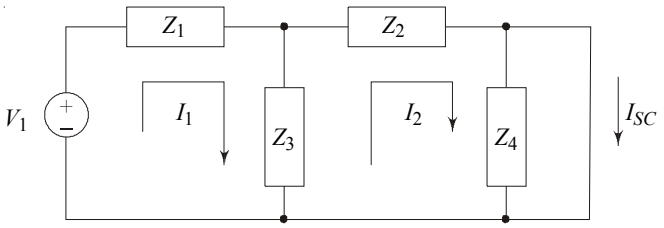


Fig. 1.21(b) Network for short-circuit current calculation

Current always takes least resistance path. Therefore, there is no current through Z_4. All current flows through the short-circuited path (I_{SC}).

$$V = I_1 Z_1 + (I_1 - I_2)\, Z_3 \tag{1}$$

$$0 = (I_2 - I_1)\, Z_3 + Z_2\, I_2 \tag{2}$$

Simplify equation (1) and (2), we get

$$I_2 = I_{SC} = I_{NOR} = \frac{V_1 Z_2}{(Z_2 + Z_3)(Z_1 + Z_2) + Z_2^2}$$

Norton's admittance calculation:

Replace the source (power supply) with its internal resistance. The circuit diagram reduces to,

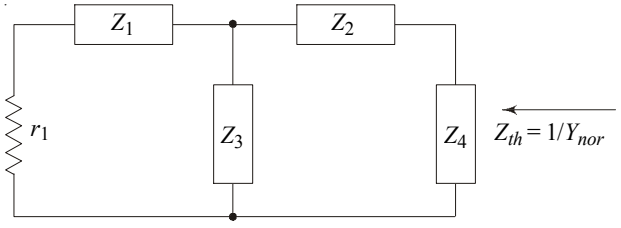


Fig. 1.21(c) Network for Norton's resistance calculation

$$Z_{in} = Z_{nor} = \{[(r + Z_1) \parallel Z_3] + Z_2\} \parallel Z_4$$

$$Y_{in} = Y_{nor} = \frac{1}{Z_{in}}$$

Norton's circuit:

The circuit reduces to a single current source in parallel with a Norton's admittance which is comes in series with the load impedance (Z_L).

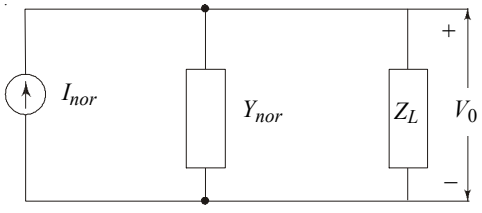


Fig. 1.21(d) Norton's network

Experiment (Norton's Theorem)

Aim: ***Verification of Norton's Theorem***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0–10)V	1
Ammeter	(0–10)mA	1
Voltmeter	(0–10)V	1

Circuit Diagram:

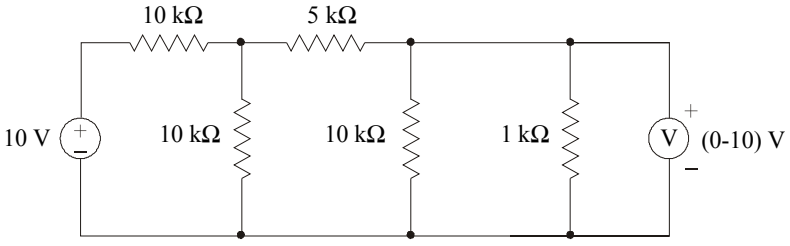


Fig. 1.22(a)

Norton's Voltage Experiment Set Up:

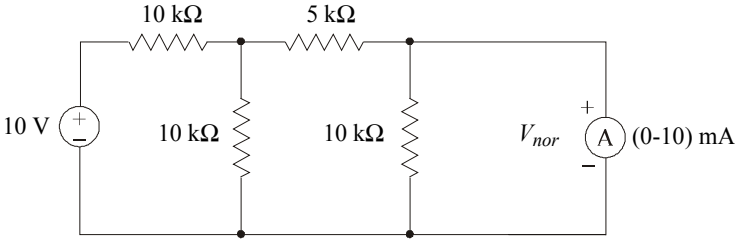


Fig. 1.22(b)

Norton's Resistance Experiment Set Up:

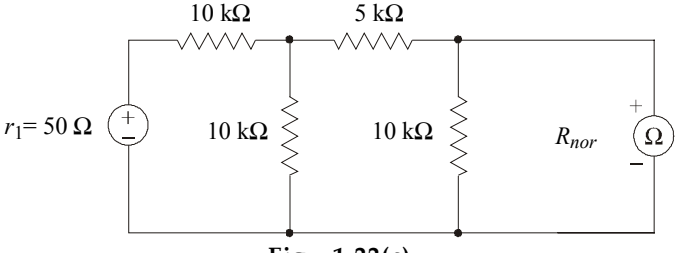


Fig. 1.22(c)

Norton's Circuit:

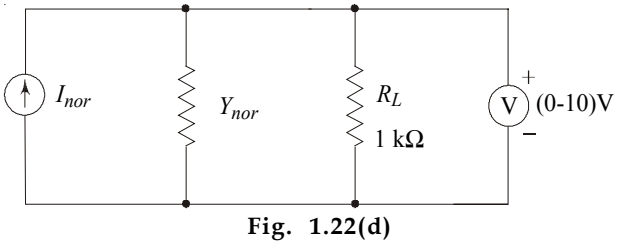


Fig. 1.22(d)

Procedure:

1. Connect the circuit as per the circuit diagram [Fig. 1.22 (a)].
2. Measure the voltage across the load using proper voltmeter.

To Find Norton's Voltage:

1. Connect the circuit as per the circuit diagram [Fig. 1.22(b)].
2. Short-circuit the load resistance and measure the short-circuited current using ammeter (I_{NO}).

To Find Norton's Resistance:

1. Connect the circuit as per the circuit diagram [Fig. 1.22(c)].
2. Replace the supply by its internal resistance and open circuit the load.
3. Using multimeter in resistance mode measure the resistance across the output terminal (R_{th}).

To Find Norton's Circuit:

1. Connect the current source (I_{nor}) and admittance (Y_{th}) in parallel as shown in the circuit diagram [Fig.1.22(d)].
2. Connect the load resistance (1k Ω).
3. Switch on the current source and measure the voltage drop across load resistance using voltmeter.
4. Voltage measured at Fig. 1.22(a) should be equal to the voltage measured at Fig. 1.22(d).

Tabular Column:

Voltage (Fig.) (Volts)	Short-Circuit Current (mA)	Norton's Resistance (Ω)	Voltage (Fig.) (Volts)

Exercise:

1. Conduct the experiment using two DC power supplies connect at any two branches.

1.13 RECIPROCITY THEOREM

Statement: *In any bilateral linear network containing one or more generators, the ratio of a voltage (V) introduced in one mesh to the current (I) in any second mesh is the same as the ratio obtained if the position of voltage and current are interchanged, other emf being removed.*

Let us consider a general network,

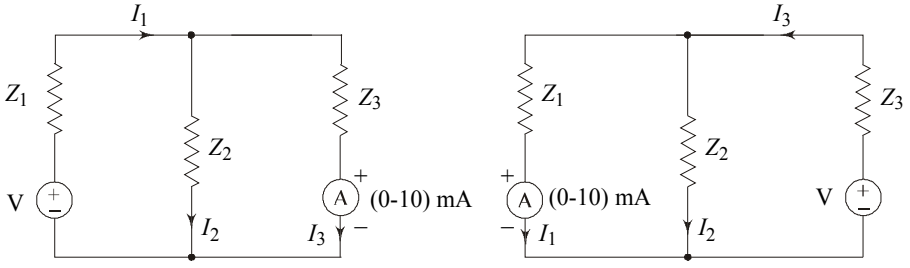


Fig. 1.23 (a) General network (b) Network with voltage and current positions is interchanged

$$\frac{V}{I_3} = \frac{V}{I_1}$$

$$I_1 = I_3 \qquad [V_1 \text{ and } V_3 \text{ are the same DC supply}]$$

Experiment (Reciprocity Theorem)

Aim: ***Verification of Reciprocity Theorem***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
Ammeter	(0-10) mA	1

Circuit Diagram:

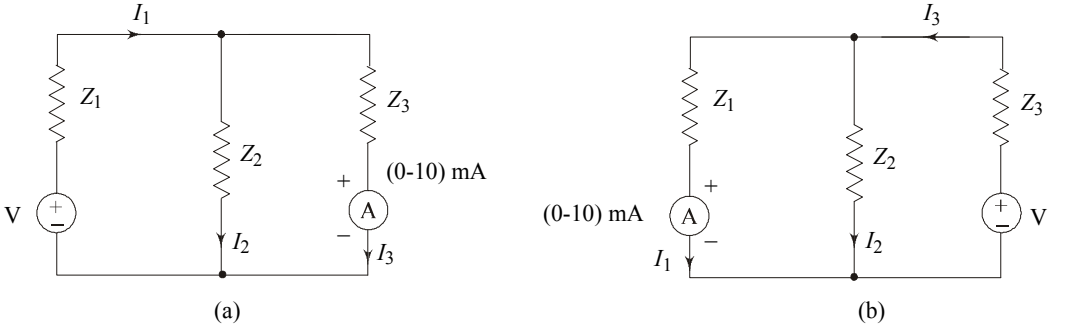


Fig. 1.24

Procedure:

1. Connect the circuit as shown in the circuit diagram [Fig.1.24(a)].
2. Switch on the supply [say V_x = 1 Volt (DC)] and note down the corresponding ammeter readings.
3. Interchange the position of ammeter and voltmeter as shown in Fig. 1.24(b).
4. Switch on the same DC supply (1Volt) and note down the reading from the ammeter.
5. Verify the reciprocity theorem by equating the voltage to current ratio of Fig. 1.24 (a) with voltage to current ratio of Fig. 1.24(b).

Exercises:

1. Verify the reciprocity theorem for AC signal (say 1 Volt, 1 kHz).
2. Verify the reciprocity theorem for the given circuit experiment and compare it with its theoretical result.

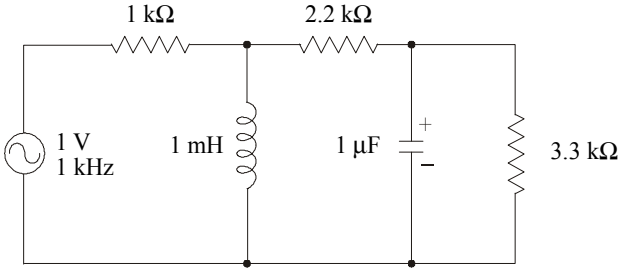


Fig. 1.25 General network

1.14 TRANSIENT RESPONSE

An equation containing one or more derived function is called differential equation. Two steps are involved in an analytical determination of the response of a physical system to given excitation.

a. Setting up of the mathematical equations that describe the system.
b. The solution of the equations.

There are two methods of solving differential equations,

1. By classical method.
2. Laplace transforms

In time domain, the voltage-current relationship for the network elements are expressed in differential equations while in frequency-domain, the current relationships for the network elements are expressed in algebraic equations. Therefore knowledge of differential equation is necessary for the analysis of linear, passive and the time-domain networks.

Consider a general first order differential equation of the nth order:

$$\alpha_0 \frac{\mathrm{d}^n i(t)}{\mathrm{d}t^n} + \alpha_1 \frac{\mathrm{d}^{n+1} i(t)}{\mathrm{d}t^{n-1}} + \cdots\cdots + \alpha_{n-1} \frac{\mathrm{d}i(t)}{\mathrm{d}t} + \alpha_n i(t) = v(t)$$

t = independent variable

i = dependent variable

(t) = forcing function (independent of $i(t)$)

When the forcing function (t) is identically zero, the equation is said to be homogeneous, otherwise the equation is non-homogeneous.

Let us consider a non-homogeneous equation,

$$\frac{\mathrm{d}i(t)}{\mathrm{d}t} + \alpha_1 \, i(t) = \alpha_2$$

where, α_1, α_2 = constants.

Multiply either sides by $e^{\alpha_1 t}$

$$\left[\frac{\mathrm{d}i(t)}{\mathrm{d}t} + \alpha_1 i(t)\right] e^{\alpha_1 t} = \alpha_2 \, e^{\alpha_1 t}$$

Therefore, $$i(t) = e^{-\alpha_1 t} \int \alpha_2 e^{\alpha_1 t} dt + C_1 \, e^{-\alpha_1 t}$$

The first term ($e^{\alpha_1 t} \int \alpha_2 \, e^{\alpha_1 t} \, \mathrm{d}t$) in the above equation is called *particular integral*, while the second term ($C_1 e^{-\alpha_1 t}$) is known as complimentary function.

For any network, α_1 will be a positive constant determined by the network parameters.

$$Lt_{t \to \infty} \, C_1 e^{-\alpha_1 t} = 0$$

Hence the value of current i as $t \to \infty$ is given by,

$$i(\infty) = Lt_{t \to \infty} \, I(t) = Lt_{t \to \infty} \, e^{\alpha_1 t} \int \alpha_2 e^{\alpha_1 t} \, \mathrm{d}t$$

The value of particular integral at $t = \infty$ is called *steady state value*. It is necessary that steady state value must not contain any exponential factor, otherwise it would reduce to zero.

The complementary function is nothing but a decaying exponential for positive real value of constant α_1, and is termed as *transient* portion of the solution.

The solution of the differential equation is often called the response. Therefore, the steady-state portion of the solution is called *steady state response*, while transient portion of the solution is called *transient response*.

The transient portion provides a smooth transition from the initial energy state of the network to the final energy state of the network by considering the initial and final values of current and voltage respectively.

Let us consider a network containing a RC series circuit.

Let the switch K be initially at position 1. In this condition, the capacitor will charge through resistor, *R*, to the maximum value of applied voltage (V).

At an instant of time, t = 0, switch K is moved from position 1 to 2.

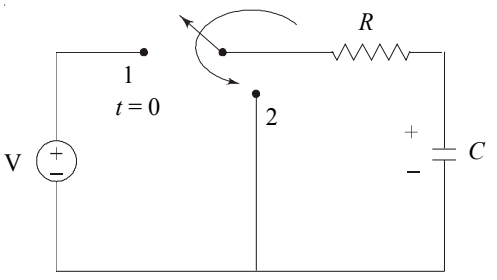


Fig 1.26

On applying KVL to the network yields,

$$\frac{1}{C}\int i\,dt + R\,i = 0 \tag{1}$$

But, $$i = \frac{dQ}{dt};\ Q = \int i\,dt$$

Therefore, $$\frac{1}{C}\,Q + R\,\frac{dQ}{dt} = 0$$

$$-\frac{1}{RC}\,dt = \frac{dQ}{dt}$$

Integrating both sides, we get

$$-\frac{t}{RC} = \log Q + C_1 \tag{2}$$

where, C_1 = constant of integration.

Let us consider one more constant in such a way that, $C_1 = \log C_2$

$$-\frac{t}{RC} = \log Q + \log C_2$$

$$-\frac{t}{RC} = \log QC_2$$

Taking anti-log on both sides,

$$e^{-t/RC} = QC_2$$

$$Q = C_3 e^{-t/RC} \left(\text{where, } C_3 = \frac{1}{C_2} \right) \tag{3}$$

Before switching $t = 0$, the charge across the capacitor C is given by,

$$Q \mid_{t=0} = CV \tag{4}$$

Substituting Equation (4) in (3) we get,

$$Q = CV_0$$

Therefore, $Q = C\ V_0 e^{-t/RC}$

Voltage across capacitor, $V_c = \frac{Q}{C} = V_0 e^{-t/RC}$

$$V_c = V_0 e^{-t/\tau}$$

Where, $\tau = RC$ (time constant)

Experiment (Transient Response)

Aim: ***To Sketch the Transient Response for the given Circuit***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0–5) V	1
Voltmeter	(0–5) V	1
Ammeter	(0–10) mA	1

Circuit Diagram:

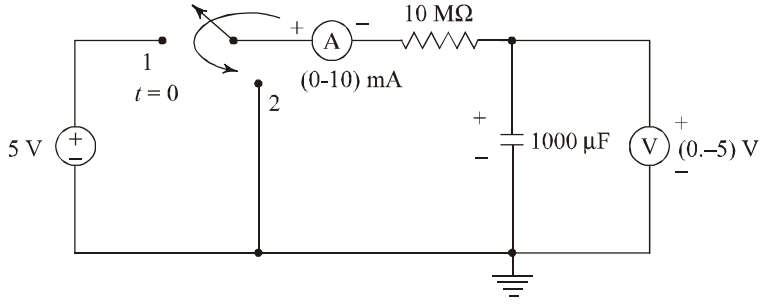


Fig. 1.27

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Switch over the contact to position 1.
3. Switch on the power supply and stopwatch simultaneously.

4. Take the ammeter and voltmeter reading in a regular time interval.
5. Switch over the contact to position 2 and simultaneously reverse the polarity of ammeter.

Note: *While reversing ammeter polarity, see to it that the capacitor is not discharged.*

6. Note down the readings from the ammeter and voltmeter at regular time intervals.
7. Plot the graph: voltage vs time (charging and discharging)
   current vs time (charging and discharging)

Tabular Column:

Charging/Discharging

Time (Sec)	Voltage (Volt)	Current (mA)

Model Graph:

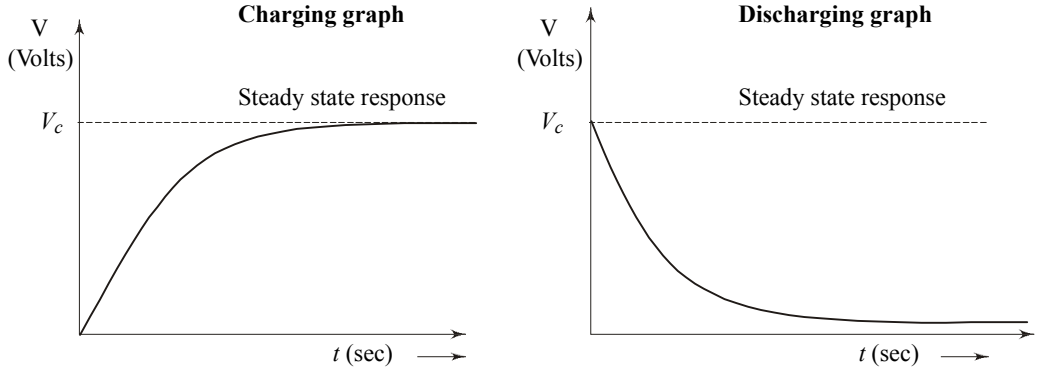


Fig. 1.27 (a) and (b)

Exercises:

1. Carry out the above procedure for *RL* and *RLC* circuit and verify your result theoretically.
2. List out some application of transients.

1.15 RESONANCE

An AC circuit is said to be in *resonance* when the applied voltage and current are in phase. Resonance circuits are formed by the combination of reactive terms (i.e., either capacitive reactance or inductive reactance) connected in either series or parallel.

In case of series resonance, the reactance of capacitance and inductance is cancelled mutually. Where- as in case of parallel resonance, the susceptance of inductance and capacitance is cancelled mutually. Such cancellation leads to operation of reactive circuits under unity power factor condition or with current and voltage in phase. These resonance circuits are also known as tuned circuits.

Power Factor Power factor is defined as the *cosine of the angle between voltage and current.* This may be leading in case of capacitive reactance and lagging in case of inductive reactance.

Power factor, $pf = \cos\phi$ (no unit)

This can also be defined as,

$$Pf = \frac{\text{resistance}}{\text{impedence}} = \frac{R}{Z}$$

If pure inductive or/and capacitive load is connected then power factor will reduce to unity as inductive reactance cancels with capacitive reactance.

Quality Factor: (Q-Factor) Quality factor can be defined as,

$$= 2\pi \frac{\text{maximum energy stored}}{\text{energy dissipated per cycle}}$$

Bandwidth **:** Bandwidth of a resonance circuit is defined as the band of frequencies on either sides of the resonance frequency. This frequency range can be obtained by dropping the graph by its half-power value, i.e., $\frac{1}{\sqrt{2}}$ times the maximum value.

$$\text{Bandwidth} = (f_2 - f_1)$$

Selectivity Selectivity is the ability to identify the frequency when it is resolved.

$$\text{Selectivity} = \text{Resonance frequency/ bandwidth}$$

$$= \frac{f_0}{(f_2 - f_1)}$$

1.15.1 Series Resonance

Let us consider a series *RLC* circuit,

The total impedance of the circuit looking from the source terminal is given by,

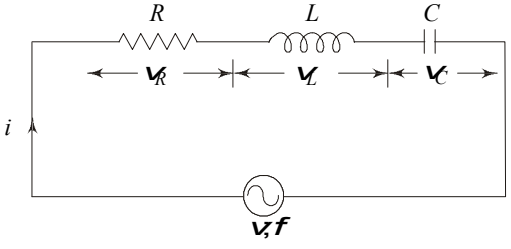


Fig. 1.28(a) Series resonance circuit

$$Z = R + j\omega L + \frac{1}{j\omega C}$$

$$Z = R + j\left(\omega L - \frac{1}{\omega C}\right)$$

$$Z = R + jX$$

A circuit is said to be an resonant if its reactive terms are zero, i.e., $X = 0$.

$$\left(\omega_0 L - \frac{1}{\omega_0 C}\right) = 0$$

$$\omega_0^2 = \frac{1}{LC}$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \text{ Hz } (\omega = 2\pi f)$$

The current at any instant in a series resonance circuit is given by,

$$i = \frac{V}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}}$$

At resonance, $i_0 = \frac{V}{R}$

Ideal Curve:

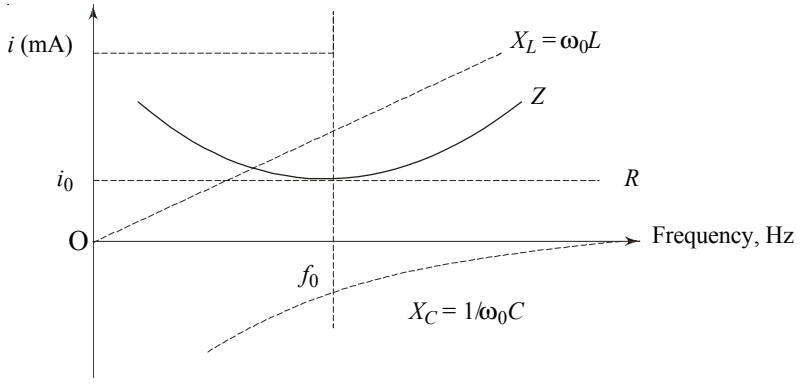


Fig. 1.28(b)

Quality Factor Let us consider the following circuits,

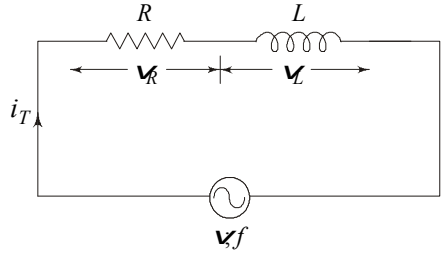


Fig. 1.28(c) RL network

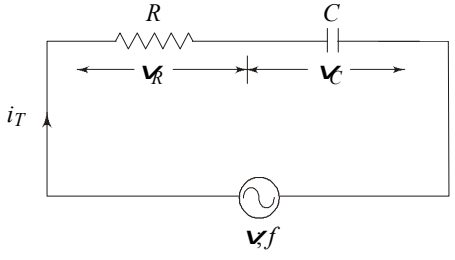


Fig. 1.28(d) RC network

For *RL* combination, [Fig. (1.31)]

$$Q = 2\pi \frac{\frac{LI_{MAX}^2}{2}}{\left(\frac{I_{MAX}}{\sqrt{2}}\right)^2 \frac{R}{f}}$$

$$Q = 2\pi f L/R$$

For RC combination, [Fig. 1.32]

$$Q = 2\pi \frac{\frac{CV_{MAX}^2}{2}}{\left(\frac{I_{MAX}}{\sqrt{2}}\right)^2 \frac{R}{f}}$$

But, $$V_{MAX} = \frac{1}{\omega C}$$

Therefore, $$Q = \frac{1}{\omega CR} = \frac{1}{2\pi fRC}$$

Since in series resonance, capacitive reactance is equal to inductive reactance ($X_C = X_L$), the Q-factor of a series resonance circuit is defined as the ratio of the voltage across inductor or capacitor to the applied voltage.

Therefore, $$Q_0 = \frac{\omega L}{R} = \frac{1}{\omega CR}$$

$$Q_0 = \frac{1}{R}\sqrt{\frac{L}{C}}$$

Experiment (Series Resonance)

Aim: ***To Plot the Resonance Curve for a Series Resonance***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0 -1) MHz	1
Voltmeter	(0 -10) V	3
Ammeter	(0 -10) mA	1

Circuit Diagram:

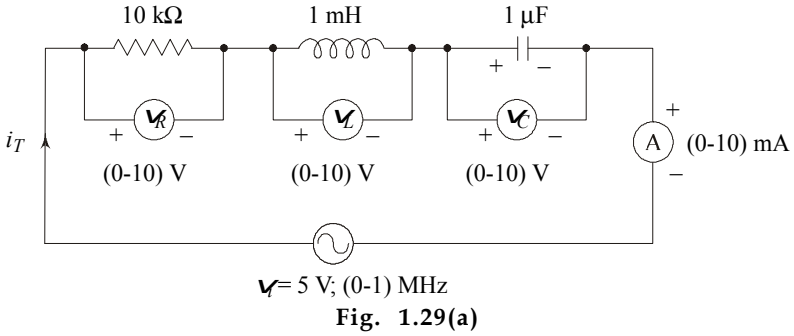


Fig. 1.29(a)

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input voltage, v_i = 5V using signal generator and vary the frequency from (0-1) MHz in regular steps.
3. Note down the corresponding output voltage and current.
4. Plot the following graph:
   (a) Current v/s frequencies
   (b) Voltage v/s frequencies

To Measure the Resonance Frequency:

1. Plot the graph: Current v/s frequencies.
2. Draw a horizontal line, which intersects the curve at $\frac{1}{\sqrt{2}}$ times the maximum current reading.
3. Lower intersected point and upper intersected point are respectively called lower cut-off frequency and upper cut-off frequency on frequency axis.

Bandwidth:

Bandwidth of a series resonance circuit is defined as the difference between the upper and lower half-power frequencies. It is normally denoted as *Bandwidth.*

The bandwidth is given by,

$$\text{Bandwidth} = (f_2 - f_1)$$

$$\text{Bandwidth} = \frac{\omega_0}{Q}$$

Where, $\omega_n = \sqrt{\omega_1 \omega_2}$

Q = Quality factor.

Selectivity:

$$\text{Selectivity} = \frac{\Delta\omega}{\omega_0} \cdots\cdots\cdots (\Delta f = f_2 - f_1)$$

$$\text{Selectivity} = \frac{R}{\omega_0 L}$$

But $Q\text{-factor} = \frac{\omega_0 L}{R}$

Therefore, $\text{selectivity} = \frac{1}{Q_0}$

Model Graph:

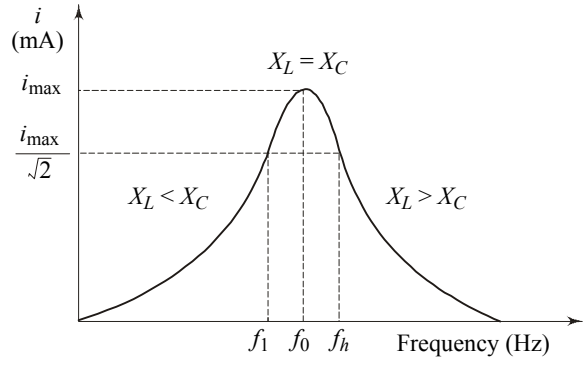


Fig. 1.29(b)

Tabulation: v_i = 5V

Frequency (Hz)	Output circuit (mA)

1.15.2 Parallel Resonance

A parallel AC circuit is said to be in resonance when its susceptance is zero. At parallel resonance, the applied voltage and resulting current will be in phase.

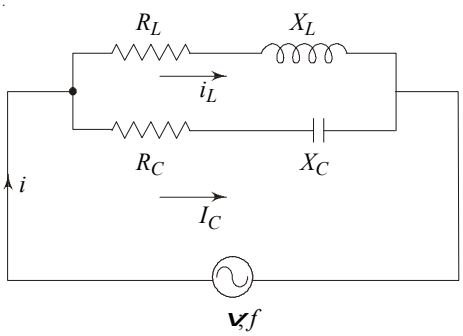


Fig. 1.30(a)

Let us consider a general parallel circuit,

Inductive admittance, $Y_L = \dfrac{1}{Z_L} = \dfrac{1}{(R_L + jX_L)}$

Divide and multiply by its conjugate $(R_L - jX_L)$

$$Y_L = \left[\frac{R_L - jX_L}{R_L^2 + X_L^2}\right]$$

Similarly, capacitive admittance, $Y_C = \dfrac{1}{Z_C} = \dfrac{1}{(R_L + jX_C)}$

Divide and multiply by its conjugate $(R_L + jX_C)$

$$Y_C = \left[\frac{R_C - jX_C}{R_C^2 + X_C^2}\right]$$

Total admittance, $Y_T = Y_L + Y_C$

$$Y_T = \left[\frac{R_L - jX_L}{R_L^2 + X_L^2}\right] + \left[\frac{R_C + jX_C}{R_C^2 + X_C^2}\right]$$

$$Y_T = \left[\frac{R_L}{R_L^2 + X_L^2}\right] + \left[\frac{R_C}{R_C^2 + X_C^2}\right] + \left[\frac{-jX_L}{R_L^2 + X_L^2}\right] + \left[\frac{jX_c}{R_C^2 + X_C^2}\right]$$

At resonance, susceptance = 0

$$\left[\frac{-jX_L}{R_L^2 + X_L^2}\right] + \left[\frac{jX_c}{R_C^2 + X_C^2}\right] = 0$$

$$X_L = \omega_0 L;\ X_C = \frac{1}{\omega_0 C};\ \omega_0 = 2\pi f_0$$

Therefore, $$\omega_0 = \frac{1}{\sqrt{LC}}\sqrt{\frac{\frac{L}{C} - R_L^2}{\frac{L}{C} - R_C^2}}$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{\frac{L}{C} - R_L^2}{\frac{L}{C} - R_C^2}}$$

Current at resonance, $i_0 = Y_0$

$$i_0 = \left\{\left[\frac{R_L}{R_L^2 + X_L^2}\right] + \left[\frac{R_C}{R_C^2 + X_C^2}\right]\right\}$$

Quality Factor

$$Q_0 = \frac{\text{resistance}}{\text{reactance}} = \frac{R}{w_0 L} = R\sqrt{\frac{C}{L}}$$

Bandwidth and Selectivity In parallel resonance circuit, the specified points are the one at which impedance falls to $1/\sqrt{2}$ of its value at resonance.

Bandwidth, $BW = f_2 - f_1$

Selectivity = Bandwidth/f_0

$= (f_2 - f_1)/f_0$

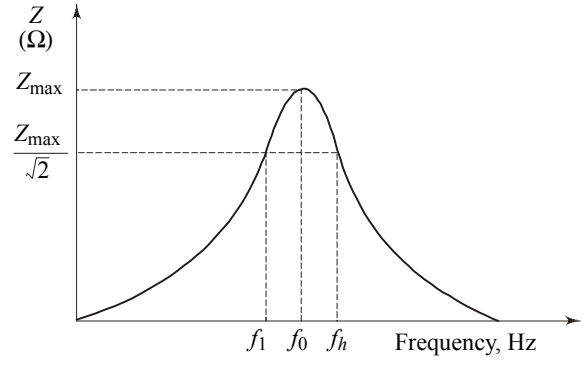


Fig. 1.30(b)

Experiment (Parallel Resonance)

Aim: ***To Plot the Resonance Curve for a Parallel Resonance***

Equipment Required:

Equipment	Range	Quantity
Signal generator Voltmeter Ammeter	(0-1) MHz	1

Circuit Diagram:

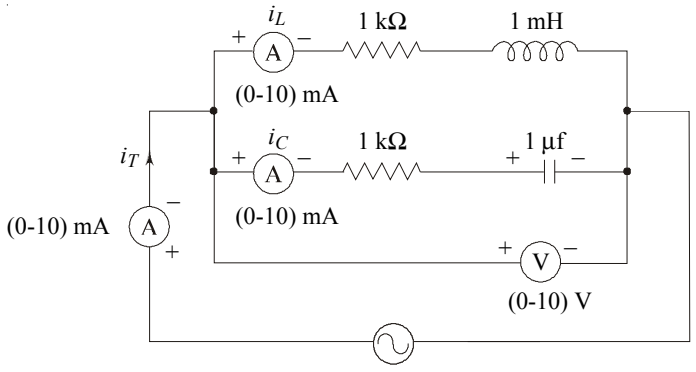


Fig. 1.31(a)

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input voltage, V_i = 5V using signal generator and vary the frequency from (0-1) MHz in regular steps.
3. Note down the corresponding output voltage and current.
4. Plot the graph: impedance (Z) vs frequencies.

To Measure the Resonance Frequency:

1. Plot the graph: impedance (Z) vs frequencies.
2. Draw a horizontal line, which intersects the curve at $\frac{1}{\sqrt{2}}$ times the maximum impedance reading.
3. Lower intersected point and upper intersected point are respectively called lower cut-off frequency and upper cut-off frequency on frequency axis.

Quality Factor:

$$Q_0 = \frac{\text{resistance}}{\text{reactance}} = \frac{R}{\omega_0 L} = R\sqrt{\frac{C}{L}}$$

Bandwidth and Selectivity:

Bandwidth, $BW = f_2 - f_1$

Selectivity = Bandwidth/f_0 = $(f_2 - f_1)/f_0$

Model Graph:

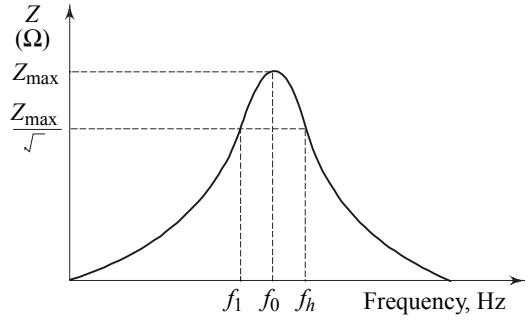


Fig 1.31(b)

Tabulation: v_i = 5V

Frequency (Hz)	Current (mA)	$Z = \frac{V_i}{i}$ (Ω)

1.16 DIFFERENTIATOR

A differentiator is a simple *RC* network. If the time constant (*RC*) is very small ($RC << \tau$) in comparison with the time required for the input signal to make an appropriate change, the circuit is called a *Differentiator.*

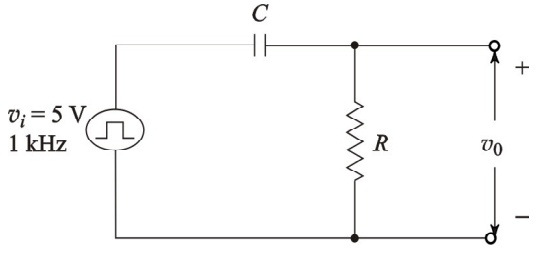


Fig. 1.32(a) Differentiator circuit

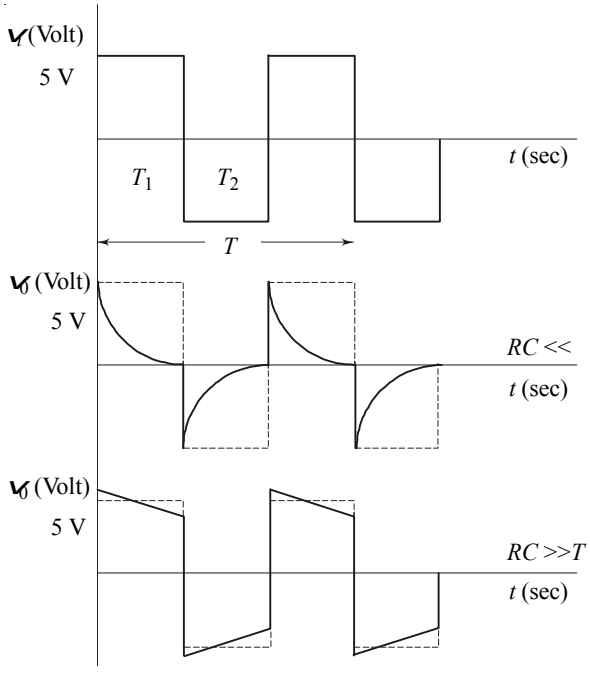


Fig 1.32 (b), (c), (d) Differentiator waveform at different time constants

The voltage drop across *R* will be very small in comparison to the drop across capacitor, *C*. So the current is determined entirely by the capacitor. Therefore, the output voltage is given by,

$$i = C\frac{dv}{dt}$$

$$v_0 = i\,R = C\frac{dv}{dt}\,R = RC\frac{dv}{dt}$$

The pulse amplitude is V and the duration t_p, if the pulse is applied, the response for times less than t_p is the same as that for the step voltage input. Hence the output at $t = t_p$ is given by $v_0 = Ve^{(-t_p/RC)} = V_p$. At the end of the pulse, the input falls abruptly by the amount V, and since the capacitor voltage cannot change instantaneously, the output must also drop by amount V.

Experiment (Differentiator)

Aim: ***To Study the given Differentiator at Defferent Time-Constant***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1

Circuit Diagram:

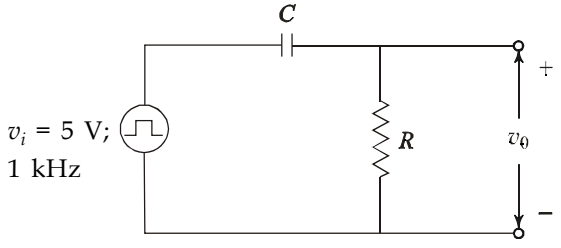


Fig. 1.33(a)

Design:

For $T = \tau$; $f = 1$ kHz; $T = \frac{1}{f} = 1$ msec

$\tau = RC = 1 \times 10^{-3}$

If, $C = 0.1$ μF, then $R = \frac{\tau}{C} = 10$ kΩ

For $T < \tau$, then $R > \frac{\tau}{C} > 10$ kΩ

For $T > \tau$, then $R < \frac{\tau}{C} < 10$ kΩ

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input voltage, v_i = 5V using signal generator and vary the frequency from (0-1) MHz in a regular steps.
3. Observe the output waveform using *CRO*.
4. Change the value of R as per the design and observe the output waveform using *CRO*.

Model Waveform:

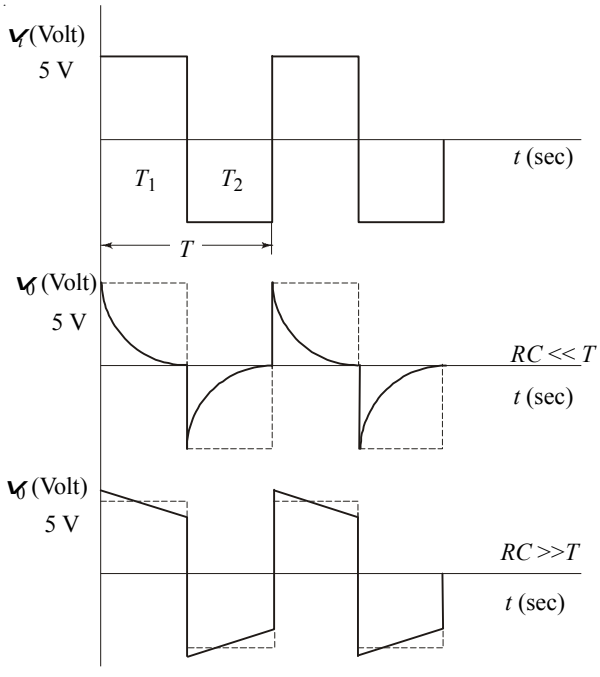


Fig. 1.33(b), (c)

1.17 INTEGRATOR

An integrator is a simple *RC* network. If the time constant (*RC*) is very large ($RC >> \tau$) in comparison with the time required for the input signal to make an appropriate change, the circuit is called an *integrator*.

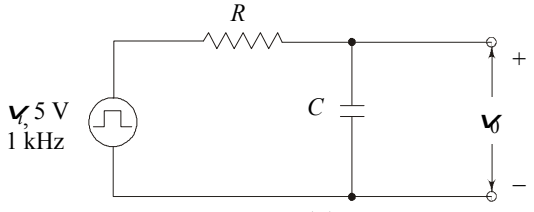


Fig 1.34(a)

The voltage drop across capacitor, *C* will be very small in comparison to the drop across resistor, *R*. So the current is determined entirely by the resistor, *R*. Therefore, the output voltage is given by,

$$i = v_i R$$

$$v_0 = \left(\frac{1}{C}\int i\,dt\right) R = \frac{1}{RC}\int i\,dt$$

Since capacitor voltage cannot change instantaneously, the output starts from zero and rises towards the steady-state value, *V*.

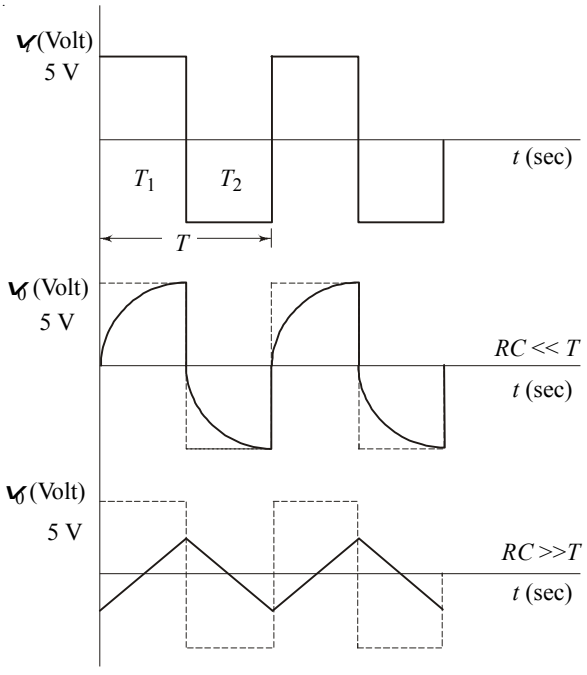


Fig. 1.34(b), (c), (d)

Therefore, $v_0 = V\left(1 - e^{\left(-t_p/RC\right)}\right)$

Experiment (Integrator)

Aim: ***To Study the given Integrator at different Time-Constant***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1

Circuit Diagram:

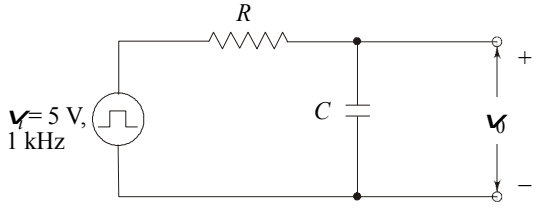


Fig 1.35(a)

Design:

For $T = \tau$; $f = 1$ kHz; $T = \dfrac{1}{f} = 1$ mSec

$\tau = RC = 1 \times 10^{-3}$

If, $C = 0.1\ \mu F$, then $R = \frac{\tau}{C} = 10\ k\Omega$

For $T < \tau$, then $R > \frac{\tau}{C} > 10\ k\Omega$

For $T > \tau$, then $R < \frac{\tau}{C} < 10\ k\Omega$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input voltage, v_i = 5V using signal generator and vary the frequency from (0-1) MHz in a regular steps.
3. Observe the output waveform using *CRO*.
4. Change the value of *R* as per the design and observe the output waveform using *CRO*.

Model Waveform:

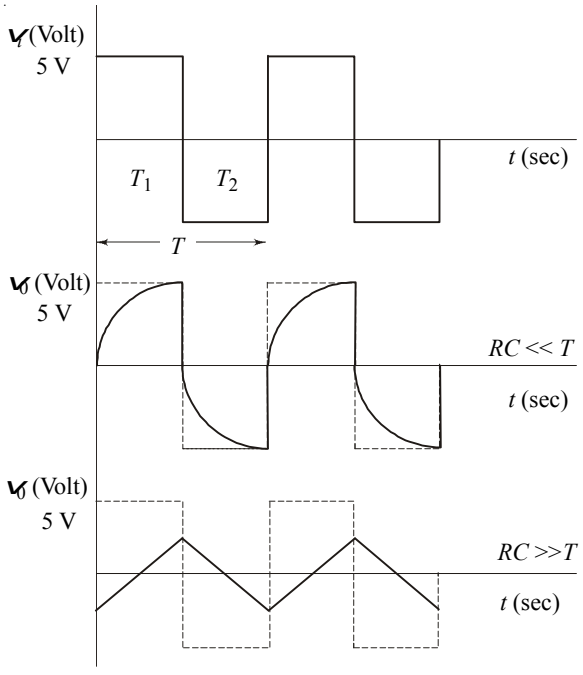


Fig. 1.35 (b) (c)

1.18 PASSIVE FILTERS

G.A. Campbell and O.I. Lobel of the Bell Telephone Laboratories invented wave filters. A filter is a reactive network, which passes the desired frequencies only. Ideally, filters should produce no attenuation in the desired band, called *pass band,* and should attenuate fully in other frequency region, called *attenuation band*. The frequency, which separates the pass band and attenuation band, is termed as *cut-off frequency* of the wave filter (f_c).

Filter finds its application in many fields like data communication, instrumentation, signal processing, etc.

Filters are broadly divided into 4 groups:

1. Low pass filter (LPF)

2. High pass filter (HPF)
3. Band pass filter (BPF)
4. Band elimination filter (BEF)

Low Pass Filter A LPF is one, which passes all frequencies up to its designed/desired cut-off frequency, f_c and attenuate all other frequencies greater than cut-off frequency.

Ideal Waveform:

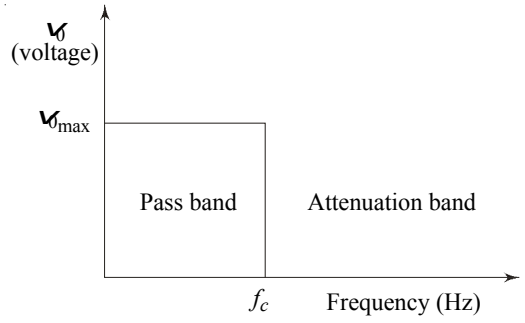


Fig 1.36(a) Ideal low pass filter

High Pass Filter A HPF is one, which passes all frequencies above designed/desired cut-off frequency, f_c and attenuates all other frequencies below cut-off frequency.

Ideal Waveform:

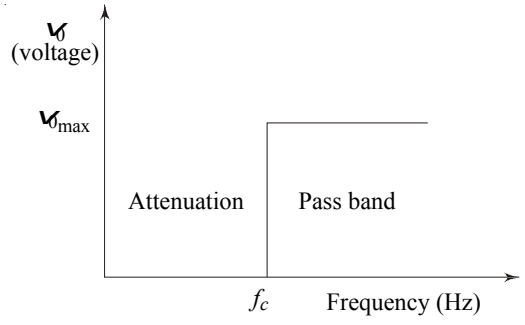


Fig. 1.36(b) Ideal high pass filter

Band Pass Filter A BPF is one which *passes* frequencies between two designed/desired cut-off frequencies (f_l = lower cut-off frequency, f_h = upper cut-off frequency) and attenuates all other frequencies.

Ideal Waveform:

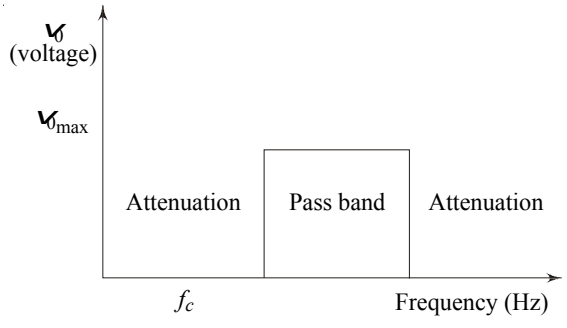


Fig. 1.36(c) Ideal band pass filter

Band Elimination Filter A BEF is one which *attenuates* frequencies between two designed/ desired cut-off frequencies (f_l = lower cut-off frequency, f_h = upper cut-off frequency) and passes all other frequencies.

Ideal Waveform:

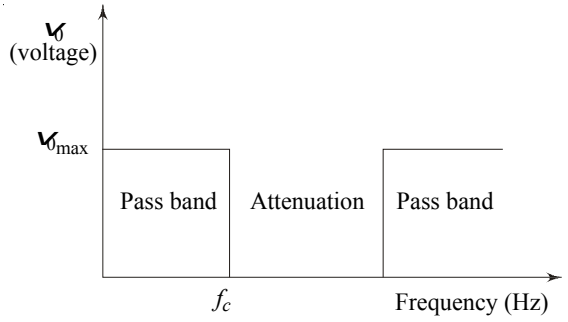


Fig. 1.36(d) Ideal band elimination filter

Filters are made of symmetrical *T* or *L* or π (network. A study of any filter requires following parameters.

1. Propagation constant, γ
2. Attenuation constant, α
3. Phase constant, β
4. Characteristic impedance, Z_0

Propagation constant, $\gamma = \alpha + j\beta$

T-Network Proto-Type The value of input impedance for the T-network when it is terminated in Z_0 is given by,

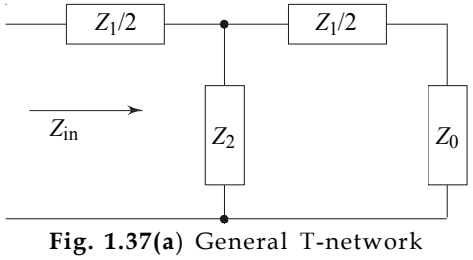


Fig. 1.37(a) General T-network

$$Z_{in} = \frac{Z_1}{2} + \left[Z_2 || \left(\frac{Z_1}{2} + Z_0 \right) \right]$$

For proper termination, $Z_{in} = Z_0$.

On simplification, the characteristic impedance, Z_0 for T-network is given by,

$$Z_{0T} = \sqrt{\frac{Z_1^2}{4} + Z_1 Z_2}$$

Short-circuited impedance (short the load impedance, Z_0) is given by,

$$Z_{sc} = \frac{Z_1}{2} + \left[Z_2 \,||\, \frac{Z_1}{2} \right]$$

Open-circuited impedance (open the load impedance, Z_0) is given by,

$$Z_{oc} = \left(\frac{Z_1}{2} + Z_2\right)$$

$$Z_{0T} = \sqrt{Z_{oc} Z_{sc}}$$

Propagation Constant, $\gamma = \log_e(I_1/I_2)$

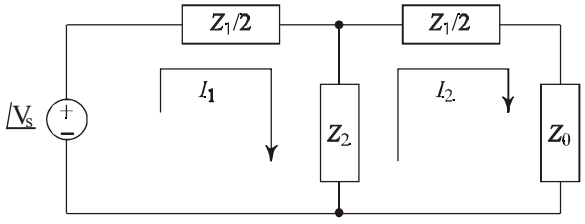


Fig. 1.37(b) Network to calculate propagation constant

Taking the mesh equation for the second mesh, we get,

$$(I_2 - I_1)\, Z_2 + I_2 \frac{Z_1}{2} + I_2\, Z_0 = 0$$

On simplification,

$$(I_1/I_2) = e^{\gamma} = \frac{Z_2 + \frac{Z_1}{2} + Z_0}{Z_2} \tag{1}$$

But we know that, $Z_{0T} = \sqrt{\frac{Z_1^2}{4} + Z_1 Z_2}$ (2)

Squaring equations (1) and (2), and subtracting equation (2) from (1), we get

$$e^{\gamma} + e^{-\gamma} - 2 = \frac{Z_1}{Z_2}$$

Dividing both sides by 2, we get

$$\text{Cosh } \gamma = 1 + \frac{Z_1}{2Z_2}$$

$$\tan \gamma = \sinh \gamma / \text{Cosh } \gamma \quad \left(\text{But}, \sinh \gamma = \sqrt{\cosh^2} - 1\right)$$

Therefore, $$\tan \gamma = \frac{Z_{0T}}{\left(Z_2 + \frac{Z_1}{2}\right)} \tag{3}$$

But, $$Z_{oc} = \left(\frac{Z_1}{2} + Z_2\right) \tag{4}$$

$$Z_{0T} = \sqrt{Z_{oc} Z_{sc}} \tag{5}$$

On manipulating equation (4) and (5) in (3), we get

$$\tan \gamma = \sqrt{\frac{Z_{SC}}{Z_{OC}}}$$

π-Network Proto Type:

$$Z_{in} = [(Z_0 \parallel 2Z_2) + Z_1] \parallel 2Z_2$$

On simplification, we get

$$Z_{0\pi} = \sqrt{\frac{Z_1 Z_2}{1 + \frac{Z_1}{4Z_2}}}$$

$$Z_{0\pi} = \frac{Z_1 Z_2}{\sqrt{Z_1 Z_2 + \frac{Z_1^2}{4}}}$$

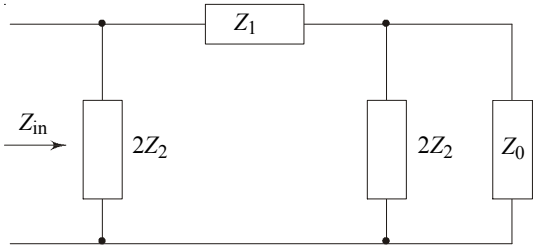


Fig. 1.38 General π-network

$$Z_{0\pi} = \frac{Z_1 Z_2}{Z_{0T}}$$

$$Z_{oc} = [2Z_2 + Z_1] \parallel 2Z_2$$

$$Z_{sc} = Z_1 \parallel 2Z_2$$

$$Z_{0\pi} = \sqrt{Z_{oc} Z_{sc}}$$

The propagation constant of a symmetrical π-section is the same as that for a symmetrical T-section.

$$\text{Cosh } \gamma = 1 + \frac{Z_1}{2Z_2}$$

1.18.1 Constant-k Low Pass Filter

The propagation constant of a complex function, $\gamma = \alpha + j\beta$,

where, attenuation constant, α = real part of the complex propagation constant and phase shift constant, β = imaginary part of the complex propagation constant.

1. when $\alpha = 0$:

The condition of pass band of zero attenuation is,

$$\beta = 2 \sin^{-1} \sqrt{\frac{Z_1}{4Z_2}} \quad \cdots\cdots\cdots - 1 \le \frac{Z_1}{4Z_2} \le 0$$

Therefore, $$\beta = 2 \sin^{-1} \left(\frac{f}{f_C} \right); \alpha = 0.$$

2. when $\beta = \pi$:

The condition of stop band is,

$$\alpha = 2 \cosh^{-1} \sqrt{\frac{Z_1}{4Z_2}} \cdots\cdots\cdots \alpha \leq \frac{Z_1}{4Z_2} \leq -1$$

Therefore, $$\alpha = 2 \cosh^{-1} \left(\frac{f}{f_C} \right); \beta = \pi.$$

Ideal Plots: (Propagation Parametrs) The characteristic impedance can be calculated by

$$Z_{0T} = Rk \sqrt{1 - \left(\frac{f}{f_C} \right)^2}$$

Z_{0T} = real, when $f < f_c$ (in pass band)

$Z_{0T} = 0$, when $f = f_c$

Z_{0T} = imaginary, when $f > f_c$ (in attenuation band, rising to ∞ reactance at infinite frequency)

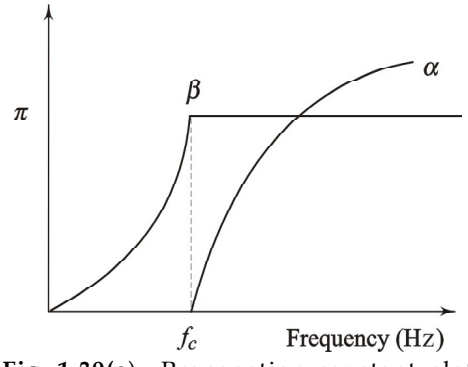


Fig. 1.39(a) Propagation constant plot

Ideal Plot: (Characteristic Impedance) The characteristic impedance of the π-network is given by

$$Z_{0\pi} = \frac{R_k}{\sqrt{1 - \left(\frac{f}{f_C} \right)^2}}$$

At cut-off frequency, $Z_1 = -4Z_2$

$$j\omega_c L = \frac{-4}{j\omega_c C}$$

$$\pi^2 f_c^2 \; LC = 1$$

We know that, $$R_k = \sqrt{\frac{L}{C}}$$

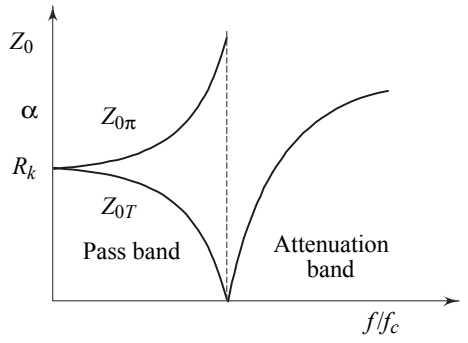


Fig. 1.39(c) Characteristic impedance plot

Therefore, $$C = \frac{1}{\pi f_C R_K} \text{ (shunt capacitor)}$$

$$L = \frac{R_k}{\pi f_C} \text{ (series inductor)}$$

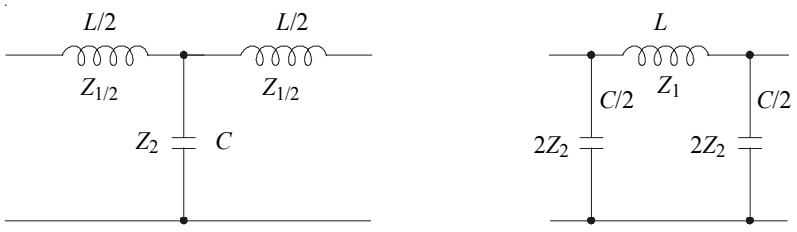


Fig. 1.39 (c) and (d) T-type and π-type network

Experiment (Constant-k LPF)

Aim: ***To Design and Test a Constant–k LPF and Measure Its Cut-Off Frequency***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1

Circuit Diagram:

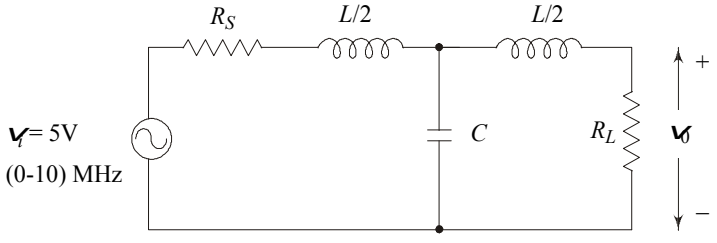


Fig. 1.40(a)

Design:

Given $R_L = 680\ \Omega$, $f_c = 2$kHz,

$R_S = 680\ \Omega$ $R_L = R_S = R_k$.

$$C = \frac{1}{\pi f_C R_k} \text{ (shunt capacitor)}$$

$$L = \frac{R_k}{\pi f_C} \text{ (series inductor)}$$

Procedure:

1. Rig up the circuit as per the circuit diagram.

2. Set input voltage, v_i = 5V using signal generator and vary the frequency from (0-1)MHz in regular steps.
3. Note down the corresponding output voltage.
4. Plot the following graph:
   (a) Output voltage v/s frequencies
   (b) Attenuation factor (α) vs frequencies
   (c) Phase angle (β) vs frequencies
   (d) Characteristic impedance (Z_0) vs frequencies (f/f_c)

Tabular Column:

Frequency (Hz)	Output Voltage (Volts)	α	β	Z_0

Model Graph:

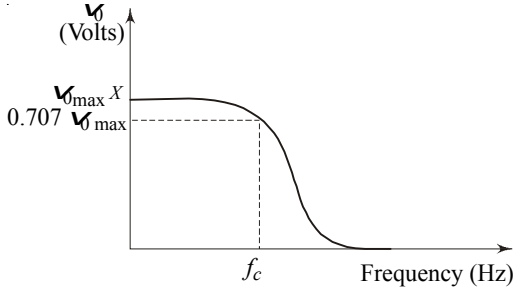


Fig. 1.40(b) Frequency response plot

Result:

	Theoretical	Practical
Cut-Off Frequency		

Exercises:

Design a π-section constant-k LPF and compare the result with T-section constant-k LPF.

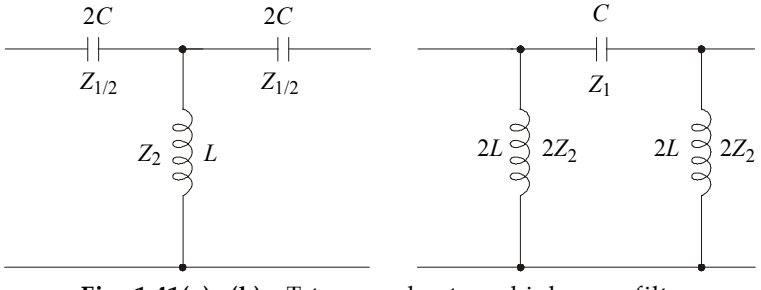


Fig. 1.41(a), (b) T-type and π-type high pass filter

1.18.2 Constant-k High Pass Filter

$$Z_1 Z_2 = \sqrt{\frac{L}{C}} = R_k$$

Cut-off frequency is given by, $Z_1 = -4Z_2$

Therefore, $$f_c = \frac{1}{4\pi\sqrt{LC}}$$

The pass band is given by,

$$\beta = 2 \sin^{-1}\left(\frac{f_C}{f}\right);\ \alpha = 0.$$

The attenuation factor is given by,

$$\alpha = 2 \cosh^{-1}\left(\frac{f_C}{f}\right);\ \beta = \pi.$$

Ideal Plot: (Propagation Parameter) The characteristic impedance can be calculated,

$$Z_{0T} = R_k \sqrt{1 - \left(\frac{f_C}{f}\right)^2}$$

$$Z_{0\pi} = \frac{R_k}{\sqrt{1 - \left(\frac{f_C}{f}\right)^2}}$$

Therefore, $$C = \frac{1}{2\pi f_C R_k}$$ (shunt capacitor)

$$L = \frac{R_k}{4\pi f_C}$$ (series inductor)

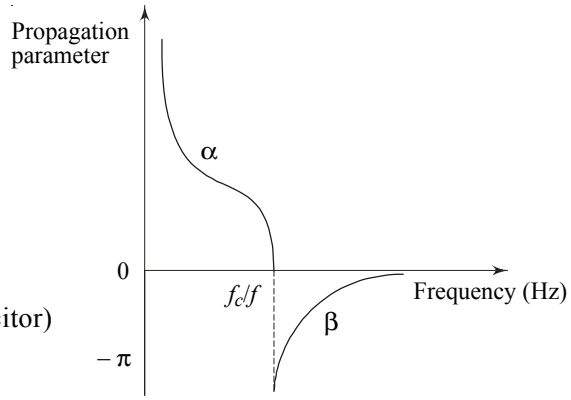


Fig. 1.41(c) Propagation constant plot

Ideal Plot: (Characteristic Impedance)

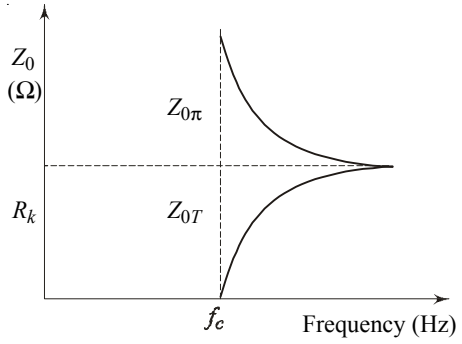


Fig. 1.41(d) Ideal characteristic impedance plot

Experiment (Constant-k HPF)

Aim: ***To Design and Test a Constant–k HPF and Measure Its Cut-Off Frequency***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1

Circuit Diagram:

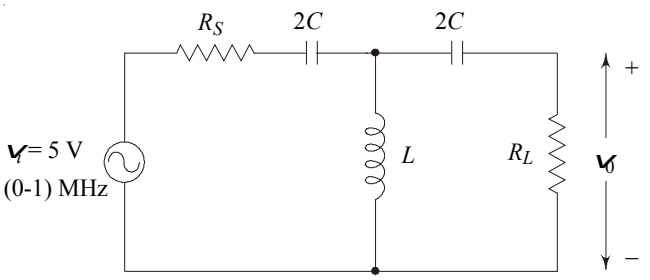


Fig. 1.42(a)

Design:

Given $R_L = 680\ \Omega, f_c = 2\text{kHz}, R_S = 680\ \Omega$

$R_L = R_S = R_k.$

$$C = \frac{1}{2\pi f_C R_k} \text{ (shunt capacitor)}$$

$$L = \frac{R_k}{4\pi f_C} \text{ (series inductor)}$$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input voltage, v_i = 5V using signal generator and vary the frequency from (0-1) MHz in regular steps.
3. Note down the corresponding output voltage.
4. Plot the following graph:
   (a) Output voltage vs frequencies
   (b) Attenuation factor (α) vs frequencies
   (c) Phase angle (β) vs frequencies
   (d) Characteristic impedance (Z_0) vs frequencies (f/f_c)

Tabular Column:

Frequency (Hz)	Output Voltage (Volts)	α	β	Z_0

Model Graph:

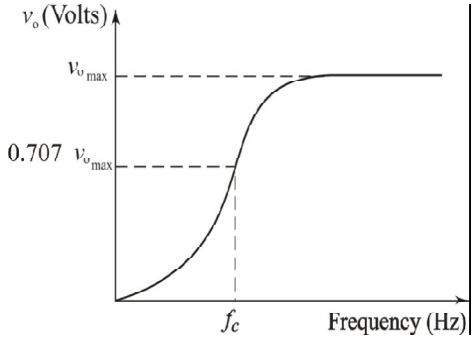


Fig. 1.42 (b)

Result:

	Theoretical	Practical
Cut-Off Frequency		

Exercises:

Design a π-section constant-k HPF and compare the result with T-section constant-k HPF.

1.18.3 Constant-k Band Pass Filter

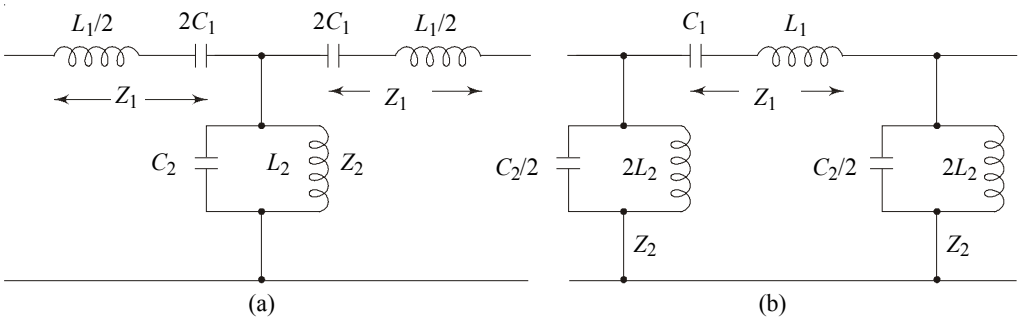


Fig. 1.43(a), (b) T-type and π-type band pass filter

Resonance condition for the series arm is,

$$\frac{\omega_0 L_1}{2} = \frac{1}{2\omega_0 C_1}$$

Therefore, $\omega_0^2 L_1 C_1 = 1$ (1)

Resonance condition for the shunt arm is,

$$\omega_0 L_2 = \frac{1}{\omega_0 C_1}$$

Therefore, $\omega_0^2 L_2 C_2 = 1$ (2)

From equation (1) and (2), we get,

$$\omega_0^2 L_1 C_1 = \omega_0^2 L_2 C_2$$

Therefore, $L_1 C_1 = L_2 C_2$

$$Z_1 = \left(j\omega L_1 - j\frac{1}{\omega C_1} \right) = j\left(\frac{\omega^2 L_1 C_1 - 1}{\omega C_1} \right)$$

$$Z_2 = \frac{(j\omega L_2)\left(\frac{j}{\omega C_2} \right)}{\left(j\omega L_2 + \frac{1}{j\omega C_2} \right)} = \frac{j\omega L_2}{\left(1 - \omega^2 L_2 C_2\right)}$$

But, $L_1 C_1 = L_2 C_2$

Therefore, $Z_1 Z_2 = \frac{L_2}{C_1} = \frac{L_1}{C_2} = R_k^2$

At cut-off frequency,

$$Z_1 = -4Z_2$$

Therefore, $Z_1^2 = -4\ Z_1 Z_2 = -4R_k^2$

$$Z_1 = \pm j2R_k$$

i.e., the value of Z_1 at lower cut-off frequency is equal to the negative of the value of Z_1 at the upper cut-off frequency,

$$\left(j\omega_1 L_1 + j\frac{1}{\omega_1 C_1} \right) = -\left(j\omega_2 L_1 + j\frac{1}{\omega_2 C_1} \right)$$

Substitute, $L_1 C_1 = \frac{1}{\omega_0^2}$ in above equation and simplify,

$$\left(1 - \frac{\omega_1^2}{\omega_0^2} \right) = \left(\frac{\omega_1}{\omega_2} \right)\left(\frac{\omega_2^2}{\omega_0^2} - 1 \right)$$

On simplification, $\omega_0^2 = \omega_1\, \omega_2$, $f_0 = \sqrt{f_1 f_2}$

Design:

If the filter is terminated in a load, $R_L = R_k$, then at the lower cut-off frequency,

$$Z_1 = -2jR_k$$

$$\left(j\omega_1 L_1 + j\frac{1}{\omega_1 C_1} \right) = -2jR_k$$

Substitute, $L_1 C_1 = \frac{1}{\omega_0^2}$ in above equation and simplify,

$$\left(1 - \frac{\omega_1^2}{\omega_0^2} \right) = 2R_k \omega_1 C_1$$

but $f_1 f_2 = f_0^2$,

therefore, $f_2 - f_1 = 4\pi R_k C_1$

$$C_1 = \frac{(f_2 - f_1)}{4\pi R_k f_1 f_2}$$

$$L_1 = \frac{1}{\omega_0^2 C_1}$$

Substitute the value of C_1 in the above equation, we get,

$$L_1 = 4\pi R_k f_1 f_2/\omega_0^2 (f_2 - f_1)$$

$$L_1 = \frac{R_k}{\pi (f_2 - f_1)}$$

To evaluate the values for the shunt arm, consider the equations,

$$Z_1 Z_2 = \frac{L_2}{C_1} = \frac{L_1}{C_2} = R_k^2$$

$$L_2 = C_2 R_k^2 = \frac{R_k (f_2 - f_1)}{4\pi f_1 f_2}$$

$$C_2 = L_1/R_k^2 = \frac{1}{\pi R_k (f_2 - f_1)}$$

Model Plot: (Propagation/Attenuation Parameter)

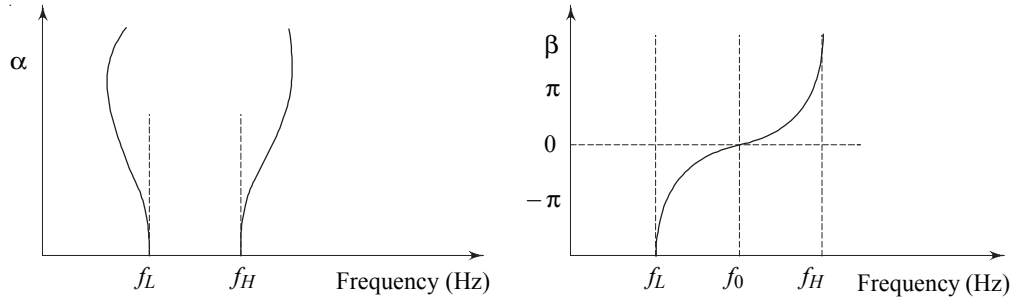


Fig. 1.43 (c), (d) Propagation constant and characteristic impedance plot

Experiment (Constant-k Band Pass Filter)

Aim: ***To Design and Test a Constant–k BPF and Measure Its Cut-Off Frequencies***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1

Circuit Diagram:

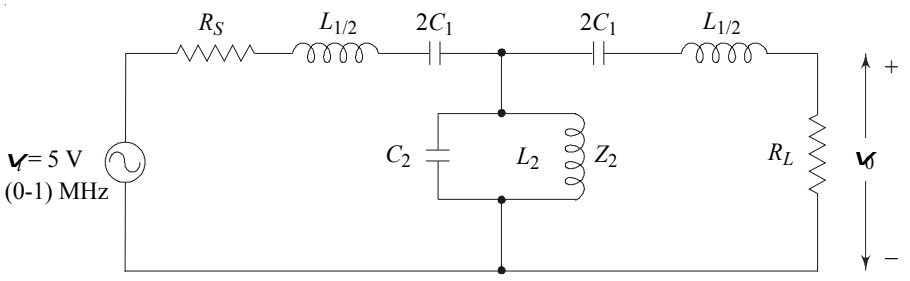


Fig. 1.43(e)

Design:

To evaluate the values for the series arm, consider the equations,

$$C_1 = \frac{(f_2 - f_1)}{4\pi R_k f_1 f_2}$$

$$L_1 = \frac{R_k}{\pi (f_2 - f_1)}$$

To evaluate the values for the shunt arm, consider the equations,

$$L_2 = \frac{R_k (f_2 - f_1)}{4\pi f_1 f_2}$$

$$C_2 = \frac{1}{\pi R_k (f_2 - f_1)}$$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input voltage, v_i = 5V using signal generator and vary the frequency from (0-1) MHz in regular steps.
3. Note down the corresponding output voltage.
4. Plot the following graph:
   (a) Output voltage vs frequencies
   (b) Attenuation factor (α) v/s frequencies
   (c) Phase angle (β) vs frequencies
   (d) Characteristic impedance (Z_0) vs frequencies (f/f_c)

Tabular Column:

Frequency (Hz)	Output Voltage (Volts)	α	β	Z_0

Model Graph:

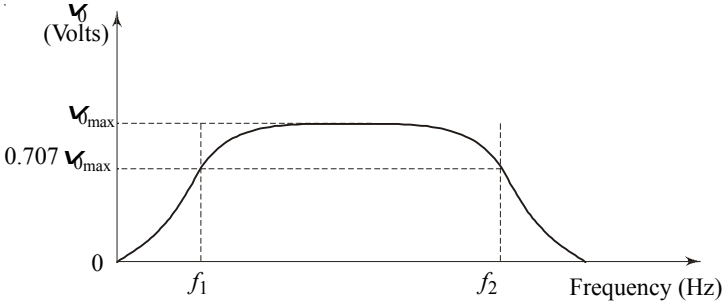


Fig. 1.43(f)

Result:

Frequency	Theoretical	Practical
Lower cut-off Frequency		
Upper cut-off Frequency		

1.18.4 Constant-k Band Elimination Filter

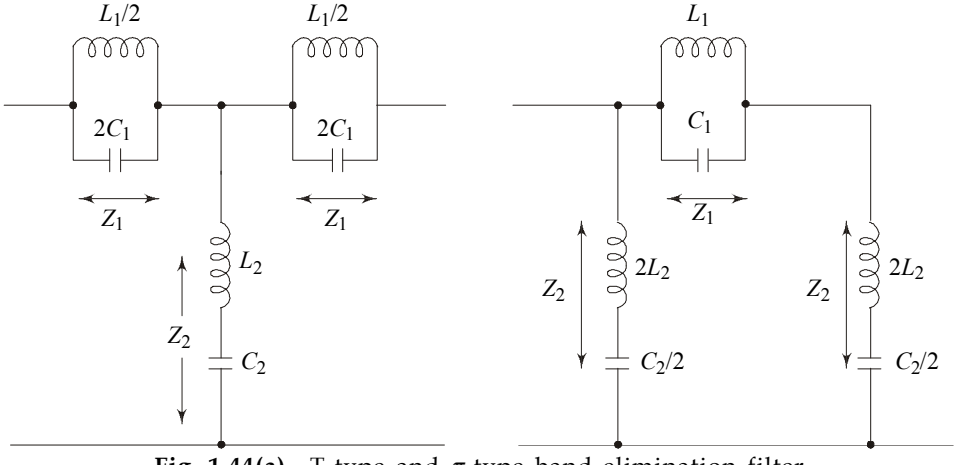


Fig. 1.44(a) T-type and π-type band elimination filter

Resonance condition for the series arm is,

$$\frac{\omega_0 L_1}{2} = \frac{1}{2\omega_0 C_1}$$

Therefore, $$\omega_0^2 L_1 C_1 = 1 \quad (1)$$

Resonance condition for the shunt arm is,

$$\omega_0 L_2 = \frac{1}{\omega_0 C_2}$$

Therefore, $$\omega_0^2 L_2 C_2 = 1 \quad (2)$$

$$f_0 = \sqrt{f_1 f_2}$$

From Equation (1) and (2), we get,

$$\omega_0^2 L_1 C_1 = \omega_0^2 L_2 C_2$$

Therefore, $L_1 C_1 = L_2 C_2$

$$Z_1 = \left(j\omega L_1 - j\frac{1}{\omega C_1} \right) = j\left(\frac{\omega^2 L_1 C_1 - 1}{\omega C_1} \right)$$

$$Z_2 = \left[(j\omega L_2) \| \left(\frac{1}{j\omega C_2} \right) \right] = \frac{(j\omega L_2)\left(\frac{j}{\omega C_2} \right)}{\left(j\omega L_2 + \frac{1}{j\omega C_2} \right)} = \frac{j\omega L_2}{\left(1 - \omega^2 L_2 C_2\right)}$$

But, $L_1 C_1 = L_2 C_2$

Therefore, $Z_1 Z_2 = \frac{L_2}{C_1} = \frac{L_1}{C_2} = R_k^2$

At cut-off frequency,

$$Z_1 = -4Z_2$$

$$f_0 = \sqrt{f_1 f_2}$$

Therefore, $Z_1^2 = -4Z_1 Z_2 = -4 R_k^2$

$$Z_2 = \pm jR_k/2$$

Design:

If the filter is terminated in a load, $R_L = R_k$, then at the lower cut-off frequency,

$$Z_2 = j\left(\frac{1}{j\omega_1 C_2} - \omega_1 L_2 \right) = j\frac{R_k}{2}$$

Substitute, $L_2 C_2 = \frac{1}{\omega_0^2}$ in above equation and simplify,

$$\left(1 - \frac{\omega_1^2}{\omega_0^2} \right) = \frac{R_k \omega_1 C_1}{2}$$

But $f_1 f_2 = f_0^2$, therefore,

$$C_2 = \frac{(f_2 - f_1)}{\pi R_k f_1 f_2}$$

$$L_2 = \frac{R_k}{4\pi (f_2 - f_1)}$$

To evaluate the values for the shunt arm, consider the equations,

$$Z_1 Z_2 = \frac{L_2}{C_1} = \frac{L_1}{C_2} = R_k^2$$

$$L_1 = C_2 R_k^2 = \frac{R_k (f_2 - f_1)}{\pi f_1 f_2}$$

$$C_1 = L_2/R_k^2 = \frac{1}{4\pi R_k (f_2 - f_1)}$$

Model Plot: (Propagation/Attenuation Parameter)

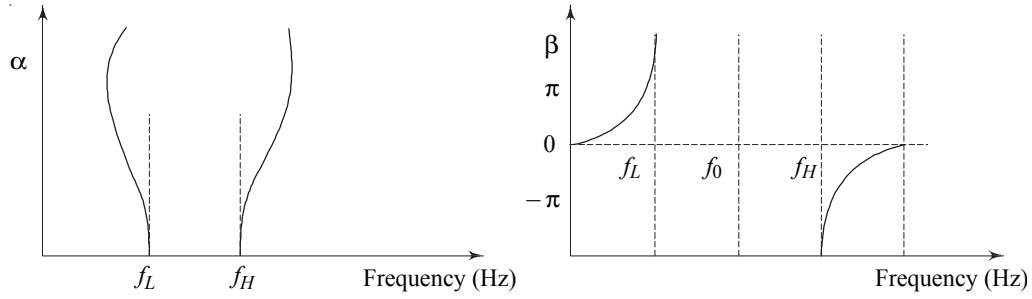


Fig. 1.44 (c), (d) Ideal propagation constant and attenuation constant plot

Experiment (Constant-k Band Elimination Filter)

Aim: ***To Design and Test a Constant–k BEF and Measure its Cut-Off Frequency***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1

Circuit Diagram:

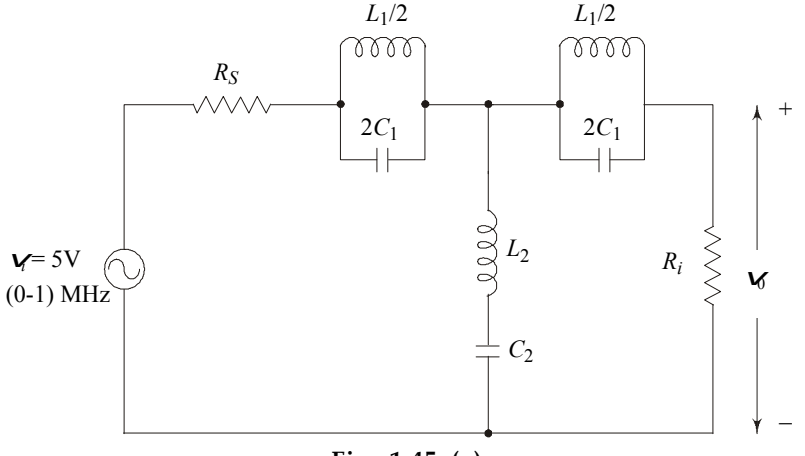


Fig. 1.45 (a)

Design:

To evaluate the values for the series arm, consider the equations,

$$C_2 = \frac{(f_2 - f_1)}{\pi R_k f_1 f_2}$$

$$L_2 = \frac{R_k}{4\pi (f_2 - f_1)}$$

To evaluate the values for the shunt arm, consider the equations,

$$L_1 = C_2 R_k^2 = \frac{R_k\,(f_2 - f_1)}{\pi f_1 f_2}$$

$$C_1 = L_2/R_k^2 = \frac{1}{4\pi R_k (f_2 - f_1)}$$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input voltage, v_i = 5V using signal generator and vary the frequency from (0-1) MHz in regular steps.
3. Note down the corresponding output voltage.
4. Plot the following graph:
   (a) Output voltage v/s frequencies
   (b) Attenuation factor (α) vs frequencies
   (c) Phase angle (β) v/s frequencies
   (d) Characteristic impedance (Z_0) vs frequencies (f/f_c)

Tabular Column:

Frequency (Hz)	Output Voltage (Volts)	α	β	Z_0

Model Graph:

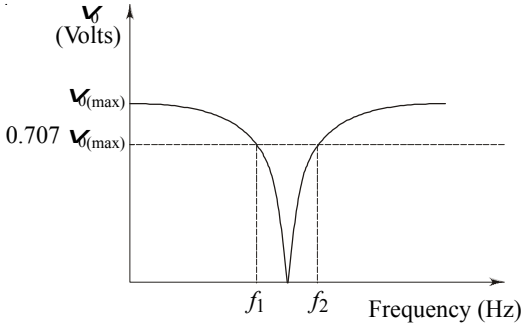


Fig. 1.45 (b)

Result:

Frequency	Theoretical	Practical
Lower cut-off frequency		
Upper cut-off frequency		

1.18.5 m-Derived Filter

The major limitation of the constant-K type filter is that the attenuation is not sharp in the stop band region.

Transformation of Constant–K Type to m–Derived Filter

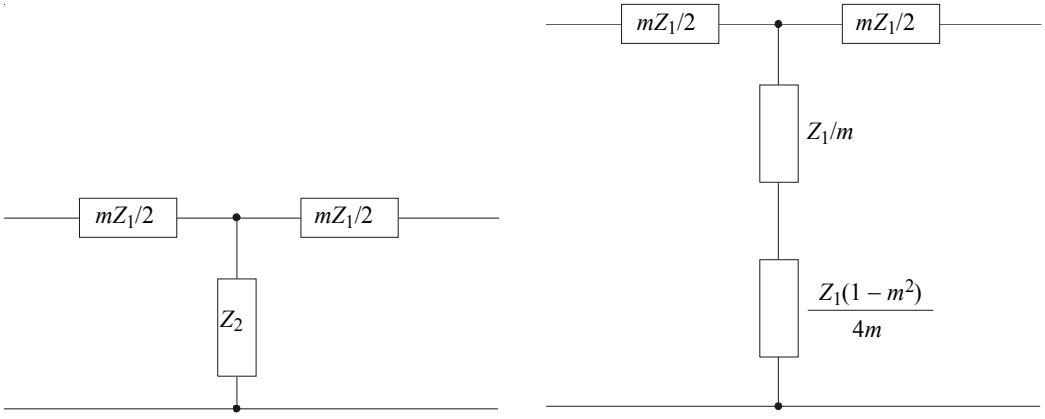


Fig. 1.46 (a) T-proto type (b) T-type m-derived filter

$$\sqrt{\frac{Z_1^2}{4} + Z_1 Z_2} = \sqrt{\frac{m^2 Z_1^2}{4} + m\frac{Z_1}{2} Z_2}$$

On simplification,

$$Z_1^2 = \frac{Z_1}{4m}\ (1 - m^2) + \frac{Z_2}{m}$$

π–Proto Type:

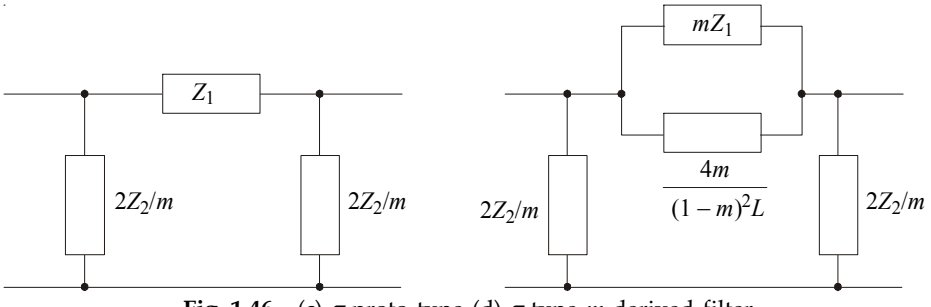


Fig. 1.46 (c) π-proto type (d) π-type m-derived filter

$$Z_{0\pi} = Z^1{}_{0\pi}$$

$$\sqrt{\frac{Z_1 Z_2}{1 + \frac{Z_1}{4Z_2}}} = \sqrt{\frac{\frac{Z_1^1 Z_2}{m}}{1 + \frac{\frac{Z_1^1}{4Z_2}}{m}}}$$

On simplification,

$$Z_1^1 = \left\{ m Z_1 \,||\, \frac{4m}{\left(1 - m^2\right)} Z_2 \right\}$$

Since $\frac{(1-m^2)}{4m}$ should be positive to realize the impedance Z_2^1 Physically, $0 < m < 1$.

1.18.6 m-Derived Low Pass Filter

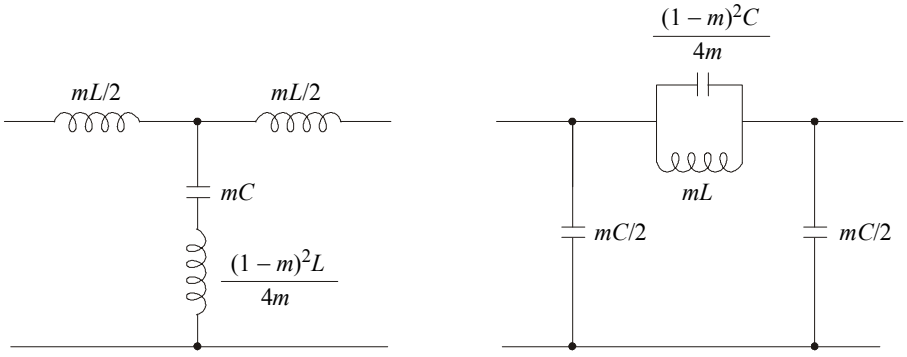


Fig. 1.47 (a), (b) T-type and π-type m-derived low pass filter

The shunt arm (T-section) is to be chosen so that it is resonant at some frequency, f_∞ above cut-off frequency, f_c. If the shunt arm is series resonant, its impedance will be minimum or zero. Therefore, the output is zero and will correspond to infinite attenuation at this particular frequency. Thus, at f_∞,

$$\frac{1}{m\omega_r C} = \frac{1-m^2}{4m} = \omega_r L$$

where, ω_r = resonant frequency

Therefore, $$f_r = \frac{1}{\pi\sqrt{LC(1-m^2)}} = f_\infty$$

Since the cut-off frequency for the LPF is,

$$f_c = \frac{1}{\pi\sqrt{LC}}$$

Therefore, $$f_\infty = \frac{f_C}{\sqrt{1-m^2}} \text{ and } m = \sqrt{1-\left(\frac{f_c}{f_\infty}\right)^2}$$

If a sharp cut-off is desired, f_∞ should be near to f_c. Therefore, smaller the value of m, sharper is the cut-off frequency.

For the m-derived π-section,

$$m\omega_r L = \frac{1}{\left(\frac{1-m^2}{4m}\right)\omega_r C}$$

$$f_r = \frac{1}{\pi\sqrt{LC(1-m^2)}}$$

Since, $$f_c = \frac{1}{\pi\sqrt{LC}}$$

Therefore, $$f_r = \frac{f_C}{\sqrt{1 - m^2}} = f_\infty$$

The pass band is given by,

$$\alpha = 2 \cosh^{-1} \left[\frac{m\left(\frac{f}{f_c}\right)}{\sqrt{1 - \left(\frac{f}{f_\infty}\right)^2}} \right]$$

The attenuation band is given by,

$$\beta = 2 \sin^{-1} \left[\frac{m\left(\frac{f}{f_c}\right)}{\sqrt{1 - \left(\frac{f}{f_\infty}\right)^2 \left(1 - m^2\right)}} \right]$$

Model Plot: (Propagation Parameter)

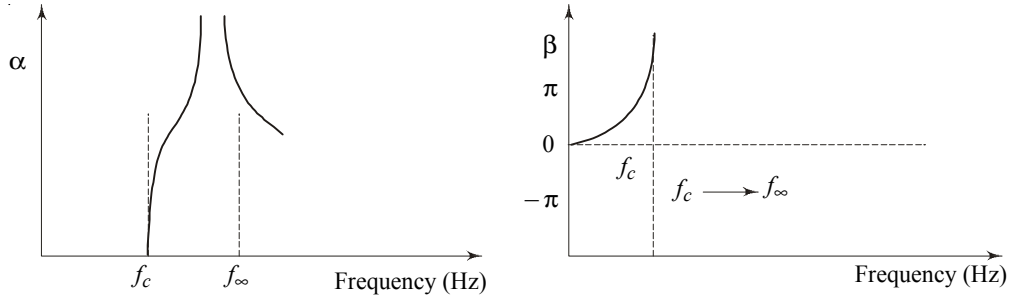


Fig. 1.47(c) Propagation constant plot

Model Plot: (Characteristic Parameter)

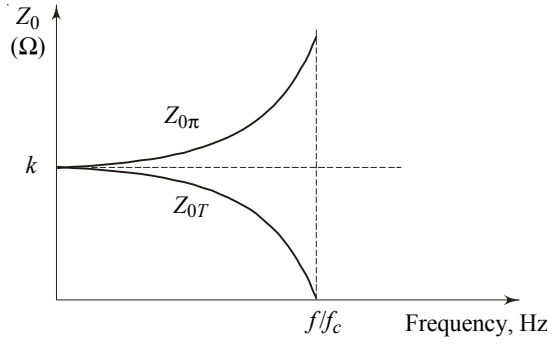


Fig. 1.47 (d) Characteristic impedance plot

Experiment (m-Derived LPF)

Aim: ***To Design and Test an m–Derived LPF and Measure its Cut-Off Frequency***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1

Circuit Diagram:

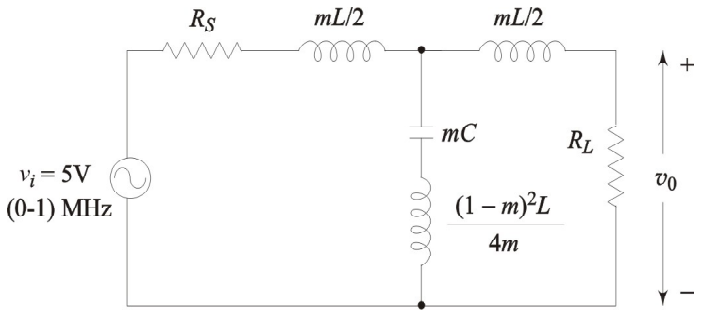


Fig. 1.48 (a)

Design: $0 < m < 1$ ($m = 0.5$, say); $f_c = 2$ kHz

Assume, $C = 0.01$ μF

$$f_r = \frac{1}{\pi\sqrt{LC\left(1-m^2\right)}}$$

Calculate $L = ?$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input voltage, $v_i = 5$V using signal generator and vary the frequency from (0-1) MHz in regular steps.
3. Note down the corresponding output voltage.
4. Plot the following graph:
   (a) Output voltage vs frequencies
   (b) Attenuation factor (α) vs frequencies
   (c) Phase angle (β) v/s frequencies
   (d) Characteristic impedance (Z_0) vs frequencies (f/f_c)

Tabular Column:

Frequency (Hz)	Output Voltage (Volts)	α	β	Z_0

Model Graph:

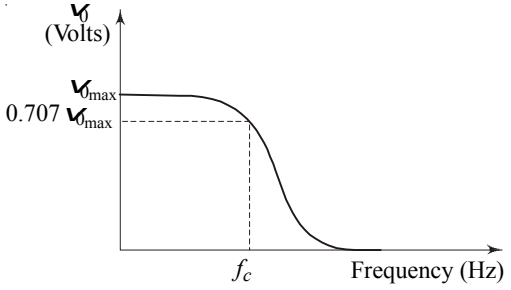


Fig. 1.48 (b)

Result:

	Theoretical	Practical
Cut-off Frequency		

Exercises:

1. Design a π-section *m*-derived LPF and calculate its parameter. Compare the result with T-section *m*-derived LPF.
2. Explain the characteristic difference between constant-k LPF and *m*-derived LPF.

1.18.7 m-Derived High Pass Filter

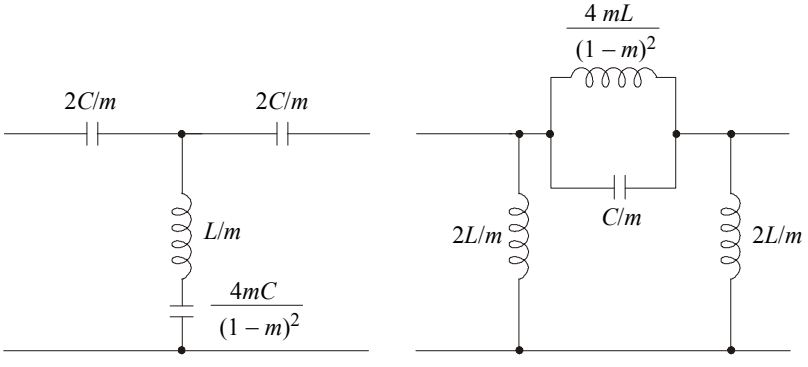


Fig. 1.49 (a), (b) T-type and π-type *m*-derived high pass filter

The shunt arm (T-section) is to be chosen so that it is resonant at some frequency, f_∞ above cut-off frequency, f_c. If the shunt arm is series resonant, its impedance will be minimum or zero. Therefore, the output is zero and will correspond to infinite attenuation at this particular frequency. Thus, at f_∞,

$$\omega_r = \left(\frac{L}{m}\right) = \frac{1-m^2}{4m}\left(\frac{1}{\omega_r C}\right)$$

where, ω_r = resonant frequency

Therefore,

$$\omega_r = \frac{1}{\frac{L}{m}\left[\frac{4m}{(1-m^2)}\right]C} = \frac{(1-m^2)}{4LC} = \omega_\infty^2$$

$$\omega_\infty = \frac{\sqrt{1-m^2}}{2\sqrt{LC}}$$

$$f_\infty = \frac{\sqrt{1-m^2}}{4\sqrt{LC}}$$

Since the cut-off frequency for the HPF is,

$$f_c = \frac{1}{4\pi\sqrt{LC}}$$

Therefore, $f_\infty = \sqrt{f_c\left(1-m^2\right)}$ and $m = \sqrt{1-\left(\frac{f_\infty}{f_c}\right)^2}$

If a sharp cut-off is desired, f_∞ should be near to f_c. Therefore, smaller the value of m, sharper is the cut-off frequency.

For the m-derived π-section,

$$\frac{m}{\omega_r C} = \frac{\omega_r L}{\left(\frac{1-m^2}{4m}\right)}$$

$$\omega_r^2 = \omega_\infty^2 = \frac{\left(1-m^2\right)}{4LC}$$

Therefore, $f_r = \frac{\sqrt{1-m^2}}{4\pi\sqrt{LC}} = f_\infty$

The pass band is given by,

$$\alpha = 2\ \cosh^{-1}\left[\frac{m\left(\frac{f_c}{f}\right)}{\sqrt{1-\left(\frac{f_\infty}{f}\right)^2}}\right]$$

The attenuation band is given by,

$$\beta = 2\ \sin^{-1}\left[\frac{m\left(\frac{f_c}{f}\right)}{\sqrt{1-\left(\frac{f_\infty}{f}\right)^2\left(1-m^2\right)}}\right]$$

Model Plot: (Propagation Parameter)

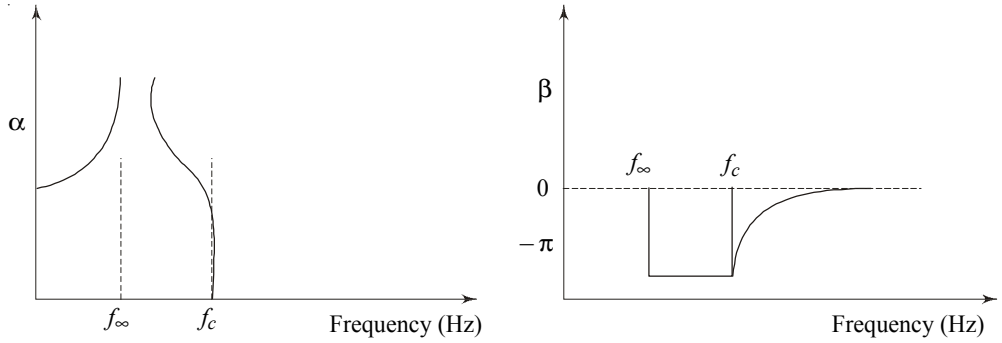


Fig. 1.49(a) Propagation constant plot

Model Plot: (Characteristic Parameter)

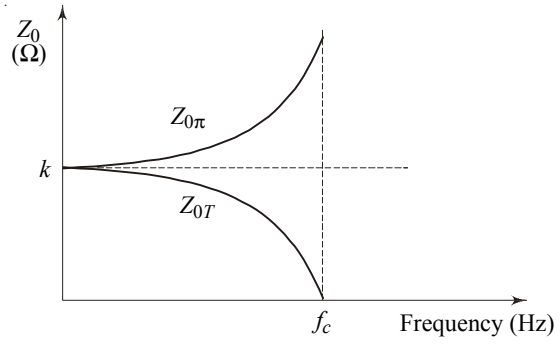


Fig. 1.49(b) Characteristic impedance plot

Experiment (m-Derived LPF)

Aim: ***To Design and Test a m–Derived LPF and Measure its Cut-Off Frequency***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1

Circuit Diagram:

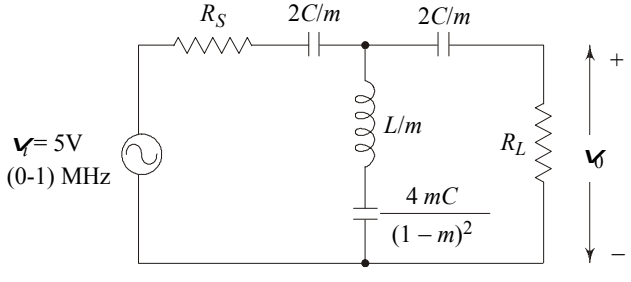


Fig. 1.50(a)

Design:

$0 < m < 1$ (m = 0.5, say); f_c = 2 kHz

Assuming, $C = 0.01\ \mu F$,

$$f_r = \frac{1}{4\pi\sqrt{LC}},$$

calculate L = ?

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input voltage, v_i = 5V using signal generator and vary the frequency from (0-1) MHz in regular steps.
3. Note down the corresponding output voltage.
4. Plot the fllowing graph:
   (a) Output voltage vs frequencies
   (b) Attenuation factor (α) vs frequencies
   (c) Phase angle (β) v/s frequencies
   (d) Characteristic impedance (Z_0) vs frequencies (f/f_c)

Tabular Column:

Frequency (Hz)	Output Voltage (Volts)	α	β	Z_0

Model Graph:

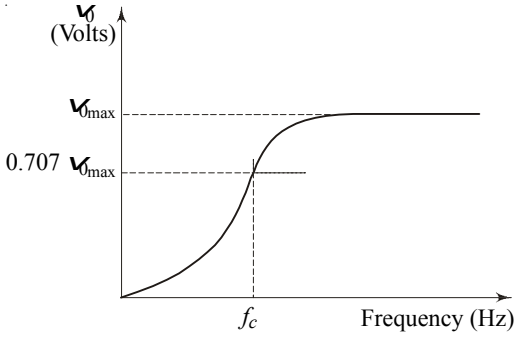


Fig. 1.50(b)

Result:

Frequency	Theoretical	Practical
Cut-off Frequency		

Exercises:

1. Design a π-section *m*-derived HPF and calculate its parameter. Compare the result with T-section *m*-derived HPF.
2. Explain the characteristic difference between constant-k HPF and *m*-derived HPF.

1.19 ATTENUATOR

An attenuator is a two-port networks (purely resistance) and is used to reduce the signal level to a designed/desired level. It will introduce loss without affecting the impedance matching between source and the terminating load. Attenuators can be symmetrical or asymmetrical, and also can be fixed or variable.

$$\text{Attenuation in dB} = 10 \log_{10} \left(\frac{P_1}{P_2} \right)$$

where, P_1 = input power

P_2 = output power

For a proper termination, source (input) resistance should be matched with characteristic resistance, R_0 of the attenuator.

i.e., $$\left(\frac{P_1}{P_2} \right) = \frac{I_1^2 R_0}{I_2^2 R_0} = \frac{I_1^2}{I_2^2} = \frac{V_1^2}{V_2^2}$$

where, I_1, V_1 = input current and voltage respectively

I_2, V_2 = output current and voltage respectively

Hence, attenuation (dB), $D_{dB} = 20 \log_{10} \left(\frac{V_1}{V_2} \right)$

$$D_{dB} = 20 \log_{10} \left(\frac{I_1}{I_2} \right)$$

If, $$N = \left(\frac{V_1}{V_2} \right) = \left(\frac{I_1}{I_2} \right), \text{ then } \left(\frac{P_1}{P_2} \right) = N^2$$

Therefore, $$N = \text{antilog} \left(\frac{D_{dB}}{20} \right)$$

π-Attenuator

Proto-type:

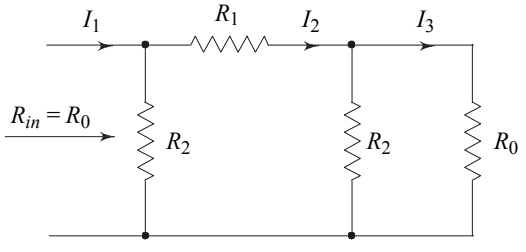


Fig. 1.51(a) π-attenuator

Applying KVL to all three meshes, we get

$$I_2R_1 + (I_2 - I_3)\ R_2 + (I_2 - I_1)\ R_2 = 0$$

$$I_3R_0 + (I_3 - I_2)\ R_2 = 0$$

$$Z_{in} = R_{in} = R_0 = \{[(R_0 \parallel R_2) + R_1] \parallel R_2\}$$

From above three equations, solve for R_1 and R_2, we get

$$R_1 = R_0\left(\frac{\left(N^2 - 1\right)}{2N}\right)$$

$$R_2 = R_0\left(\frac{N+1}{N-1}\right)$$

T-Attenuator

Proto-Type:

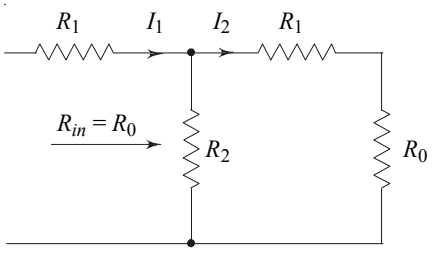


Fig. 1.51(b) T-attenuator

Applying KVL to all three meshes, we get

$$I_2R_1 + (I_2 - I_1)\ R_2 + I_2\ R_0 = 0$$

$$Z_{in} = R_{in} = R_0 = \{[(R_0 + R_1) \parallel R_2] + R_1\}$$

From the above two equations, solving for R_1 and R_2, we get

$$R_2 = R_0\left(\frac{2N}{N^2 - 1}\right)$$

$$R_1 = R_0\left(\frac{N-1}{N+1}\right)$$

where, $$N = \left(\frac{I_1}{I_2}\right)$$

Lattice Attenuator or Bridge Attenuator

Proto-Type:

$$Z_0 = \sqrt{Z_{sc}Z_{oc}}$$

$$Z_{sc} = \frac{2R_1R_2}{R_1 + R_2}$$

$$Z_{oc} = \frac{R_1 + R_2}{2}$$

$$Z_0 = R_0 = \sqrt{R_1R_2}$$

Applying KVC to the above two-closed loop, we get

$$I_1(R_0 + R_1) = (I_2 - I_3)\ (R_1 + R_0)$$

$$N = \left(\frac{I_1}{I_2 - I_3}\right)$$

From the above two equations, solving for R_1 and R_2, we get

$$R_1 = R_0\left(\frac{N-1}{N+1}\right)$$

$$R_2 = R_0\left(\frac{N+1}{N-1}\right)$$

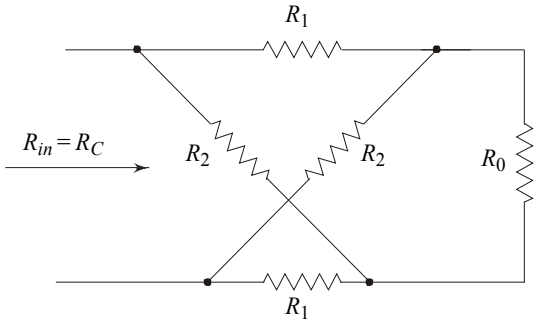


Fig 1.51(c) Lattice attenuator

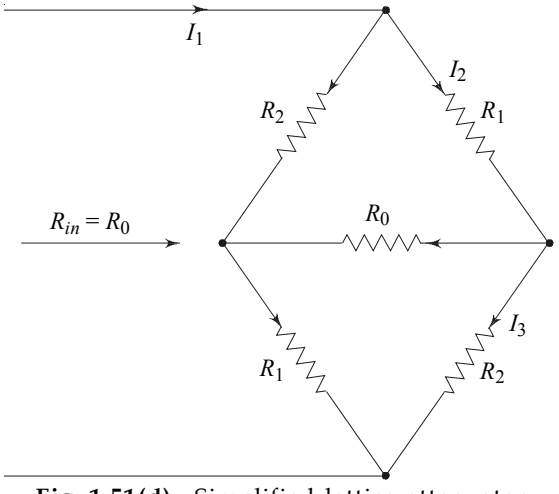


Fig 1.51(d) Simplified lattice attenuator network

Bridge T-Attenuator

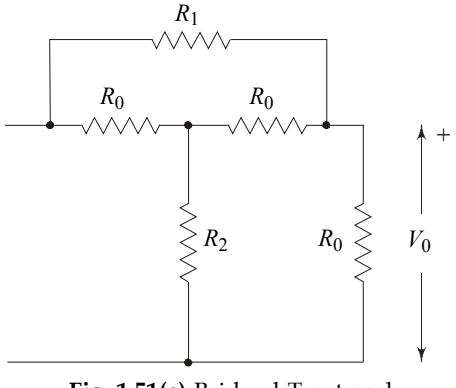


Fig. 1.51(e) Bridged T-network

Condition to attain attenuation is $R_1R_2 = R_0^2$. To solve the above network, use Bi-section theorem.

Bi-Section Theorem Statement: *A network having mirror image symmetry can be reduced to an equivalent lattice structure. The series arm of the equivalent lattice is found by bisecting the given network into two parts, short circuiting all the cut wires and equating the series impedance of the lattice to the input impedance of the bisected network. The diagonal arm is equal to the input impedance of the bisected network when cut wires are open-circuited.*

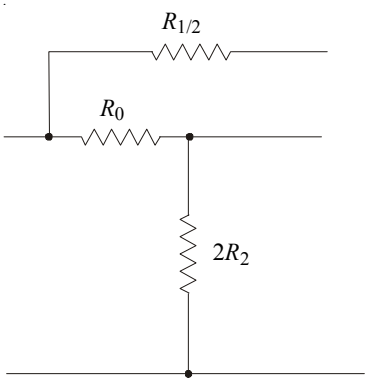


Fig. 1.51(f) Bridged T-network with bi-section

$$R_S = \left[R_0 \,||\, \frac{R_1}{2} \right] \cdots\cdots\cdots \text{(series arm of lattice network)}$$

$$R_{OC} = (R_0 + 2R_2) \cdots\cdots\cdots \text{(diagonal arm of lattice network)}$$

Therefore,

$$R_s = R_0 \left(\frac{N-1}{N+1} \right) \Rightarrow R_2 = \frac{R_0}{N-1}$$

$$R_{oc} = R_0 \left(\frac{N+1}{N-1} \right) \Rightarrow R_1 = R_0 \,(N-1)$$

Experiment (Attenuator)

Aim: ***Design an π–Attenuator, which Attenuate given Signal to the Desired Level***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1

Circuit Diagram:

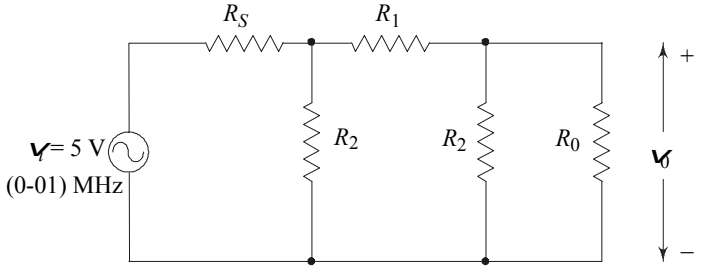


Fig. 1.52(a)

Design:

Given $D = 2\text{d}B$; $R_S = R_L = 680\ \Omega = R_0$

$$R_1 = R_0 \left(\frac{N^2 - 1}{2N} \right)$$

$$R_2 = R_0 \left(\frac{N + 1}{N - 1} \right)$$

$$N = \text{antilog} \left(\frac{D_{dB}}{20} \right)$$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input voltage, v_i = 5V using signal generator and vary the frequency from (0 - 1) MHz in regular steps.
3. Note down the corresponding output voltage.
4. Plot the graph: Output voltage vs frequencies

Tabular Column:

Frequency (Hz)	Output Voltage (Volts)

Model Graph:

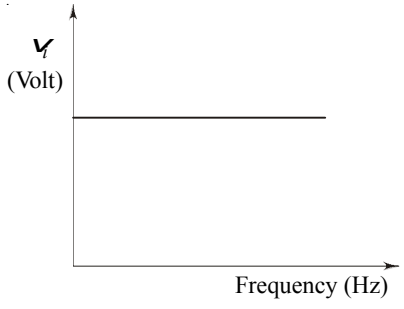


Fig. 1.52(b)

Result:

	Theoretical	Practical

Exercises:

Repeat the procedure for other types of attenuators

1. T- type attenuator
2. Bridge T-type attenuator
3. Lattice attenuator

OBJECTIVE QUESTIONS

1. Distinguish between statically and dynamically induced emf.
2. What is the condition for resonance in RLC series circuit?
3. Draw the phasor diagram (showing voltage and current) for a series RL circuit, taking the current as the reference phasor.
4. What is leakage flux? What is its effect?
5. Where will you use (1) moving coil instruments (2) moving iron instruments?
6. Give the application of capacitors.
7. Give the application of inductors.
8. What is the difference between active and passive transducer?
9. Give the relation between damping factor, damped and undamped frequencies, in relation to RLC circuit.
10. Mention any two advantages of representation of network equations in matrix form.
11. Give any four differences between series and parallel resonance circuits.
12. Give the relationship between Q-factor and bandwidth of a resonance circuit.
13. What is a dual network?
14. Define complex frequency and specify its unit.
15. Give some of the application of transformers.
16. What is fringing?
17. What is the meaning of transformer humming?
18. What is an attenuator? Give some applications.
19. What are the demerits of constant-k filters?
20. Show numerical relationship between decibel and neper.
21. Give one application of maximum power transfer theorem.
22. Define a time constant of a circuit.
23. Give some application of superposition theorem.
24. Give some application of Norton's theorem.
25. What is meant by normalized impedance?
26. Where do you find the application of Resonance concept?
27. "Kirchhoff's current law is valid for inductors and capacitors in parallel". Is it true? Give explanation.

2 ELECTRONIC DEVICE CHARACTERISTIC

2.1 INSULATOR, CONDUCTOR AND SEMICONDUCTOR

A good conductor of electricity is called a conductor. In case of conductors, the forbidden band, which is lying between the conduction band and the valence band, overlaps. Hence even a small bias results in the movement of carriers from the valence band to the conduction band.

A poor conductor of electricity is called an insulator. In case of insulators, the forbidden band, which is lying between the conduction band and the valence band is very broad. Hence there is no movement of carriers from the valence band to conduction band even under biased condition.

A substance for which the width of the forbidden band lies between that of a conductor and an insulator ($\simeq$ 1 eV) is called a semiconductor. The most important semiconductors are silicon and germanium whose forbidden energy region values are 0.785 eV and 1.21 eV respectively. However, the conduction increases with temperature.

Intrinsic and Extrinsic Semicondctors

If the semiconductor is in pure form, it is called an intrinsic semiconductor. In order to increase its conductivity, a pure semiconductor is doped with different dopents depending on the requirement, and is called an extrinsic semiconductor.

Conductivity is directly proportional to the concentration of free electrons. Silicon and germanium are the two semiconductors generally used. These two are tetra-valent. At room temperature, some of the covalent bonds break resulting in conduction. Here an electron, which is dislodged, creates a vacant space, called hole. The hole movement is always opposite to that of the electron movement. Generally, hole movement will be referred to as conventional current, i.e., conventional current direction is always opposite to electron current direction.

P-Type And *N*-Type Semiconductors

If a small percentage of trivalent atoms (e.g., Boron, gallium, indium) is added as an impurity to a pure semiconductor (silicon or germanium), three out of four covalent bonds are filled and the vacancy existing in the fourth bond constitutes a hole. These impurities are called acceptor impurities which give rise to a hole for conduction. Such types of semiconductors are called *p*-type semiconductors.

If to a pure semiconductor (silicon or germanium) a small percentage of pentavalent atoms (e.g., antimony, phosphorus, and arsenic), is added five out of four covalent bonds are filled

and an electron is left out. This results in a conduction due the electron. These impurities are called as donor impurities. Such types of semiconductors are called *n*-type semiconductor.

2.2 TESTING OF ELECTRONIC DEVICES

Diode

1. Connect a multimeter (in resistance mode) across the diode.
2. Observe the resistance of the diode in that position. If it shows a lower resistance value, the diode is in forward bias. Then, the terminal connected to the positive terminal of the multimeter is *p*-junction and other terminal is *n*-junction.
3. Now, reverse the multimeter position and observe the resistance value. If it is high resistance then the given diode is good.

Transistor

1. Transistor follows the same rules as that of a diode.
2. For a npn transistor, connect the multimeter positive terminal to the base terminal of the transistor and the negative terminal to the emitter terminal of the transistor.
3. Follow the procedure given for diode. If it is successful, then the given transistor's base-emitter junction is good.
4. Now, shift the negative terminal of the multimeter to the collector terminal of the transistor by maintaining the positive terminal same.
5. Follow the procedure given for diode. If it is successful, then the given transistor's base-collector junction is good.
6. Observe the collector- to- emitter resistance of the given transistor. It should be a high resistance in both the directions.
7. The above said procedure can be executed for pnp transistor. Here, the multimeter positions should be interchanged, the rest of the procedure remaining same.

Uni-Junction Transistor

1. In case of UJT, emitter to $base_1$ (configuration-1) and emitter to $base_2$ (configuration-2) should exhibit a typical diode characteristic except that the diode resistance in forward and reverse cases is different for the two configurations.
2. The resistance across $base_1$ to $base_2$ should be a fixed resistance in either direction.

Field Effect Transistor

1. In case of FET, drain to source should be a fixed resistance in either direction.
2. Gate to drain or gate to source should be an open circuit or a very high resistance.

2.3 SEMICONDUCTOR DIODE

A *p-n* junction diode is formed by joining a *p*-type and a *n*-type semiconductor through a metallic junction. The symbol and operations are discussed bellow. A diode is a two terminal, uni-junction device. It is unidirectional, i.e., it conducts in only one direction (only on forward biasing).

Biasing is defined as the process in which the device is connected to an external source. If the +ve terminal of the supply is connected to the (*p*-region) anode and –ve terminal to the

(*n*-region) cathode, the diode is said to be *forward biased.* If the connections are reversed, i.e., the +ve terminal of the supply is connected to the (*n*-region) cathode and –ve terminal to (*p*-region) anode, the diode is said to be *reverse biased.*

2.3.1 Unbiased Diode

The current, which flows under unbiased condition, is called *diffusion current.* Diffusion is a process in which the charge carriers move from a region of higher concentration to a region of lower concentration. Diffusion is due to change in concentration gradient across the junction.

In case of diode, the concentration of holes in the *p*-region is more compared to *n*-region and similarly the concentration of electrons are more in *n*-region than in the *p*-region. Due to this difference in concentration there exists a concentration gradient resulting in diffusion. The holes thus diffuse into the *n*-region and the electrons into the *p*-region. During this process they undergo recombination with the opposite charge carriers on completion of their mean time. These recombined carriers are neutral in charge and they oppose the future movement of charge carriers from one region to another. The region near the junction, occupied by the recombined charges, are known as the *Depletion region,* as it is depleted of mobile charge carriers. This is also known as *Space charge* or *Transition region*.

The depletion layer acts as a barrier and prevents further diffusion of charges beyond a certain potential. The difference of potential across the depletion layer is called as the *Barrier potential*. For silicon diodes, it ranges from 0.6 V-0.7 V and for germanium diode, it ranges from 0.2 V-0.3 V.

2.3.2 Biased Diode

The current, which flows under bias condition, is called drift current. Drift current is a process in which the charge carriers move from one region to another due to applied voltage. Drift current exists under forward biasing condition.

Forward Biased Diode On forward biasing a diode initially no current flows due to the barrier potential. The applied forward potential repels the charge carriers and hence pushes them towards the junction (Fig. 2.1). As the applied potential increases, it exceeds the barrier potential at one value (above cut-off value), and the charge carriers gain sufficient energy to cross the potential barrier and enter the other region. The holes, which are the majority carriers in the *p*-region, become minority carriers on entering the *n*-region and electrons, which are the majority carriers in the *n*-region, becomes minority carriers on entering the *p*-region. This injection of the minority carriers results in a current, opposite to the direction of electron movement.

Reverse Biased Diode On reverse biasing, the majority charge carriers are attracted towards the terminals due to the applied potential (Fig. 2.2). This results in widening of the depletion region. Since the charge carriers are pushed towards the terminals no current flows in the device due to majority charge carriers. There will be some current in the device due to the thermally generated minority carriers. The generations of such carriers are independent of the applied potential and hence the current is a constant for all increasing reverse potential. This current is referred to as 'Reverse saturation current, I_{co}' and it

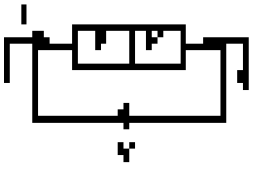


Fig. 2.1

increases with temperature. When the applied reverse voltage is increased beyond a certain limit, it results in breakdown. During breakdown, the diode current increases tremendously for a particular voltage.

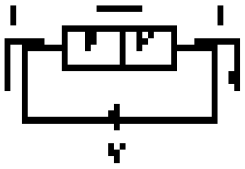


Fig. 2.2

Breakdown in Diode There are two types of breakdown:

1. Avalanche multiplication
2. Zener breakdown

Avalanche Multiplication When the reverse potential increases, thermally generated carrier acquires sufficient energy from it and by colliding it releases energy which breaks the covalent bonds of the bound charges. This results in a new electron-hole pair. These carriers in turn acquire energies from the applied potential, thermal energy and fusion energy and collide with other bound charges. This collision and generation of new electron-hole pairs is continuous and multiplicative, which results in a large amount of charge carriers and thus an increase in reverse current.

Zener Breakdown Due to the applied reverse potential, an electric field exists near the junction. This field exerts a strong force on the bound charges, which breaks the covalent bonds and releases free charge carriers. These newly created electron-hole pairs result in a sudden increase of reverse current. Since the field intensity is directly proportional to the charge concentration, for heavily doped diodes breakdown is due to Zener mechanism, while lightly doped ones breakdown due to avalanche multiplication. As the level of doping is increased, the breakdown voltage decreases.

Effect of Temperature on Breakdown Voltage Heavily doped diodes have a junction with a narrow depletion width and a high field intensity. An increase in temperature increases the energy of the valance electrons and hence makes it easier for the electrons to escape from the covalent bonds. A low applied voltage is sufficient to pull them out from the bond and hence the breakdown voltage decreases with increase in temperature. Such diode exhibits a negative temperature co-efficient. Generally, true Zener breakdown is involved below 6V.

Lightly doped diodes have a junction with a broad depletion layer and low field intensity and the breakdown is due to avalanche multiplication where the charge carriers collide with the bound charges to result in breakdown. When the temperature increases, the vibrations, displacement of atoms in the crystal increases. Due to this the probability of collision with the atoms increases. The intrinsic holes and electrons have less opportunity to give sufficient energy between collisions to start the avalanche process. Hence voltage increases with increase in temperature. Such diode exhibits a positive temperature co-efficient. Generally, true avalanche multiplication is involved above 6V.

2.3.3 Diode Equation

Diode Characteristics In a diode, the following relation relates the current to the voltage;

$$I = I_0 \left[\text{Exp}\ (V / \eta V_T) - 1\right]$$

where, I = Diode current

I_0 = Reverse saturation current

V = Applied bias voltage (+ve if forward biased and –ve if reverse biased)

η = Constant, for germanium semiconductor = 1

for silicon semiconductor = 2

V_T = Volt equivalent of temperature
= $T/11600$ (T in ^{0}Kelvin)

When the diode is forward biased, the applied voltage is positive and is large compared to V_T and Exp ($V / \eta V_T$) >> 1, therefore 1 can be neglected from the equation. Then the diode equation becomes,

$$I = I_0 \text{ Exp } (+V / \eta V_T)$$

Thus on forward biasing, the diode current increases exponentially with an increase in the forward voltage after the cut-in voltage is reached or the barrier potential is overcome.

When the diode is reverse biased, the applied voltage is negative and is small compared to V_T and Exp ($-V / \eta V_T$) << 1. Therefore, exponential term can be neglected. Then the diode equation becomes,

$$I \simeq -I_0$$

Thus on reverse biasing, the reverse current is independent of the applied reverse voltage and is equal to the reverse saturation current. When the reverse voltage is increased beyond a certain limit the diode breakdown and the reverse current shoots up to a very large value. Since reverse saturation current is a temperature dependent parameter, it approximately doubles for every 10° C rise in temperature.

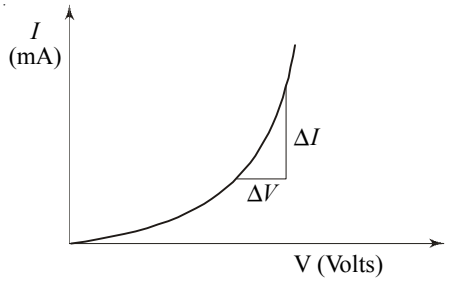


Fig. 2.3

Diode Risistance The static resistance R of a diode is defined as the ratio of V/I at any point on the diode characteristics. It is the reciprocal of the slope of the line joining the operating point to the origin.

The dynamic resistance 'r', of a diode is defined as the ratio of change in voltage to the change in current. The dynamic resistance is not a constant as static resistance; it depends upon the operating voltage, i.e.,

$$r = \mathrm{d}V / \mathrm{d}I$$
$$= \eta V_T / I_0 \text{ Exp } (V / \eta V_T)$$
$$= \eta V_T / (I + I_0)$$

Since ηV_T is small compared to I, r is very small. Hence the forward resistance of the diode is small.

Transition Capacitance, C_T: When the reverse bias is applied, majority carriers move away form the junction. This results in more immobile charges. Hence the thickness of this layer increases with reverse voltage. This results in the accumulation of charge carriers near the junction outside the depletion layer. This represents a charged capacitor with opposite charges on either side of

the plates. This is referred to as the transition capacitance or space charge capacitance or depletion capacitance, C_T, Where C_T is given by,

$$C_T = \varepsilon A / W$$

From the above relation it is known that the transition capacitance mainly depends upon the cross sectional area of the junction and is inversely proportional to the depletion width. ε is the dielectric media of the depletion layer.

Diffusion Capcitance, C_D: When the forward bias is applied, majority carriers move from one region to another resulting in a small depletion layer. This inturn results in the accumulation of charge carriers near the junction outside the depletion layer. This also represents a charged capacitor with opposite charges on either side of the plates. This is referred to as the diffusion capacitance, C_D. Diffusion capacitance is given by,

$$C_D = \tau / r$$

where r = dynamic resistance

τ = mean life time (time interval between the appearance and disappearance of a charge carrier before it undergoes recombination).

Experiment (Diode Characteristics)

Aim: To study the Diode Characteristics Under Forward and Reverse Bias Condition

1. Junction Diode
2. Zener Diode

Equipment Required:

Name of the Equipment	Range	Quantity Y
Power supply	(0-30) V	1 No
Ammeter	(0-30) mA	1 No
	(0.100) μA	1 No
Voltmeter	(0-1) V	1 No
	(0-30) V	1 No

Circuit:

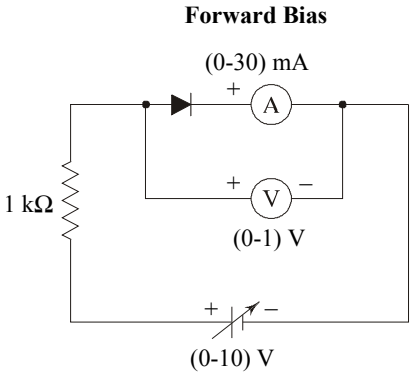


Fig. 2.4

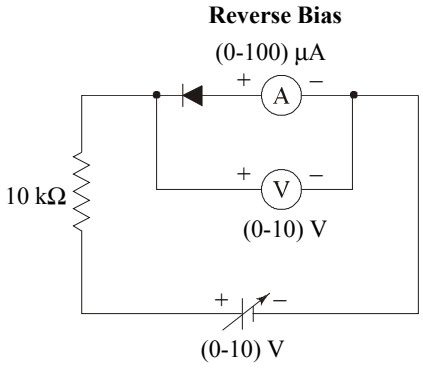


Fig. 2.5

Procedure:

Forward Biasing

1. Connect the circuit as per the circuit diagram.
2. Vary the power supply voltage in such a way that the readings are taken in steps of 0.1V in the voltmeter till the needle of the power supply shows 20 V.
3. Note down the corresponding ammeter readings.
4. Plot the graph: V against I
5. Find the dynamic resistance, $r = \dfrac{\Delta V}{\Delta I}$

Reverse Biasing

1. Connect the circuit as per the circuit diagram.
2. Vary the power supply voltage in steps of 1 V till the voltmeter reads 20 V.
3. Note down the corresponding ammeter readings.
4. Plot the graph: V against I.
5. Find the dynamic resistance, $r = \dfrac{\Delta V}{\Delta I}$

Follow the above-mentioned procedure for other diodes.

Result:

Forward and reverse bias characteristics of junction and Zener diodes are plotted and their dynamic resistance is as follows:

Dynamic resistance, r	Junction diode	Zener diode
Forward bias		
Reverse bias		

Model Graph:

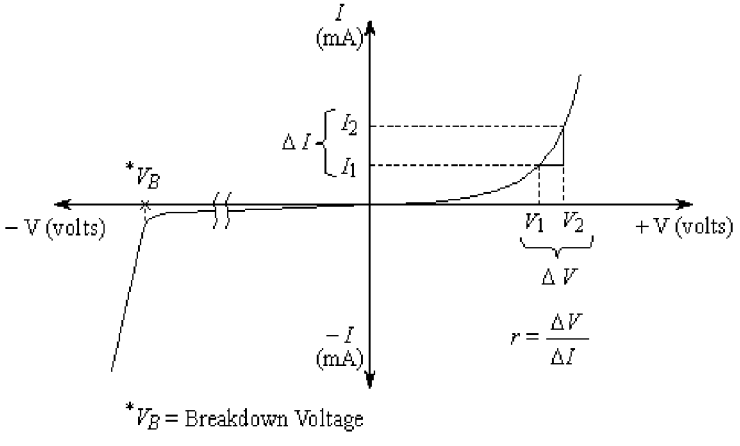


Fig. 2.6

Testing of Diode Put negative probe on cathode and positive probe on anode, it will not show any deflection. Now put a negative probe on the cathode; it will show reading. If in both of these positions the diode does not show any deflection,. then the diode is open. If in both of

these positions the diode show low resistance, the diode is leaking. If in both of them positions the diode shows 0 ohms, then the diode is short. If we take the voltage drop across the diode that is forward biased, it will show 0.6 V to 0.7 V for silicon diode and 0.2 V to 0.3 V for germanium diode.

2.4 DIODE RECTIFIER

The process of converting the alternating voltage and currents to a pulsating direct current is called *rectification*. Any electrical device that offers low resistance to current in one direction and a high resistance in the other direction is capable of converting a sinusoidal waveform into a unidirectional waveform. This sort of characteristic is obtained in a diode and hence it is used in the design of a rectifier.

Filter To obtain a pure DC voltage at the output, filtering is done where the AC is removed and the DC is obtained.

Voltage Regulation The output varies with the variation in AC mains or non-linearity. To compensate for these variations a voltage regulator is used which regulates and maintains the output voltage at the same value.

Block Diagram

Fig. 2.7

Conversion of AC to DC is called rectification and it is obtained through a rectifier circuit, which use diodes as circuit element.

When one half of the AC cycle is rectified then it is known as half-wave rectification and if both the half-cycles are rectified then it is known as full-wave rectification.

2.4.1 Half-Wave Rectifier

Consider the given circuit. Assume the diode to be ideal, i.e., $V_f = 0$, $R_r = \infty$, $R_f = 0$. During the +ve half cycle, the diode is forward biased and it conducts and hence a current flows through the load resistor. During the –ve half cycle, the diode is reverse biased and it is equivalent to an open circuit. Hence the current through the load resistance is zero. Thus the diode conducts only for one half cycle and results in a half-wave rectified output.

Mathematical Analysis (neglecting R_f and R_S) Let $V_{ac} = V_m \sin \omega t$ is the input AC signal. The current I_{ac} flows only for one half cycle, i.e., from $\omega t = 0$ to $\omega t = \pi$ whereas it is zero for the duration $\pi \le \omega t \le 2\pi$.

Therefore,
$$I_{ac} = \frac{V_{ac}}{R} = \frac{V_m \sin \omega t}{R} = I_m \sin \omega t \cdots\cdots 0 \le \omega t \le \pi$$
$$= 0 \cdots\cdots\cdots \pi \le \omega t \le 2\pi$$

where, I_m = maximum value of current

V_m = maximum value of voltage

Average or DC Value of Current

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} I_m(\sin \omega t)\, d\omega t$$

$$= \frac{Im}{2\pi}\left[\int_0^{\pi} \sin wt\, d\omega t + \int_{\pi}^{2\pi} 0\, d\omega t\right] = \frac{1m}{\pi}$$

Similarly,

$$V_{dc} = \frac{V_m}{\pi}$$

The RMS Value of Current

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} I_{ac}^2\, \omega t}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{2\pi} I_m^2 \sin^2 \omega t\, d\omega t} = \sqrt{\frac{I_m^2}{2\pi}\left[\int_0^{\pi} \sin^2 \omega t\, d\omega t + \int_{\pi}^{2\pi} 0 d\omega t\right]}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\int_0^{\pi} \frac{1-\cos 2wt}{2}\, dwt} = \frac{Im}{2}$$

Similarly,

$$V_{rms} = \frac{Vm}{2}$$

Ripple Factor The output of a half-wave rectifier consists of some undesirable AC components termed as ripple. These can be removed using suitable filter circuits.

Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol γ.

$$\gamma = \frac{V\text{ac}}{V\text{dc}}$$

But $$V_{rms}^2 = V_{ac}^2 + V_{dc}^2$$

Therefore, $$\gamma = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{dc}}$$

Converting V_{rms} and V_{dc} into its corresponding V_m value, we get

$$\gamma = 1.21$$

Rectification Factor The ratio of the output DC power to the input AC power is defind as efficiency.

Output power = $I_{dc}^2\, R$

Input power = $I_{rms}^2(R + R_f)$

where, R_f = forward resistance of the diode.

The diode forward resistance is taken into consideration as the input AC is affected by it.

$$\eta = \frac{P\text{dc}}{P\text{ac}} = \frac{I_{\text{dc}}^2 R}{I_{\text{rms}}^2 \left(R + R_f\right)}$$

Convert I_{dc} and I_{rms} into its corresponding I_m value.

$$\eta = \frac{4}{\pi^2} \times \frac{R}{R + R_f}$$

$$= 40.5\% \text{ (if } R_f << R, \ R_f \text{ can be neglected)}$$

Transformer Utility Factor (TUF) Transformer utility factor can be defined as the ratio of DC power delivered to the load to the AC rating of transformer secondary.

$$\text{TUF} = \frac{P_{\text{dc}}}{P_{\text{ac}} \text{ (rated)}}$$

where $$P_{\text{ac}} \text{ (rated)} = V_{\text{ac}} \text{ (rated)} \times I_{\text{dc}} = \frac{Vm}{\sqrt{2}} \times \frac{\text{Im}}{2}$$

Therefore, $$\text{TUF} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

Percentage of Regulation It is a measure of the variation of AC output voltage as a function of DC output voltage.

$$\text{Percentage of regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

V_{NL} = Voltage across load resistance when no current flows through it.

V_{FL} = Voltage across load resistance when all current flows through it.

For an ideal half-wave rectifier, the percentage of regulation is 0 per cent. For a practical half-wave rectifier,

$$V_{NL} = \frac{Vm}{\pi}$$

$$V_{FL} = \frac{Vm}{\pi} - I_{\text{dc}}(R + R_f)$$

Converting I_{dc} into its corresponding I_m value and substituting in the percentage of regulation formula, we get,

$$\text{Percentage of regulation} = \frac{R_f + R}{R_L} \times 100\%$$

Since $R_f + R_S$ is small compared to R_L, the percentage of regulation is very small for half-wave rectifier.

Peak Inverse Voltage, PIV It is the maximum voltage that has to be withstood by a diode when it is reverse biased.

$$\text{PIV} = V_m$$

Advantages of Half-Wave Rectifier

1. Low cost
2. Simple circuit

Disadvantages of Half-Wave Rectifier

1. High γ
2. Low η
3. Low TUF
4. Since current flows for half a cycle, transformer core gets saturated.

Reduction of Ripple Factor Using Capacitor Filter The reactance of the capacitor, $X_c = \frac{1}{2\pi fc}$. At zero frequency, the capacitor acts as an open circuit (under DC input condition) and as the frequency increases, the reactance of the capacitor gradually decreases. Therefore, for AC signal, the capacitor acts as a variable reactance path depending on the frequency.

During the +ve half cycle, the diode conducts and a current flows in the circuit. This current charges the capacitor to the peak input voltage. This charge across the capacitor reverse biases the diode and the diode stops conducting. Once the capacitor is charged to the peak value, it discharges through the load resistance, R. The discharge continues till the input voltage exceeds the capacitor voltage and starts the conduction of diode once again and hence charges the capacitor.

The discharge of C depends on R. If R is very high, the discharge will be slow as the resistor offers a very high resistance to the flow of current through it. Hence the output will be almost a constant and ripple will be considerably reduced. If R is low, the discharge will be fast as the resistors offer very less resistance to the flow of current through it. Hence the output will contain appreciable ripple.

Calculation of Ripple Factor, γ The average value of load current I_{dc} is the average value of the capacitor discharge current over an interval T_2. The amount of charge discharged by the C during this interval is $I_{dc} \times T_2 = Q$ (discharge).

This charge is replaced during the interval T_1 at which the voltage across the capacitor changes by an amount equal to the peak to peak voltage of the ripple, Vr_{pp}.

We know $Q = VC$,

$$Q \text{ (charging)} = V_{r,\,pp} \times C$$

Since, Q (charging) = Q (discharging)

$$V_{r,\,pp} \times C = I_{dc} \times T_2$$

Therefore, $$V_{r,\,pp} = I_{dc} \frac{T_2}{C}$$

Assume R is high. Therefore, recharge time for C is less compared to its discharging time, i.e., $T_1 << T$

Therefore, $$T_2 \approx \frac{T}{2} = \frac{1}{2f}$$

The ripple waveform is triangular in nature and so its rms value is

$$V_{r,\ \text{rms}} = \frac{V_{r,\ pp}}{2\sqrt{3}}$$

But, $$I_{\text{dc}} = \frac{V_{\text{dc}}}{R},$$

Therefore, $$V_{r,\ pp} = \frac{V_{\text{dc}}}{RC} \times \frac{1}{2f}$$

Substituting in $V_{r,\ \text{rms}}$ we get,

$$V_{r,\ \text{rms}} = \frac{V_{\text{dc}}}{4\sqrt{3fRC}}$$

$$\gamma = \frac{V_{r,\ \text{rms}}}{V_{\text{dc}}} = \frac{1}{4\sqrt{3fRC}}$$

Advantages of Capacitor Filter

1. γ is reduced
2. η is improved
3. TUF is increased

2.4.2 Full-Wave Rectifier

The full-wave rectifier consists of a center-tap transformer, which results in equal voltages above and below the center-tap. During the +ve half cycle, a +ve voltage appears at the anode of D_1 while a –ve voltage appears at the anode of D_2. Due to this, diode D_1 is forward biased and it results in a current Id_1 through the load R.

During the –ve half cycle, a +ve voltage appears at the anode of D_2 and hence it is forward biased resulting in a current I_{d2} through the load. At the same instant a –ve voltage appears at the anode of D_1, thus reverse biasing it and hence it does not conduct.

The current through the load during both half cycles is in the same direction and hence it is the sum of the individual currents and is unidirectional.

$$I = I_{\text{d1}} + I_{\text{d2}}$$

$$V_{\text{ac}} = V_m \sin \omega t$$

$$I_{\text{d1}} = \frac{Vm}{R} \sin\omega t \ \cdots\cdots\cdots\cdots 0 \le \omega t \le \pi$$

$$= 0 \ \cdots\cdots\cdots \pi \le \omega t \le 2\pi$$

$$I_{\text{d2}} = 0 \ \cdots\cdots\cdots 0 \le \omega t \le \pi$$

$$= \frac{-Vm}{R} \sin\omega t \ \cdots\cdots\cdots \pi \le \omega t \le 2\pi$$

The individual currents and voltages are combined in the load and therefore their average values are double that obtained in a half-wave rectifier circuit.

Average Value of Current, I_{dc}

$$I_{\text{dc}} = \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin \omega t \, \mathrm{d}\omega t - \int_{\pi}^{2\pi} I_m \sin \omega t \, \mathrm{d}\omega t\right] = \frac{2 I_m}{\pi}$$

Similarly,

$$V_{\text{dc}} = \frac{2 Vm}{\pi}$$

RMS Value of Current, V_{rms}

$$I_{\text{rms}} = \sqrt{\frac{1}{2\pi}\left[\int_0^{2} I_m^2 \sin^2 \omega t \, \mathrm{d}\omega t\right]} = \frac{I_m}{\sqrt{2}}$$

Similarly,

$$V_{\text{rms}} = \frac{V_m}{\sqrt{2}}$$

Ripple Factor, γ

$$\gamma = \frac{V_{\text{ac}}}{V_{\text{dc}}} = \frac{\sqrt{V_{\text{rms}}^2 - V_{\text{dc}}^2}}{V_{\text{dc}}}$$

Converting V_{rms} and V_{dc} to their corresponding V_m values, we get

$$\gamma = 0.48$$

Efficiency, η

$$\eta = \frac{P_{\text{dc}}}{P_{\text{ac}}} = \frac{I_{\text{dc}}^2 R}{I_{\text{rms}}^2 \left(R + R_f\right)}$$

Converting I_{dc} and I_{rms} to their corresponding I_m values, we get

$\eta = 81\%$ (if $R >> R_f$, then R_f can be neglected)

Transformer Utility Factor, TUF A full-wave rectifier can be considered as a parallel connection of two half-wave rectifiers. There are two windings for the transformer secondary. Therefore, for full-wave rectifier,

$$\text{TUF}_{\text{secondary}} = 2 \times \text{TUF}_{\text{secondary}} \text{ (half-wave rectifier)} = 0.574$$

$\text{TUF}_{\text{primary}}$ is defined as the ratio of the DC output delivered to the load to the AC rating of the transformer primary.

$$\text{TUF}_{\text{primary}} = \frac{V_{\text{dc}} I_{\text{dc}}}{V_{\text{rms}} I_{\text{rms}}}$$

Writing the above values in terms of maximum value we get

$\text{TUF}_{\text{primary}} = 0.812$ (if R_s: transformer secondary winding resistance + $R_f << R$, then $R_s + R_f$ can be neglected)

Therefore, the average TUF = $\frac{\text{TUF}_{\text{secondary}} + \text{TUF}_{\text{primary}}}{2} = 0.693$

Peak Inverse Voltage, PIV

$$\text{PIV} = 2\ V_m$$

Advantages of Full–Wave Rectifier

1. γ is reduced.
2. η is improved.
3. TUF is increased.
4. DC saturation of the core does not result as equal current flow through the secondary during both the half cycles.

Disadvantages of Full-Wave Rectifier

1. Output voltage is half the secondary voltage.
2. Diodes with high PIV ratings are used.
3. Manufacturing of center-tapped transformer is quite expensive and so full-wave rectifier with center-tapped transformer is costly.

Bridge Rectifier The disadvantages of a full-wave rectifier are overcome in a bridge-rectifier, which does not require a center-tapped transformer.

During the +ve cycle, diodes D_1 and D_2 are forward biased and D_3 and D_4 are reverse biased. Thus current flows in the circuit due to D_1 and D_2 . During –ve cycle D_1 and D_2 are reverse biased and D_3 and D_4 are forward biased which results in a current in the same direction. Thus the current flows for the whole cycle across the load resulting in full-wave rectification.

The diodes used in the case of bridge rectifier should have a PIV of V_m. Since the bridge rectifier does not require a center-tapped transformer, its cost, weight and size are lesser compared to a full-wave rectifier.

Considering an ideal diode and $R_S = 0$, on carrying out a similar analysis as a full-wave rectifier, we get

$$I_{\text{dc}} = \frac{2I_m}{\pi} \text{ and } V_{\text{dc}} = \frac{2V_m}{\pi}$$

$$I_{\text{rms}} = \frac{I_m}{\sqrt{2}} \text{ and } V_{\text{rms}} = \frac{V_m}{\sqrt{2}}$$

$$\gamma = 0.48 \text{ and } \eta = 81.2\%$$

$$\text{TUF} = 0.812$$

$$\text{PIV} = V_m$$

Experiment (Rectifier)

Aim: ***Study of Rectifiers with and without Capacitor Filter***

1. Half-wave rectifier
2. Full-wave rectifier
3. Bridge rectifier

To Find Its:

1. Percentage regulation
2. Ripple factor
3. Transformer utility factor
4. Efficiency

Equipments Required:

Name of the Equipment	Range	Quantity
CRO	(0-20) MHz	1 No
Multimeter		1 No

Circuit:

Half-wave Rectifier:

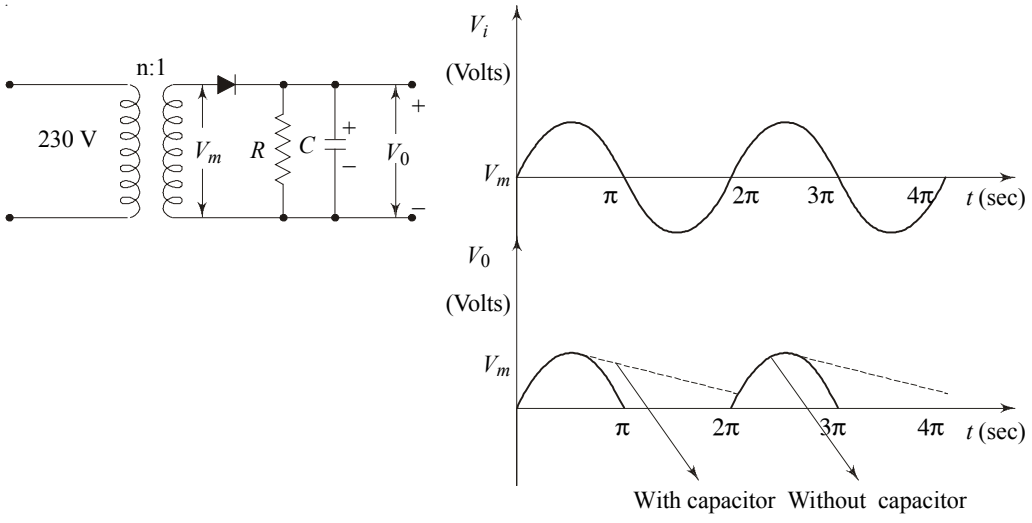


Fig. 2.8

Full-wave Rectifier:

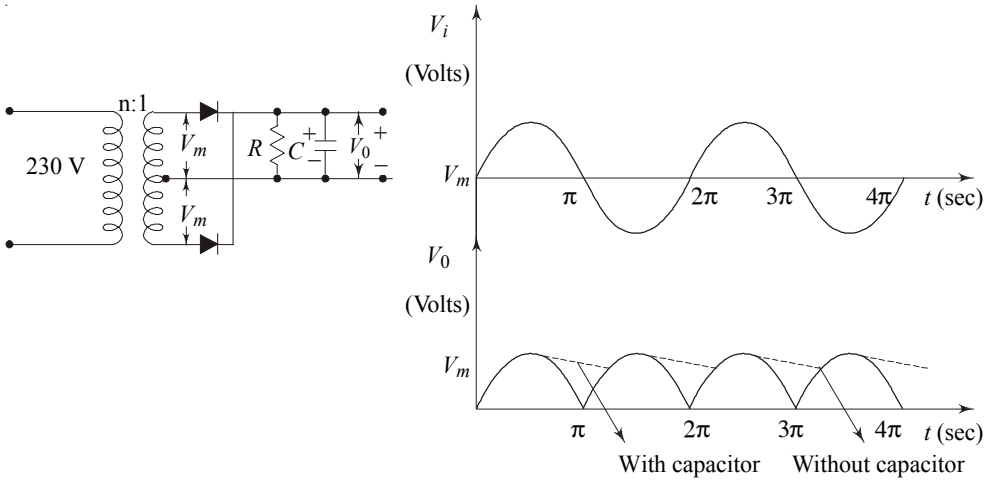


Fig. 2.9

Bridge Rectifier:

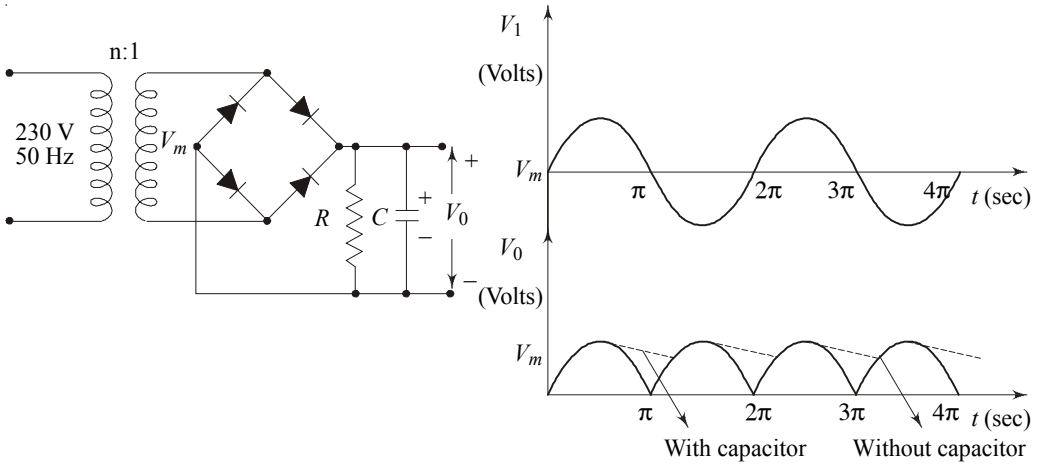


Fig. 2.10

Procedure:

Without Capacitor Filter:

1. Test your transformer: Give 230 V, 50 Hz source to the primary coil of the transformer and observe the AC waveform of rated value without any distortion at the secondary of the transformer.
2. Connect your circuit to the secondary terminals of the transformer.
3. Connect your CRO across the load.
4. Keep the CRO switch in ground-mode and observe the horizontal line and adjust it to the X-axis.
5. Switch the CRO into DC mode and observe the waveform. Note down its amplitude, *Vm* and frequency from the screen along with its multiplication factor.
6. Calculate V_{dc} using the relation: $V_{dc} = \frac{V_m}{\pi}$
7. Switch the CRO into AC mode and observe the waveform. Note down its amplitude, V_m and frequency from the screen along with its multiplication factor.
8. Calculate V_{ac} using the relation: $V^2_{rms} = V^2_{ac} + V^2_{dc}$

   $$V_{rms} = \frac{V_m}{2}$$

9. Calculate the ripple factor from the given formula: $\gamma = \frac{V_{ac}}{V_{dc}}$
10. Remove the load and measure the output AC voltage (AC-mode) and calculate the percentage of voltage regulation using the formula:

$$\text{Percentage regulation} = \frac{V_{noload} - V_{load}}{V_{load}} \times 100\ \%$$

To measure ratio of rectification, observe the power (DC and AC) using wattmeter across the load. The ratio of rectification is given by $\frac{P_{dc}}{P_{ac}}$

With Capacitor:

1. Calculate the value of R by assuming C = 1000 μF and f = 50 Hz using the formula:

   $\gamma = \frac{1}{4\sqrt{3}\, fRC}$ (assume γ as 0.002 or any small value) for full wave rectifier

   $\gamma = \frac{1}{2\sqrt{3}\, fRC}$ for half-wave rectifier.

2. Connect the capacitor across the load resistance and proceed with the above procedure from 1-11 as shown above.

**** Follow the above-mentioned procedure for full wave and bridge rectifier.***

Result:

Parameters	Half-Wave	Full-Wave	Bridge
Ripple factor : with filter : Theoretical Practical Ripple factor : without filter : Theoretical Practical Percentage regulation : Theoretical Practical			

2.5 CLIPPING CIRCUITS

There are varieties of networks that have the ability to *clip-off* a portion of the input signal without distorting the remaining part of the input signal, called *clipper*. Clipping circuits are also referred to as voltage (or current) limiters, amplitude selectors or slicers. Depending on the orientation of the diode and the polarity of the reference voltage, the input signal will *clip*.

A clipping circuit requires a minimum of one diode (either in series or parallel) and one resistor. Power supply is often used to set the various clipping levels.

Let us analyze the following few circuits, where R = 1 kΩ (say)

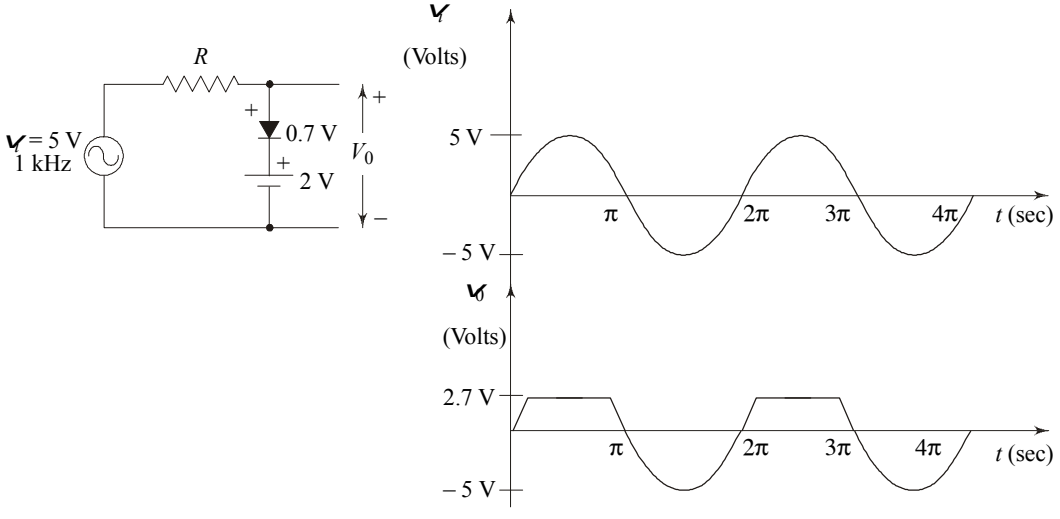


Fig 2.11

Diode forward bias drop is assumed to be 0.7 V.

During the positive half-cycle of the input, less than 2 V, DC supply is dominant over the input signal. So diode is reverse biased and output becomes a faithful reproduction of input till it reaches 2.7 V [diode drop (0.7 V) + DC supply (2 V)]. Once input signal exceeds 2.7 V, diode is forward biased and there is a current in the circuit. Hence the output is clipped at 2.7 V and it remains constant till the input signal falls below the clipped level.

During the negative half-cycle, diode becomes fully reverse-biased. Hence the output waveform is a faithful reproduction of the input.

Let us consider one more circuit where the diode comes in series with the input signal source.

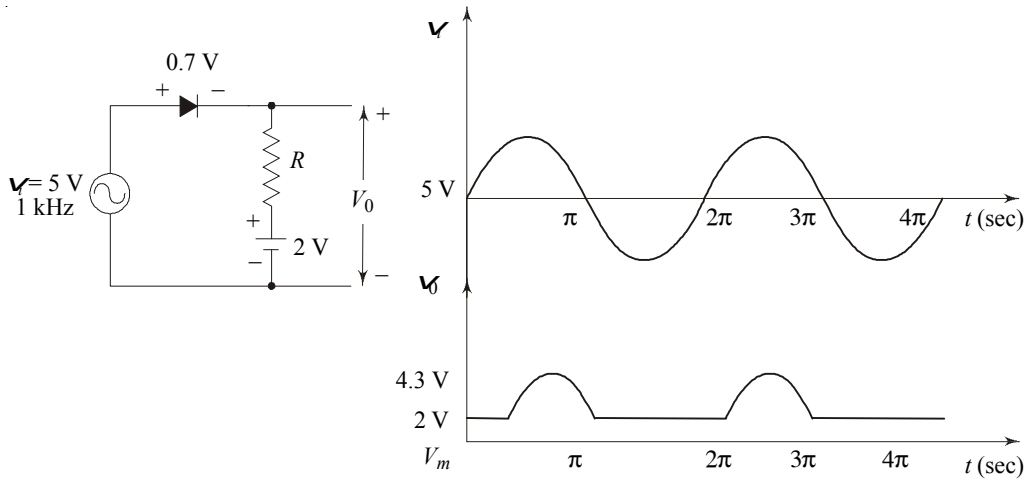


Fig. 2.12

During the positive half-cycle of the input, less than 2 V, DC supply is dominant over the input signal. So diode is reverse biased and output becomes DC (voltage across DC supply, 2 V) till it reaches 2 V. Once input signal exceeds 2.7 V, diode becomes forward biased and there is a current in the circuit. Hence the output across the resistance is directly proportional to the input AC signal.

During the negative half-cycle, diode becomes fully reverse-biased. Hence output waveform equals the DC supply voltage (+ 2 V).

The same explanation holds good for any clipping circuit with or without DC supply. If the DC supply is made equal to zero, the input signal is always referred with respect to zero voltage (ground potential).

Experiment (Clipping Circuits)

Aim: ***To Observe the Clipping Waveform in Different Clipping Configurations***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1
Power supply	(0-30) V	1

Circuit Diagram:

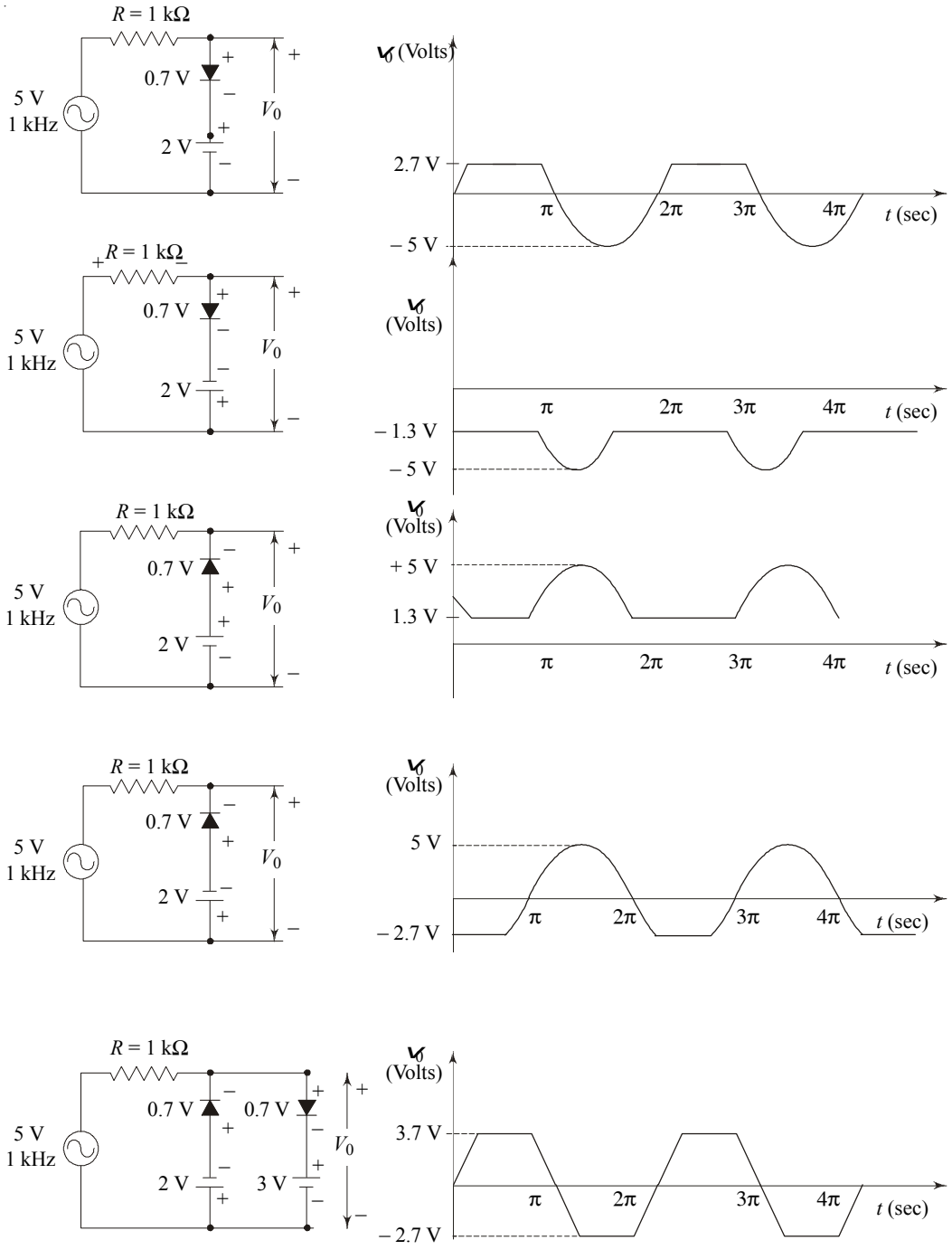


Fig. 2.13

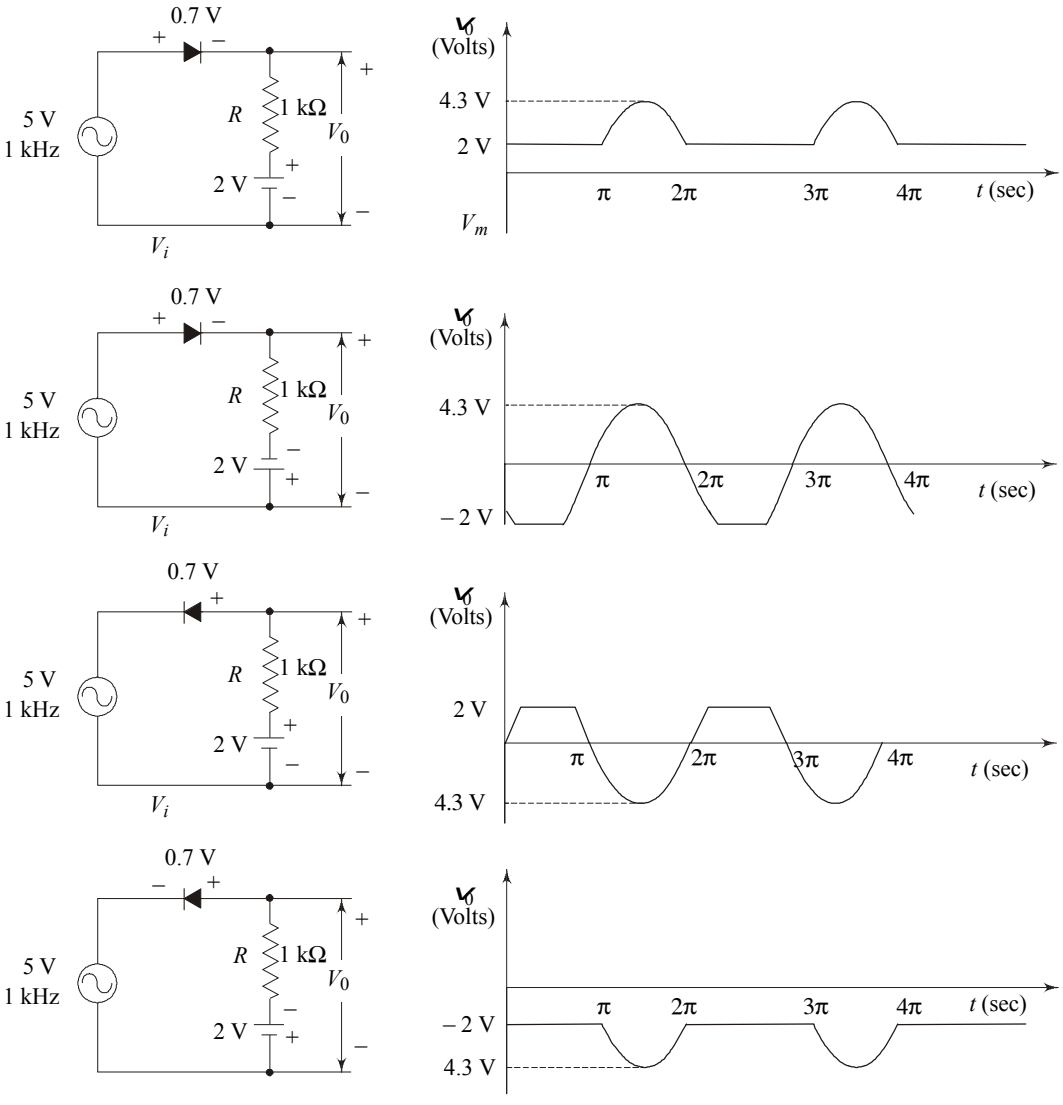


Fig. 2.14

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input signal voltage (say 5 V, 1 kHz) using signal generator.
3. Observe the output waveform using CRO (DC-mode).
4. Sketch the observed waveform on the graph sheet.

2.6 CLAMPER CIRCUITS

The clamping network is one that will *clamp* an input signal to a different DC level. The network consists of a capacitor, a diode and a resistance, but it can also have an independent DC supply to introduce an additional DC shift.

The magnitude of R and C must be chosen such that the time constant, $\tau = RC$, is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval when the diode is non-conducting.

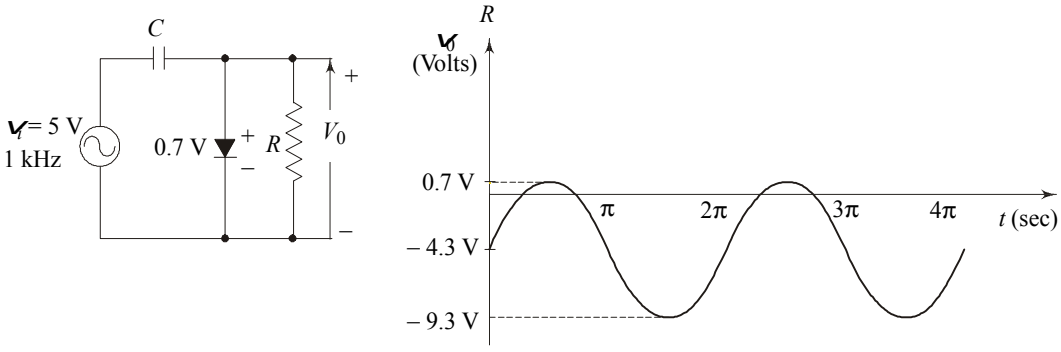


Fig. 2.15

During the positive half-cycle, diode is forward biased and shorts out the effect of the resistor, R. This results in small RC time constant so that the capacitor will charge to peak value (diode drop is considered) very quickly. During this interval, the output voltage is almost short-circuited voltage, $V_0 = {}^{+}0.7$ V (diode drop alone).

During the negative half-cycle, diode will be reverse biased. Therefore the effective output voltage is the voltage drop across the resistance, R.

Voltage drop across R = drop across capacitor + input voltage

$$= -(\text{Diode drop}) - 5 = -4.3 - 5 = 9.3\ V$$

The abovesaid circuit is called a positive clamper. We can also obtain a negative clamper by inverting the diode direction.

Experiment (Clamper Circuits)

Aim: ***To Study the Clamping Circuits***
(a) ***positive clamping circuit*** **(b)** ***negative clamping circuit***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1
Power supply	(0-30) V	1

Circuit Diagram:

Design:

Given $f = 1$ kHz,

$$T = \tau = \frac{1}{f} = 1 \times 10^{-3}\ \text{Sec} = RC$$

Assuming, $C = 0.1\ \mu\text{F}$

Then, $R = 10\ \text{k}\Omega$

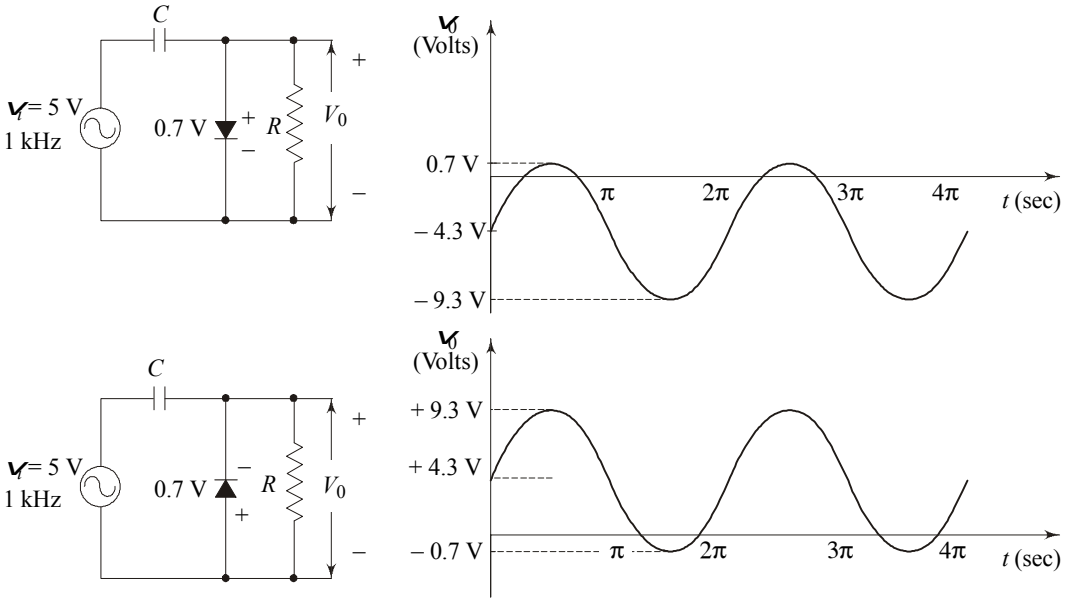


Fig. 2.16

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input signal voltage (say 5 V, 1 kHz) using signal generator.
3. Observe the output waveform using CRO (DC-mode).
4. Sketch the observed waveform on the graph sheet.

2.7 TRANSISTORS

Transistors can be broadly classified as unipolar and bipolar based on the charge carriers taking part in the conduction. In a unipolar transistor the conduction is due to majority charge carriers alone while in a bipolar transistor the conduction is due to both majority and minority charge carriers. A BJT or a Bipolar Junction Transistor is a three terminal two junction semiconductor device and the conduction here is due to both the charge carriers. Hence it is a bipolar device and it amplifies the electrical impulses as they are transferred from the input to the output. A few advantages of the BJT are given below:

1. Low current requirement.
2. Small size.
3. Less weight.
4. Long operating and shelf life.
5. Rugged in nature.

Structure BJT is classified into two types based on the structure (*npn* & *pnp*). A *npn* transistor consists of two *n*-layers in between which a *p*-layer is sandwitched. Similarly, the pnp transistor consists of two *p*-layers in between which a *n*-layer is sandwitched. The transistor consists of three terminals—the Emitter, Base, and Collector. The emitter layer is the source of charge carriers and it is heavily doped with a moderate cross-sectional area. The collector collects the charge carriers emitted by the emitter region and hence has a moderate doping and a large cross-sectional area. The base region is in between these and it

acts as a path for the movement of charge carriers. In order to reduce the recombination of electrons and holes in the base region, this region is lightly doped and is of narrow cross-sectional area.

Terminal	Nature of doping	Cross-sectional area
Emitter	Heavy	Moderate
Base	Light	Narrow
Collector	Moderate	High

2.7.1 Transistor Modelling

The terminal behavior of any two-port network can be specified by two voltages (input and output) and two currents (input and output). We may select two of the four parameters as the independent parameter and remaining two (dependent parameter) in terms of the chosen independent parameter.

If the input current and output voltage are independent and the given network is linear, we may write

$$v_I = h_{11} i_I + h_{12} v_0$$

$$i_0 = h_{21} i_1 + h_{22} v_0$$

The quantity h_{11}, h_{12}, h_{21} and h_{22} are called the h (hybrid)-parameters (they are not alike dimensionally). Let us analyze each h-parameter.

$$h_{11} = \left.\frac{v_i}{i_i}\right|_{v_0 = 0}$$ = input resistance with output terminals short-circuited (Ω), h_i

$$h_{12} = \left.\frac{v_i}{v_0}\right|_{i_i = 0}$$ = reverse voltage gain with input terminals open-circuited (dimension less), h_r

$$h_{21} = \left.\frac{i_0}{i_i}\right|_{v_0 = 0}$$ =forward current gain with output terminals short-circuited (dimension less), h_f

$$h_{22} = \left.\frac{i_0}{v_0}\right|_{i_i = 0}$$ = output admittance with input terminals open-circuited (υ), h_0

The first subscript in h-parameter represent the type of h-parameter (input resistance, i/ forward current gain, f/ output admittance, o/ reverse voltage gain, r) and the second subscript represent the type of configuration (CE/CB/CC).

***h*-parameter model: (transistor)**

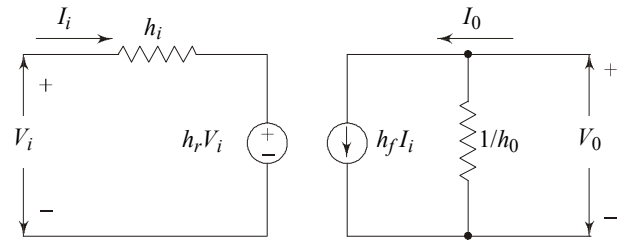


Fig. 2.17

Biasing

The transistor being a two-junction device can be biased in the following manner.

E-B junction	C-B junction	Mode of operation
Reverse bias	Reverse bias	Cut-off
Forward bias	Reverse bias	Active or Normal
Forward bias	Forward bias	Saturation
Reverse bias	Forward bias	Inverse mode

Now after knowing the basics of BJT we shall discuss why it is so called. We are already aware that due to the conduction of both majority and minority carriers it is called Bipolar. The name transistor arises from *transfer resistor*. Normally, a transistor operates with the EB junction forward biased and CB junction reverse biased. It is obvious that the current through the forward biased region is greater than the current through the reverse biased region. But in a transistor the current is the same in both the junctions which indicates that there is a transfer of resistance between the two junctions. Due to this fact the transistor is known as a transfer resistor or transistor.

2.7.2 Transistor Configurations

It is known that the main application of a transistor is as an amplifier. An amplifier requires two input terminals and two output terminals. The transistor being a three terminal device makes it applicable as an amplifier by making one of the terminals common to both the input and output. Depending on which terminal is made common the transistor is classified into three configurations—common base, common emitter, and common collector.

Common Base Configuration

In this configuration the base is made common to both the input and output. The emitter is given the input and the output is taken across the collector. In order to analyze the features of this configuration let us determine the different gains of the circuit. To start, the current gain is defined as the ratio between the *o*/*p* and *i*/*p* current. Hence $A_I = \frac{I_c}{I_e}$. We know that $I_e = I_c + I_b$ and so, here the current gain is less than unity. Similarly, the voltage gain is the ratio between the *o*/*p* and *i*/*p* voltage and so $A_v = \frac{V_c}{V_e} = \frac{I_c R_c}{I_e R_e}$. Though $I_e > I_c$, R_c, the reverse resistance of collector junction is greater than R_e, the forward resistance of emitter junction and so $I_c R_c >> I_e R_e$. Hence the voltage gain is high. Due to the high voltage gain, the power gain is also high.

Common Emitter Configuration

In this configuration the *i*/*p* is given to the base and *o*/*p* is observed at the collector. Here $A_i = \frac{I_c}{I_b}$. Since $I_c >> I_b$ the current gain is high. Similarly $A_v = \frac{V_c}{V_b}$, i.e., $A_v = \frac{I_c R_c}{I_b R_b}$. Since $I_c >> I_b$ and $R_c >> R_e$, A_v is also high. With a high current gain and voltage gain, the power gain is also high. Due to this the CE-configuration is most preferred.

Common Collector Configuration

In this the input is given to the base and the output is taken at the emitter. Since the signal is transferred in the same junction there is no voltage amplification. Here $A_I = \frac{I_e}{I_b}$. Since $I_e >> I_b$, the current gain is high. Due to the high current gain the power gain is also high. In this configuration the output at the emitter is same as that at the base and so this circuit is also known as *emitter follower*.

2.7.3 Current Component of a Transistor

Let us discuss the current flowing through each terminal of a npn transistor when it is biased to operate in the normal mode.

Emitter Terminal The emitter being forward biased experiences current due to majority charge carriers, i.e., electrons from the emitter and holes from the base. The electron current in emitter region is represented as I_{ne} and the hole current base region as I_{pb}. Therefore, the total current through the emitter is $I_e = I_{ne} + I_{pb}$.

Base Terminal The base being an intermediate region is affected by both the forward and reverse bias applied at the junctions and hence the current is due to both majority and minority carriers. Part of the electron current from the emitter and the hole current from the base constitute the majority carrier current. Similarly, the current due to holes from the collector (I'_{pc}) and electrons from the base (I'_{nb}) constitute the minority current. Since the direction of these currents are opposite in nature the minority current component is considered to be negative. Therefore,

$$I_b = [1 - K]\, I_{ne} - I'_{nb} - I'_{pc} \tag{1}$$

Collector Terminal The charge carriers emitted by the emitter partly undergo a recombination at the base and the remaining charges reach the collector resulting in a majority current due to electrons. Since the CB junction is reverse biased the majority currents flow between the collector and base and so the total current is the sum of all the three, i.e.,

$$I_c = K\, I_{ne} + I'_{nb} + I'_{pc} \tag{2}$$

Adding Equation (1) and (2), we get

$$I_c + I_b = I_{ne} + I_{pb} = I_e$$

The current gain α is defined as ratio between I_e and I_c, i.e.,

$$\alpha = I_e / I_c < 1$$

The current gain β is defined as the ratio between I_b and I_c, i.e.,

$$\beta = \frac{I_b}{I_c} >> 1$$

Now that we are familiar with the basics of transistor let us discuss the operation of a transistor under unbiased and biased conditions.

2.7.4 Unbiased Transistor

As discussed with respect to diodes, a depletion region is created in the transistor also in both the junctions due to the difference in the concentration in the three regions. Since the doping levels in each region is different the width of the depletion region is not the same in all the regions. The width is more in the lightly doped region, compared to the heavily doped region, i.e., it is more in the base region compared to the emitter and collector regions. Thus in the transistor also a depletion potential is developed across the junctions under unbiased condition.

Base Width Modulation Before we go on to discuss about a biased transistor let us see what *Base width modulation* or *Early effect* means. This effect was discovered by the scientific name *EARLY* and it tells us about the variation in the width of the base region with respect to the applied potential at the CB junction. We are already aware of the fact that the width of the depletion region decreases with forward bias and the increases with reverse bias. In a transistor, the EB junction is forward biased and so the variation of the depletion layer width is negligible whereas in the CB junction, the reverse bias has an appreciable effect. The width of the depletion region increases with respect to reverse bias and the penetration of the depletion layer is deeper in the lightly doped region compared to the heavily doped region and so the effective width of the base region reduces. This variation in the base width due to the applied reverse bias at the CB junction is known as *Base width modulation.*

Effect of Base Width Modulation

1. Chances for recombination is less and so the base current reduces.
2. The charge concentration near the EB junction is high and so the diffusion of charges into the emitter region increases resulting in an increased I_e, I_c and current gain, α.
3. When the reverse bias is increased to a larger value the effective base width reduces to zero thereby causing a voltage breakdown in the device. This is known as *Punch through effect*.

Now let us see how a transistor functions under normal biasing conditions in the entire three configurations.

2.8 CHARACTERISTICS OF A TRANSISTOR (CE/CB/CC)

Common Base Configuration In CB Configuration, Base is common to both input and output. To understand the operation of a transistor in these configurations it is preferable to learn the characteristics. The input characteristics relate I_i and V_i for a constant V_o and the output characteristics relate I_o and V_o for a constant I_i.

In CB Configuration the input characteristics relate I_E and V_{EB} for a constant V_{CB}. Initially let $V_{CB} = 0$ then the input junction is equivalent to a forward biased diode and the characteristics resembles that of a diode. Where $V_{CB} = + V_1$ (volts) thus due to early effect I_E increases and so the characteristics shifts to the left.

The output characteristics relate I_C and V_{CB} for a constant I_E. Initially I_C increases and then it levels for a value $I_C = \alpha I_E$. When I_E is increased I_C also increases proportionality. Though increase in V_{CB} causes an increase in α, since α is a fraction, it is negligible and so I_C remains a constant for all values of V_{CB} once it levels off.

Common Emitter Configuration Here emitter is common to both input and output. The input characteristics relate I_B and V_{BE} for a constant V_{CE}. When V_{CE} is 0 V the transistor operates like a forward biased diode. When V_{CE} is increased, due to base width modulation I_B decreases and the graph shifts to the right.

The output characteristics relate I_C and V_{CE} for a constant I_B. For a particular value of I_B, I_C increases lunarly with V_{CE} and levels off after some time based on the relation $I_C = \beta I_B$. As V_{CE} increases its effect on α is less but $\beta = \frac{\alpha}{1-\alpha}$ has an appreciable change. So but due to early effect an increase in V_{CE} causes an appreciable increase in β and thus on I_C. So the current increases with V_{CE} making the characteristics slanting rather than a straight line as in CB configuration.

Common Collector Configuration Here, I_B vs V_{BC} is dealt for the input characteristics and I_E vs V_{EC} is dealt for the output characteristics. It is obvious that it is merely interchanging the emitter and collector terminals, and so the characteristics are similar to that of Common Emitter characteristics.

Applications

1. Amplification
2. Modulation
3. Waveform generation
4. Switching, etc.

Experiment (Transistor Characteristics)

Aim: ***To Plot the Transistor Characteristic of Common-Emitter Configuration and to Find the h-Parameters for the Same***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	2
Ammeter	(0-10) mA, (0-1) mA-1	1
Voltmeter	(0 -30) V	1
	(0-2) V	1

Circuit Diagram:

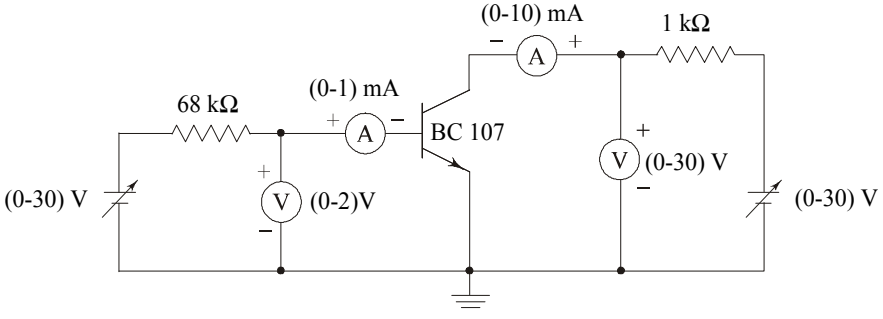


Fig. 2.18

Procedure

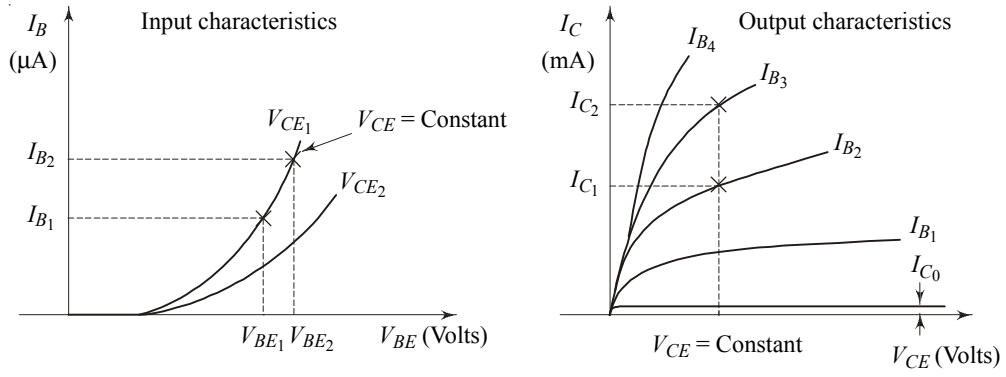
I. Input Characteristic:

1. Rig up the circuit as per the circuit diagram.
2. Set V_{CE} = 5 V (say), vary V_{BE} insteps of 0.1V and note down the corresponding I_B. Repeat the above procedure for 10 V, 15 V etc.
3. Plot the graph: V_{BE} *vs* I_B for a constant V_{CE}.
4. Find the *h*-parameters: (a) h_{fe}: forward current gain.
   (b) h_ie: input impedance.

II. Output Characteristic:

1. Rig up the circuit as per the circuit diagram.
2. Set $I_B = 20\mu$A (say), vary V_{CE} insteps of 1V and note down the corresponding I_C. Repeat the above procedure for 40 μA, 80 μA, etc.
3. Plot the graph: V_{CE} Vs I_C for a constant I_B.
4. Find the h-parameters: (a) h_{oe}: output admittance
   (b) h_{re}: reverse voltage gain

Waveforms:



$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} = \frac{V_{BE_2} - V_{BE_1}}{I_{B_2} - I_{B_1}} \qquad h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}}$$

$$h_{re} = \left.\frac{\Delta V_{BE}}{\Delta V_{CE}}\right|_{I_B\ =\ \text{constant}} = \frac{V_{BE_2} - V_{BE_1}}{V_{CE_2} - V_{CE_1}} \qquad h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B\ =\ \text{constant}} = \frac{I_{C_2} - I_{C_1}}{V_{CE_2} - V_{CE_1}}$$

Fig. 2.19

Tabular Column:

Input Characteristic: V_{CE} Constant

V_{BE} (Volts)	I_B (μA)

Output Characteristic: I_B Constant

V_{CE} (Volts)	I_C (mA)

Result:

Parameters	Practical Readings
h_{fe} h_{ie} h_{re} h_{oe}	

Experiment (Transistor Characteristics)

Aim: ***To Plot the Transistor Characteristic of Common-Collector Configuration and to Find the h-Parameters for the Same***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	2
Ammeter	(0-10) mA (0-1) mA	1
Voltmeter	(0-30) V	1
	(0-2) V	1

Circuit Diagram:

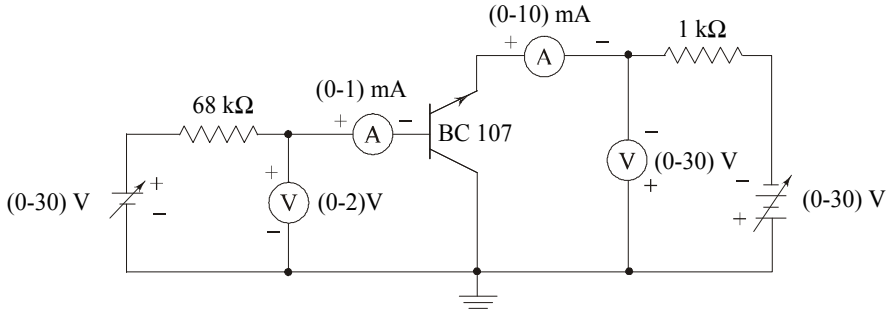


Fig. 2.20

Procedure:

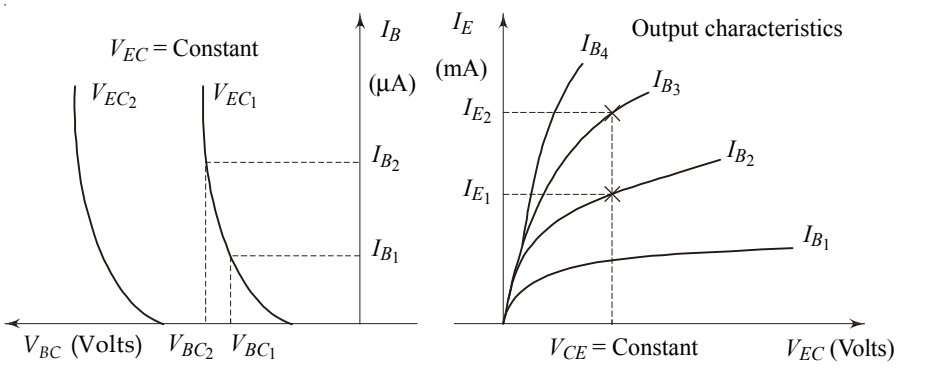
I. Input Characteristic:

1. Rig up the circuit as per the circuit diagram.
2. Set V_{EC} = 5 V (say), vary V_{BC} insteps of 0.1 V and note down the corresponding I_B. Repeat the above procedure for 10 V, 15 V, etc.
3. Plot the graph: V_{BC} vs I_B for a constant V_{EC}.
4. Find the h-parameters: a. h_{fc}: forward current gain
   b. h_{ic}: input impedance

II. Output Characteristic:

1. Rig up the circuit as per the circuit diagram.
2. Set $I_B = 20\mu$A (say), vary V_{EC} insteps of 1V and note down the corresponding I_E. Repeat the above procedure for 40 μA, 80 μA, etc.
3. Plot the graph: V_{CE} vs I_C for a constant I_B.
4. Find the h-parameters: a. h_{oc}: output admittance
   b. h_{rc}: reverse voltage gain

Waveforms:



$$h_{ic} = \left.\frac{\Delta V_{BC}}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} = \frac{V_{BC_2} - V_{BC_1}}{I_{B_2} - I_{B_1}} \qquad h_{fc} = \left.\frac{\Delta I_E}{\Delta I_B}\right|_{V_{EC}\ =\ \text{constant}} = \frac{I_{E_2} - I_{E_1}}{I_{B_2} - I_{B_1}}$$

$$h_{rc} = \left.\frac{\Delta V_{BC}}{\Delta V_{CE}}\right|_{I_B\ =\ \text{constant}} = \frac{V_{BC_2} - V_{BC_1}}{V_{CE_2} - V_{CE_1}} \qquad h_{oc} = \left.\frac{\Delta I_E}{\Delta V_{EC}}\right|_{I_B\ =\ \text{constant}} = \frac{I_{E_2} - I_{E_1}}{V_{EC_2} - V_{EC_1}}$$

Fig. 2.21

Tabular Column:

Input Characteristics: V_{EC} Constant

V_{BC} (Volts)	I_B (μA)

Output Characteristics: I_B Constant

V_{EC} (Volts)	I_E (mA)

Result:

Parameters	Practical Readings
h_{fc}	
h_{ic}	
h_{rc}	
h_{oc}	

Experiment (Transistor Characteristics)

Aim: ***To Plot the Transistor Characteristic of Common-Base Configuration and to Find the h-Parameters for the Same.***

Equipement Required:

Equipment	Range	Quantity
Power supply	(0-30) V	2
Ammeter	(0-10) mA	2
Voltmeter	(0-30) V	1
	(0-2) V	1

Circuit Diagram:

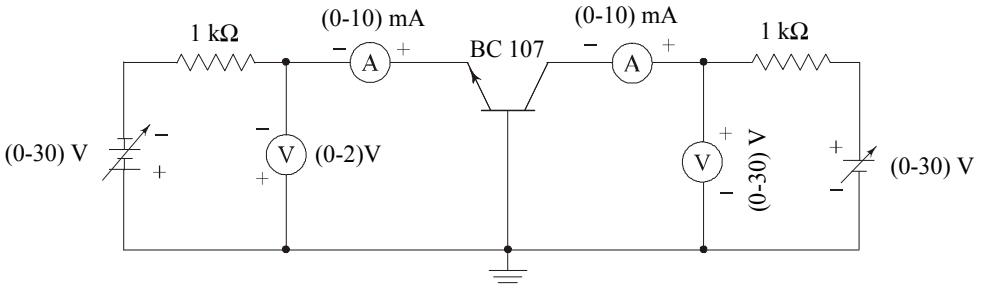


Fig. 2.22

Procedure:

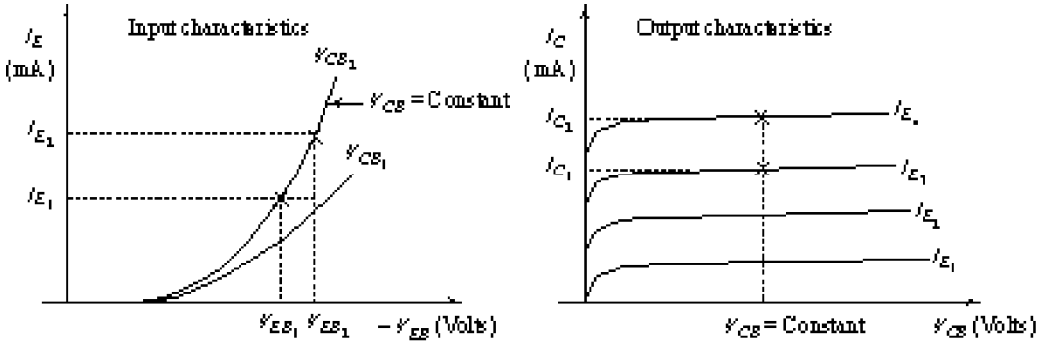
I. Input Characteristic:

1. Rig up the circuit as per the circuit diagram.
2. Set V_{CB} = 5 V (say), vary V_{EB} insteps of 0.1 V and note down the corresponding I_E. Repeat the above procedure for 10 V, 15 V, etc.,
3. Plot the graph: V_{EB} vs I_E for a constant V_{CB}.
4. Find the *h*-parameters: (a) h_{fb}: forward current gain
   (b) h_{ib}: input impedance

II. Output Characteristic:

1. Rig up the circuit as per the circuit diagram.
2. Set I_E = 2 mA (say), vary V_{Cb} insteps of 1 V and note down the corresponding I_C. Repeat the above procedure for 4 mA, 6 mA, etc.
3. Plot the graph: V_{CB} vs I_C for a constant I_E.
4. Find the *h*-parameters: (a) h_{ob}: output admittance
   (b) h_{rb}: reverse voltage gain

Waveforms:



$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}\bigg|_{V_{CB}\,=\,\text{constant}} = \frac{V_{EB_2} - V_{EB_1}}{I_{E_2} - I_{E_1}} \qquad h_{fb} = \frac{\Delta I_C}{\Delta I_E}\bigg|_{V_{CB}\,=\,\text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{E_2} - I_{E_1}}$$

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}\bigg|_{I_E\,=\,\text{constant}} = \frac{V_{EB_2} - V_{EB_1}}{V_{CB_2} - V_{CB_1}} \qquad h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}\bigg|_{I_E\,=\,\text{constant}} = \frac{I_{C_2} - I_{C_1}}{V_{CB_2} - V_{CB_1}}$$

Fig. 2.23

Tabular Column:

Input Characteristics: V_{CB} Constant

V_{EB} (Volts)	I_E (mA)

Output Characteristics: I_E Constant

V_{CB} (Volts)	I_C (mA)

Result:

Parameters	Practical Readings
h_{fb} h_{ib} h_{rb} h_{ob}	

2.9 TRANSISTOR AS A SWITCH

The transistor can be operated as a switch when it is operated in cut-off and saturation mode of operation.

Under conditions of cut-off, the transistor is like an open circuit and under conditions of saturation, the transistor is like a closed switch.

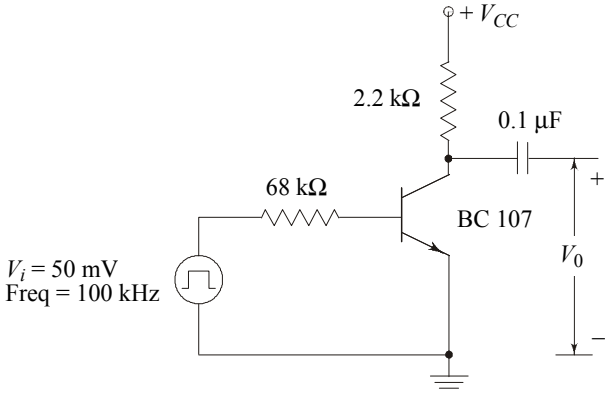


Fig. 2.24

When I_B is small or zero, the transistor is at cut-off and there is no drop across R_C. Since the current is zero, the transistor operates as an open switch. The collector voltage is almost equal to supply voltage (V_{CC}).

If I_B is increased from zero to a very high value, the transistor conducts fully and the drop across R_C is very high, approximately V_{CC}. Since the current is maximum, the transistor is equivalent to a closed switch. Thus by varying I_B between minimum and maximum values, the transistor can be operated as a switch.

Transistor at Cut-off

At cut-off, both emitter junction and collector junction is reverse biased. The cut-off in a transistor is defined by the condition, $I_E = 0$. Due to the small reverse current flowing in the reverse bias junction, I_C is not ideally zero, though $I_E = 0$.

Hence to achieve cut-off condition in a transistor, I_B is made zero and then the emitter-base junction is reverse biased slightly, if required.

$$I_C = \beta I_B + (1 + \beta)\, I_{CO}$$

When $$I_B = 0,\ I_C = \left(\frac{1}{1-\alpha}\right) I_{CO}$$

In germanium transistor, α is not zero under condition of cut-off, so $\left(\frac{1}{1-\alpha}\right)$ is quite large. Hence I_C is not negligible. To obtain $I_C = 0$, the emitter-base junction has to be reverse biased by 0.1 V. In silicon transistor, $\alpha = 0$ at cut-off and so $I_C = I_{CO}$ is small and negligible. Hence reverse biasing of emitter-base junction is not required in case of silicon transistor. It is sufficient if $I_B = 0$ mA to obtain cut-off condition.

The collector current under cut-off condition is designated as I_{CBO}. This is more than I_{CO} due to surface leakage current and avalanche multiplication effects in reverse bias junction. I_{CBO} depends on temperature and it doubles for every 10° rise in temperature of the junction.

Transistor in Saturation

If the voltage V_{BB} is increased to value above the cut-in level, the transistor conducts. As I_B increases further, I_E also starts increasing.

The large signal current gain, $h_{FE} = I_C / I_B$. As I_B increases, $I_C = h_{FE}\, I_B$ obtained at the collector also increases. Therefore, $V_{CE} = V_{CC} - I_C R_C$ decreases.

Since V_{CE} is low, V_{CB} is also low. As V_{CE} decrease, V_{CB} also decreases and becomes zero. If V_{CE} decreases further, V_{CB} decreases in the negative direction which results in forward biasing the collector-base junction, i.e., under this condition, base is at a higher positive potential than the collector and the transistor is said to be in saturation as both junctions are forward biased.

Experiment (Transistor Switch)

Aim: ***Study the Switching Characteristics of a Transistor***

1. Rise time
2. Fall time
3. ON/OFF time
4. Delay time

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1
Power supply	(0-30) V	1

Circuit Diagram:

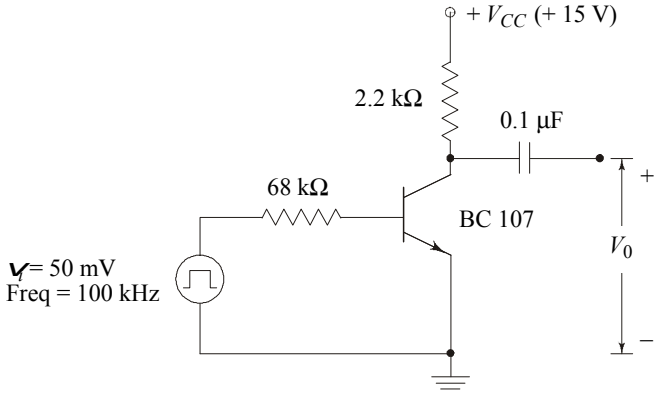


Fig. 2.25

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input signal (say 50 mV, 100 kHz), using a signal generator.
3. Observe the output at the collector of the transistor using a CRO (AC-mode).
4. Note down the parameters listed above and plot it on a graph.

Waveform:

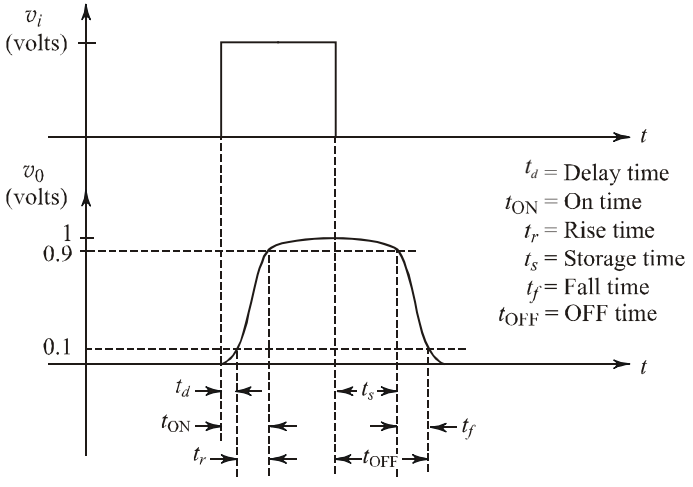


Fig. 2.26

Result:

Parameters	Practical Readings
Rise time	
Fall time	
ON/OFF time	
Delay time	

2.10 FIELD-EFFECT TRANSISTOR

This is an uni-polar device in which the conduction is due to majority carriers alone. This is a three terminal device in which the field or potential at the third terminal controls the current flow between the first two terminals. Hence the name *Field-effect transistor*. This is categorized into two types depending on the construction as JFET and MOSFET. Depending on the channel material, it is further classified as *n*-channel FET and *p*-channel FET. Before we discuss the other features, let us compare certain features of a BJT and FET.

Comparison With BJT:

1. It is uni-polar while BJT is bi-polar.
2. It is simpler to fabricate and it occupies less space in the IC.
3. Due to reverse biased input junction, the device offers high input impedance compared to BJT.
4. Less noisy.

2.10.1 Junction Field Effect Transistor

Construction Depending on the channel material, the semiconductor is chosen for, e.g., if it is a *n*-channel FET, we choose a *n*-type semiconductor bar from which the source and drain terminals are pulled out from either sides. The majority charges enter the device through the source terminal and leave the device through the drain terminal. On either sides of the semiconductor bar a high concentration of *p*-type impurities are diffused and the regions are shorted to get a terminal named gate. The source terminal is always forward biased with respect to drain and the gate is reverse biased with respect to source.

Characteristics The operation of the device can be clearly understood by discussing the output characteristics and the transfer characteristics. The static output characteristic deals with the variation of I_D with respect to V_{DS} for a constant V_{GS}. Initially assume that V_{GS} is 0 V. Then for a small applied voltage V_{DS}, the device acts like a resistor and the current increases linearly with the voltage. With an increase in current an unequal ohmic drop results. The drop is more near the drain compared to the source due to the reverse bias there and so the channel region gets restricted resulting in a constant current flow. The voltage at which the current levels-off is known as the *Pinch-off voltage*. If V_{DS} is increased further the reverse voltage at the drain region increases resulting in a breakdown. Thus the device operates in three regions, i.e., as a resistor in the variable resistance region, as a constant current device in the active region and finally, the breakdown region in which the device collapses.

If now a gate voltage is applied, the depletion region widens. The penetration is more near the drain region and less near the source region and thereby the effective channel width reduces which reduces the amount of charges moving from the source to the drain, thereby decreasing the I_D. The pinch-off and breakdown occur at an earlier stage due to the increased overall reverse bias. Thus as the gate bias is increased the channel width is reduced and I_D decreases.

Transfer Characteristics This relates the V_{GS} and I_D for a constant V_{DS}. When $V_{GS} = 0$, then for a particular value of V_{DS}, I_D is maximum. As V_{GS} is increased due to the reduction in the effective channel width, I_D decreases and finally becomes zero at which the device is said to be at cut-off. These characteristics can be obtained for different values of V_{DS}.

Application

1. Amplifiers
2. Switches, etc., for better performance compared to BJT.

2.10.2 Metal Oxide Semiconductor Field Effect Transistor or Insulated Gate Field Effect Transistor [MOSFET or IGFET)

The metal oxide semiconductor FET is a combination of a metal, dielectric and a conductor forming the device. This is classified into Enhancement MOSFET and Depletion MOSFET depending on the mode of operation. It is further classified as *n*-channel MOSFET and *p*-channel MOSFET depending on the channel material.

Construction Consider an *n*-channel MOSFET in which the substrate is of *p*-channel with a very light doping. Diffusing *n*-type impurities into the substrate creates the drain and source. A layer of silicon-dioxide, which acts as the dielectric medium, is coated over the semiconductor. Over this a metal area is constructed and the gate terminal is brought out of it. The metal area in conjunction with the insulating dielectric oxide layer and the semiconductor channel forms a parallel plate capacitor. When a gate potential is given, charges are induced on either of the dielectric resulting in conduction. Let us now discuss the operation of the MOSFET in both the modes of operation.

Enhancement MOSFET Here the source and drain terminals are formed as explained above. The channel in between these terminals is not formed physically, i.e., the channel is created due to the induced charge carriers when a suitable gate potential is applied. In an *n*-channel MOSFET, when the gate voltage is positive, negative charge carriers are induced into the semiconductor thereby forming a channel between the source and the drain. The width of the induced channel depends on the amount of charges induced which in turn depends on the gate voltage applied. Thus when the gate potential is low, less charges are induced resulting in a channel of less width and hence the drain current is low. When the gate voltage is increased, more charges are induced thereby increasing the channel width and the drain current is low. When the gate voltage is increased, more charges are induced thereby increasing the channel width and the drain current is enhanced or increased. Since the drain current is enhanced with respect to the gate potential, this is known as *Enhancement MOSFET*. When a voltage is applied between the source and the drain as in a JFET, initially there is a rise in I_D and after the pinch-off voltage, I_D levels off.

Depletion MOSFET Here, the channel is physically existing, i.e., it is diffused during the manufacture and not induced during the process as in the other type. This MOSFET can be operated both as Enhancement MOSFET and Depletion MOSFET depending on the gate voltage. For an *n*-channel MOSFET, if the gate voltage is positive, the induced charges are negative which operates the device in the enhancement mode. If the gate voltage is negative, the induced charges are positive and it results in recombination in the channel region, which depletes the availability of free charges for conduction and so, the drain current decreases. Thus, as the negative voltage at the gate terminal is increased, the drain current decreases. It is clear from the above discussion that the device can be operated in either of the modes depending on the

gate potential. The same discussion holds good for the *p*-channel MOSFET also with appropriate gate potential for both the modes of operation.

Experiment (Field-Effect Transistor)

Aim: ***To Plot the Drain and Transfer Characteristic for the Given FET and to find the Drain Resistance and Transconductance***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	2
Ammeter	(0-30) mA	1
Voltmeter	(0-30) V	2

Circuit Diagram:

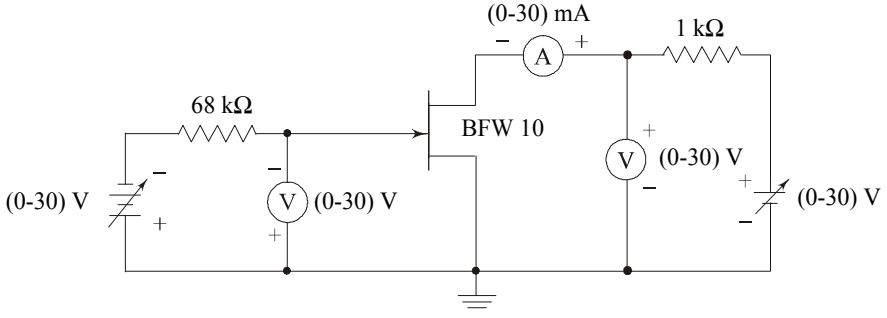


Fig. 2.27

Procedure:

Drain Characteristic:

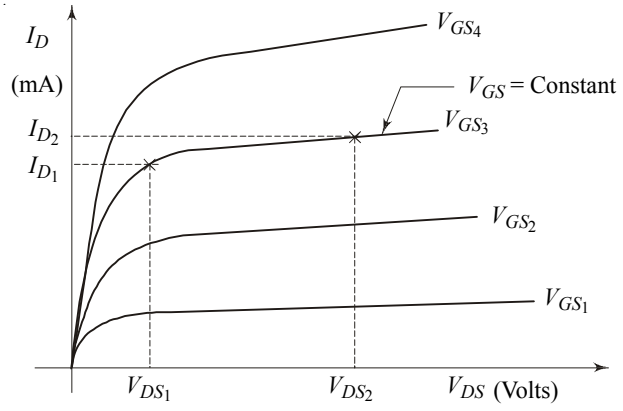
1. Rig the circuit as per the circuit diagram.
2. Set gate voltage V_{GS} = –1 V, vary drain voltage V_{DS} in steps of 1 V and note down the corresponding drain current, I_D.
3. Repeat the above procedure for V_{GS} = 0 V, + 1 V, etc.
4. Plot the graph: V_{DS} vs I_D for a constant V_{GS}.
5. Find the drain resistance, $r_D = \Delta V_{DS} / \Delta I_D$.

Transfer Characteristics:

1. Rig the circuit as per the circuit diagram.
2. Set drain voltage V_{DS} = + 5 V, vary gate voltage V_{GS} in steps of 1 V (negative voltage) and note down the corresponding drain current, I_D.
3. Repeat the above procedure for V_{DS} = + 10 V, + 15 V, etc.
4. Plot the graph: V_{GS} vs I_D for a constant V_{DS}.
5. Find the trans-conductance, $g_m = \Delta I_D / \Delta V_{GS}$.

Waveforms:

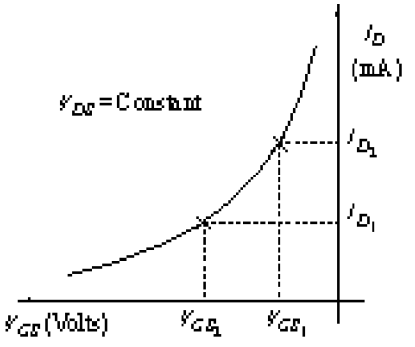
Drain Characteristics:



$$r_D = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}\,=\,\text{constant}} = \frac{V_{DS_2} - V_{DS_1}}{I_{D_2} - I_{D_1}}$$

Fig. 2.28

Transfer Characteristic:



$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\bigg|_{V_{DS}\,=\,\text{constant}} = \frac{I_{D_2} - I_{D_1}}{V_{GS_2} - V_{GS_1}}$$

Fig. 2.29

Tabular Column:

Drain Charactristics: V_{GS} Constant

V_{DS} (Volts)	I_D (mA)

Transfer Characteristics: V_{DS} Constant

V_{GS} (Volts)	I_D (mA)

Result:

Parameters	Practical Readings
r_D g_m $\mu = g_m \times r_D$	

2.11 UNI-JUNCTION TRANSISTOR

This is a three terminal, single or uni-junction semiconductor device. The uni-junction transistor (UJT) finds its main application in switching circuit, where rapid discharge of the capacitor is desired.

Construction This consists of an *n*-type semiconductor bar, which is lightly doped. Two terminals base1 and base2 are taken out from the upper and lower end of the bar. A heavily doped *p*-region is diffused into the *n*-type bar, which results in a *pn*-junction. A terminal is taken out of this region and named as emitter. The emitter is always forward biased with respect to the base 1. Base 2 is kept at a higher positive potential with respect to base 1.

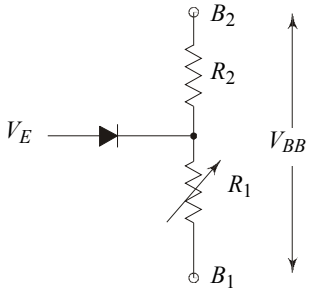


Fig. 2.30

Equivalent Circuit The *n*-type semiconductor bar is similar to a fixed resistor between emitter and base 2, and is equivalent to a variable resistor between emitter and base 1. Since the resistance of base 1 region varies with the conduction of devices, it is represented as the variable resistance. The *pn*-junction is represented as a diode.

Operation When a voltage V_{bb} is applied to the base terminals a drop appears across the internal resistance as follows.

Drop across the resistor between emitter & base 2 (R_2) = $V_2 = V_{BB} R_2 / (R_1 + R_2)$. Similarly, the drop across resistor, R_1 is $V_1 = V_{BB} R_1 / (R_1 + R_2)$. The ratio of the internal resistors is defined as the *Intrinsic stand-off ratio*, η, so the $V_1 = \eta V_{BB}$. Due to the existing *pn*-junction, a depletion potential is created and when a voltage is given to the device at the emitter terminal, the device does not conduct till the emitter voltage, *Vee* exceeds the sum of the depletion potential and the drop across R_1, i.e., $V_{EE} > V_d + V_1$. If $V_{EE} < V_d + V_1$, the emitter-base junction is considered to be reverse biased and so the device is in the off-state.

When $V_{EE} > V_d + V_1$, then the EB_1 junction is forward biased and holes move from the heavily doped emitter region into the base 1 region resulting in a large amount of current. Due to the sudden increase in the charge concentration in the base 1 region, its conductivity is increased or the resistivity is decreased, which results in a voltage drop across B_1. This region in which there is a decrease in voltage for an increased current is known as the *Negative resistance region*, and the device is said to be in the ON state. With further increase in the emitter voltage, the emitter current also increases as in case of a *pn*-junction diode resulting in the saturation region. Thus the device operates in 3 regions, i.e., at cut-off region while in the off-state and negative resistance region and saturation region in the ON state.

Applications

1. Pulse generator for firing SCR.

2. In the negative resistance region, it can be operated as a relaxation oscillator.
3. Used as a fast acting switch.
4. Used as sine wave generator, square wave generator, saw-tooth generator.
5. Used in time delay circuits.

Experiment (Uni-Junction Transistor)

Aim: ***To Plot the Characteristics of a Given UJT.***

Circuit Diagram:

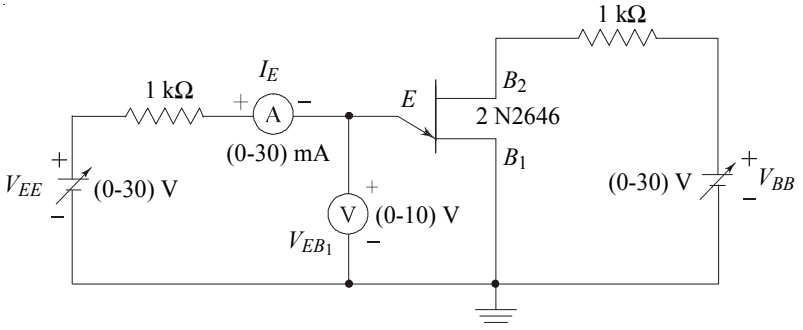


Fig. 2.31

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	2
Ammeter	(0-30) mA	1
Voltmeter	(0-30) V	1

Procedure:

1. Rig up the ckt as per the circuit diagram.
2. Set V_{BB} = 10 V.
3. Vary V_{EE} and note down the readings of V_{EB1} & I_E.
4. Plot the graph: V_{EB1} vs I_E for a constant V_{BB}
5. Determine the intrinsic stand-off ratio

$$\eta = \frac{V_P - V_D}{V_{BB}}$$

Waveforms:

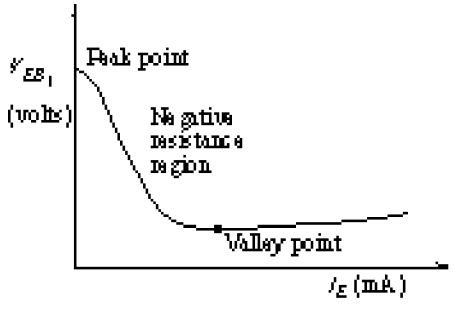


Fig. 2.32

Tabular Column:

V_{BB} is constant:

I_E (mA)	V_{EB1} (volts)

Result:

Parameters	Practical Readings
η	

2.12 SILICON CONTROLLED RECTIFIER

The four layer devices are three junction, four terminal semiconductor devices. The terminals are anode, cathode, anode gate and cathode gate. The doping of the anode and cathode layers are high while that of the gate regions are low. The anode is always at a higher positive potential than the cathode. This forward biases the outer junctions J_1 & J_3 while the inner junction J_2 is reverse biased. Due to the presence of a reverse biased junction in series no current other than a small amount of minority current flows through the device.

When the applied potential is increased the forward bias at the outer layers and the reverse voltage at the inner layer increase resulting in avalanche multiplication. The potential at which the breakdown occurs is known as *breaking potential or firing potential*. Since breakdown occurs there is a large increase in current through the device and hence a decreased resistance and voltage across the device. With further increase in the anode potential, the current increases with respect to the applied voltage. Thus the device is in the cut-off region or in the off state before the breakdown potential and after V_{BO}, it is in the ON state, initially, entering the negative resistance region and then operating in the saturation region.

A voltage applied at the gate terminal can control the breakdown voltage. Such a device in which either of the gate terminals are used to control the operation of the device is called a SCR (*Silicon Controlled Rectifier*). The gate terminal is forward biased with respect to cathode and when a gate potential is given, the inner junction is forward biased and introduction of the gate current decreases the break over voltage thereby turning ON the SCR at a earlier stage. Thus the gate terminal is used to control the turn ON of the SCR. Once the SCR is ON, the gate loses control and only reducing the anode to cathode voltage can put off the device.

2.12.1 Two Transistor Analogy of a SCR

Consider the *pnp* and npn transistor connected back to back. The transistor Q_1 feeds Q_2 and Q_2 in turn feeds Q_1. Thus when the bias is given the current through the devices increase in a cumulative fashion resulting in a very large amount of current driving the transistors to saturation. Consider the following analysis,

Let the collector current of Q_1 be $I_{C1} = \alpha_1 I_{E1} + I_{CO1}$

Collector current of Q_2 be $I_{C2} = \alpha_2 I_{E2} + I_{CO2}$

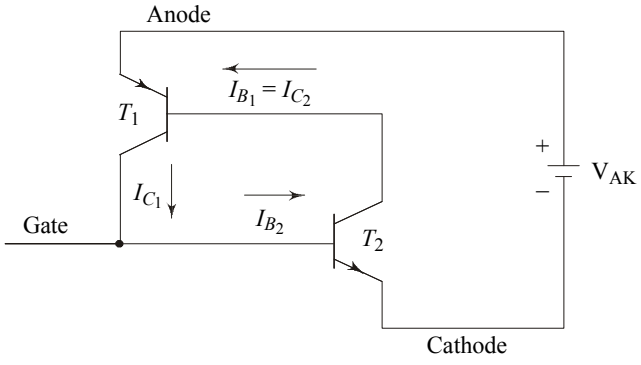


Fig. 2.33

Therefore, the total current in the circuit is $I_C = I_{C1} + I_{C2}$

Assuming $I_{C1} + I_{C2} = I_E$ and $I_{E1} = I_{E2} = I_E$.

Adding the above equations, we get

$$I_{C1} + I_{C2} = I_E = I_E[\alpha_1 + \alpha_2] + I_{CO1} + I_{CO2}$$

$$I_E = \frac{I_{C01} - I_{C02}}{1 - (\alpha_1 - \alpha_2)}$$

From the equations, it is obvious that when the sum of the current gains, $\alpha < 1$, then the emitter current (I_E) is finite but when $\alpha = 1$, then the I_E is infinite. Thus at cut-off the factor $[\alpha_1 + \alpha_2] < 1$ and this is possible only in silicon material and so all the four layer devices are manufactured using silicon. Initially when the voltage is given, the gain is low. With increase in voltage the gain increases due to avalanche multiplication and when $[\alpha_1 + \alpha_2] = 1$, break over occurs resulting in an even more increased current. Introduction of gate current increases the gain α and so the break over occurs at an earlier stage.

Operation of a SCR Under Reverse Bias When a reverse voltage is applied to a SCR, the outer layers are reverse biased and the inner layers are forward biased and there is no possibility of current flowing through the device. When the reverse voltage is increased beyond a certain value, the device breaks down resulting in a sharp current for a particular voltage. Thus it is clear that the device operates in one direction only and so it is unidirectional and hence can be used in controlled rectification. Thus a SCR is called a silicon controlled rectifier since it is made out of silicon and is used for controlled rectification.

Experiment (Silicon Controlled Rectifier)

Aim: ***To Find the Latching and Holding Current for a Given SCR***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	2
Ammeter	(0-30) mA	2
Voltmeter	(0-30) V	1

Circuit Diagram:

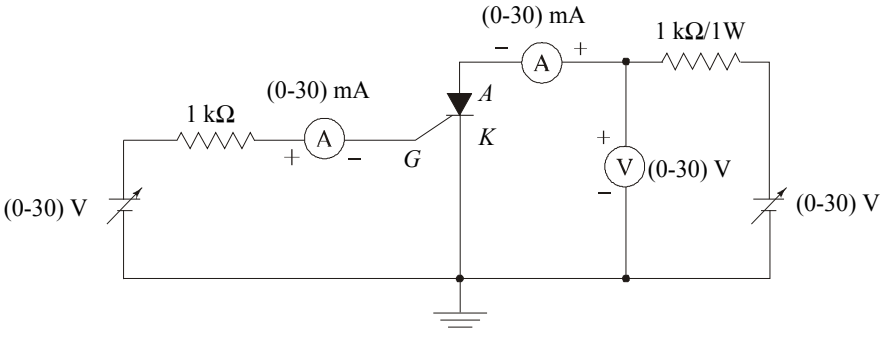


Fig. 2.34

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set gate current I_G equal to firing current, vary anode to cathode voltage, V_{AK}, in steps of 0.5 V and note down the corresponding anode current, I_A.
3. V_{BO} is the point where voltage (V_{AK}) suddenly drops and there is a sudden increase in anode current I_A.
4. Note down the current at that point called latching current.
5. Increase the V_{AK} in steps of 1 V till its maximum.
6. Open the gate terminal and decrease the V_{AK}.
7. Holding current is the current below which the deflection in both voltmeter (V_{AK}) and ammeter (I_A) suddenly reduces to zero.

Holding current is the minimum current that a SCR can maintain its on condition. Holding current is always less than latching current.

Waveforms:

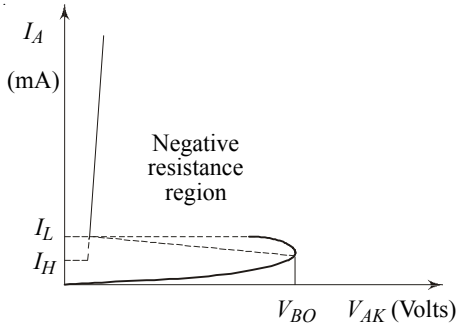


Fig. 2.35

Tabular Column:

V_{AK} (Volts)	I_A (mA)

Result:

Parameters	Practical Readings
V_{BO}	
I_L	
I_H	

2.13 LIGHT EMITTING DIODE (LED)

A *pn* junction diode, which emits light on forward biasing, is known as a light emitting diode. The emitted light may be either in the visible range or the invisible range, and the intensity of light depends on the applied potential.

Principle In a *pn* junction charge carrier recombination takes place when the electrons cross from the *n*-layer to the *p*-layer. The electrons are in the conduction band on the *p*-side while holes are in the valence band on the *p*-side. The conduction band has a higher energy level compared to the valence band and so when the electron recombines with a hole the difference in energy is given out in the form of heat or light. In case of silicon or germanium, the energy dissipation is in the form of heat, whereas, in case of gallium-arsenide and gallium-phosphide, it is the form of light. But this light is in the invisible region and so these materials cannot be used in the manufacture of LED. Hence gallium-arsenide phosphide which emits light in the visible region is used to manufacture an LED.

Construction An *n*-type layer is grown on a substrate and a *p*-type layer is grown over it by diffusion process. The *p*-layer is kept at the top because carrier recombination takes place in it. The terminals anode and cathode are taken out of the *n*- and *p*-layer respectively. The anode connections are made at the edge in order to provide more surface area for the emission of light. A metal film is applied to the bottom of the substrate to reflect light to the surface of the device and also to provide connection for the cathode terminal. Finally the structure are provided with an encapsulation (cover) to protect them from destruction.

Advantages

1. Works on low voltage and current and hence consumes less power.
2. Requires no warm up time.
3. Can be switched ON and OFF at a faster rate.
4. Long lifetime.
5. Small size and less weight.

Applications

1. Infra red LEDs are used in burglar alarms.
2. Used in solid state video displays.
3. Used in the field of optical communication.
4. Used in image sensing circuits.
5. Used in numeric displays like watches, pocket calculators, etc.

In numeric displays, the LEDs are arranged as a seven-segment array. The desired digit is obtained by suitably biasing the required segments. e.g., if the digit required is 5 then the segments *a*, *f*, *g*, *c*, *d* are forward biased and the segment *b*, *e* are reverse biased so that the five segments glow depicting the digit 5.

2.14 PHOTO-DETECTORS

2.14.1 Photo Diode

A photo diode is a two terminal *pn* junction device, which operates on reverse bias. On reverse biasing a *pn* junction diode, there results a constant current due to minority charge carriers known as reverse saturation current. Increasing the thermally generated minority carriers by applying external energy, i.e., either heat or light energy at the junction can increase this current. When we apply light energy as an external source, it results in a photo diode that is usually placed in a glass package so that light can reach the junction. Initially when no light is incident, the current is only the reverse saturation current that flows through the reverse biased diode. This current is termed as the *dark current* of the photo diode. Now when light is incident on the photo diode then the thermally generated carriers increase resulting in an increased reverse current which is proportional to the intensity of incident light. A photo diode can turn on and off at a faster rate and so it is used as a fast acting switch.

Applications

1. Photo detector.
2. Optical communication systems.

2.14.2 Photo Transistor

It is a transistor with an open base, there exists a small collector current consisting of thermally produced minority carriers and surface leakage. By exposing the collector junction to light, a manufacturer can produce a *phototransistor,* a transistor that has more sensitivity to light than a photo diode.

Because the base lead is open, all the reverse current is forced into the base of the transistor. The resulting collector current is

$$I_{CEo} = \beta_{dc}\, I_R$$

The main difference between a phototransistor and a photodiode is the current gain, β_{dc}. The same amount of light striking both devices produces β_{dc} times more current in a phototransistor than in a photo diode.

Experiment (Photo-Detector)

Aim: ***Study of Photo-Detector's Characteristic***

1. light dependent resistor
2. photo-diode
3. photo-transistor

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	2
Ammeter	(0-10) mA	1
Voltmeter	(0-10) V	1

(0-30) V 1

Circuit Diagram:

Light Dependent Resistor

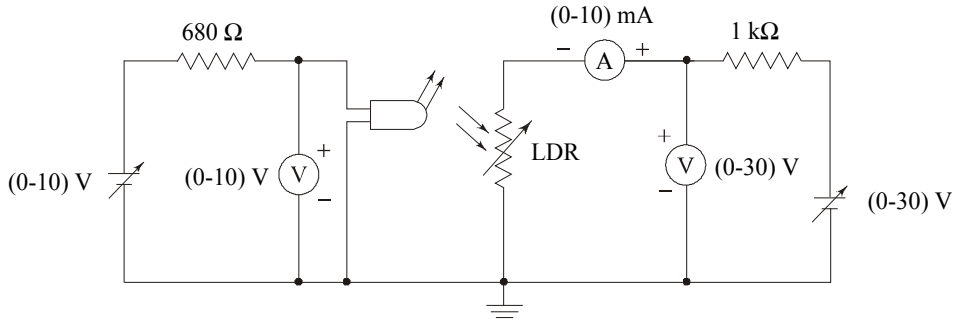


Fig. 2.36

Photo Diode:

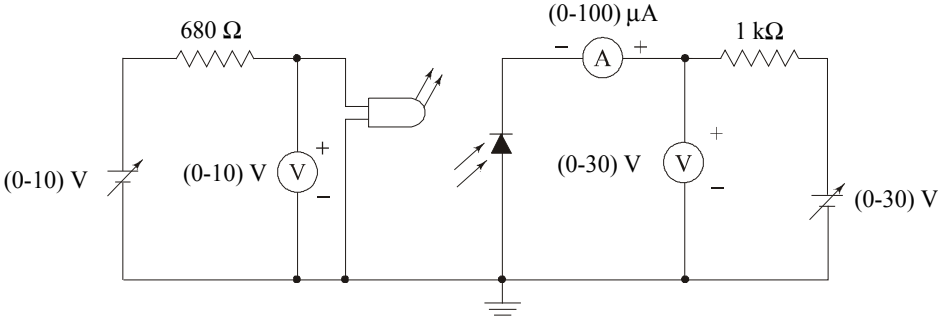


Fig. 2.37

Photo-Transistor

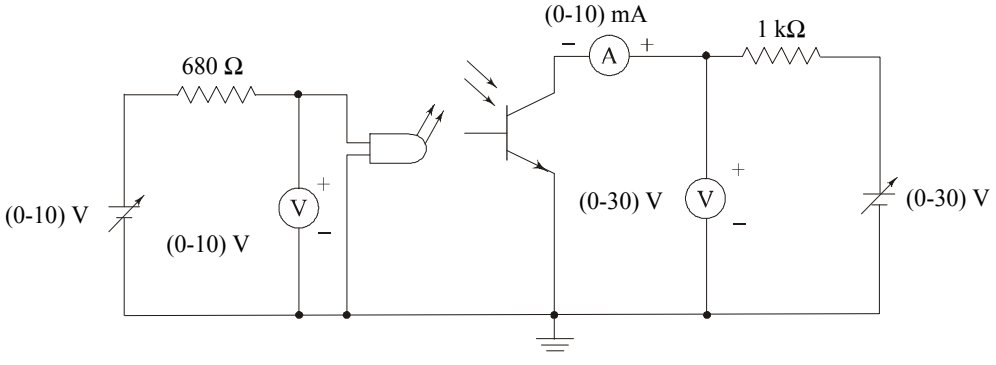


Fig. 2.38

Procedure:

Light Dependent Resistor:

1. Rig up the circuit as per the circuit diagram.
2. Maintain a known distance (say 5 cm) between the DC bulb and the LDR.

3. Vary the voltage of the bulb in steps of 1 V and note down the resistance value across the LDR using multimeter.
4. Plot the graph: V vs R.

Photo-Diode:

1. Rig up the circuit as per the circuit diagram.
2. Maintain a known distance (say 5 cm) between the DC bulb and the photo-diode.
3. Set the voltage of the bulb (say, 2 V), vary the voltage of the diode in steps of 1 V and note down the corresponding diode current, I_r.
4. Repeat the above procedure for V_L = 4 V, 6 V, etc.
5. Plot the graph: V_D vs I_r for a constant V_L.

Waveform:

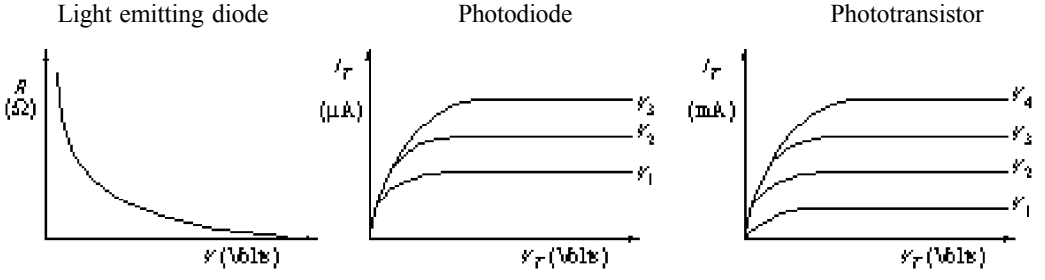


Fig. 2.39

Repeat the photo-diode experimental procedure for photo-transistor also.

2.15 VOLTAGE REGULATOR

Voltage regulators are electronic circuitaries, which counteract the variation due to load fluctuation. The heart of a voltage regulator is a zener diode. Since zener diode maintains constant voltage irrespective of their current after breakdown, regulation of voltage can be made available.

Zener Diode The zener diode is specially designed to operate in the reverse biased condition. It is already seen that in the reverse biased condition the diode breaks down beyond a particular voltage known as the *Breakdown voltage* and it offers a constant voltage thereafter for a large variation in the current. Hence a zener diode is particularly used as a voltage regulator. The breakdown voltage of the zener can be varied with respect to the doping concentration, i.e., the breakdown voltage decreases with increase in doping concentration.

Voltage regulators are broadly divided into two main types.

1. Shunt voltage regulator.
2. Series voltage regulator.

2.15.1 Shunt Voltage Regulator

A shunt voltage regulator provides regulation by shunting current away from the load to regulate the output voltage. In shunt regulator, the regulating device is in shunt or parallel with the load. The zener diode is a regulating device, which is connected in parallel with the load. The variation in output may occur due to variation in the input or in the load. The

regulation for the first condition is line regulation and for the second case is load regulation. Now we shall discuss both the types of regulation using a zener diode operated in the breakdown region.

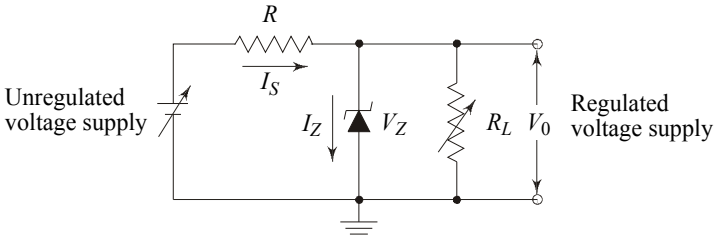


Fig. 2.40

Line Regulation The zener being operated in the breakdown region offers a constant breakdown voltage V_z across it and since it is in shunt with the load, the load voltage is also V_z. We assume that the input voltage varies between V_{in} (min) and V_{in} (max). The current from the input $I_s = (V_{in} - V_z)/R_s$ flows through the load and zener. If the load is assumed to be a constant then the decrease or increase in the input current due to variations in the input voltage passes through the zener since the load current is fixed. As long as the diode is in the breakdown region for any change in the current through it the voltage is still V_z and so the load voltage remains unaffected. Thus the regulation occurs here.

Mathematical Analysis It is clear that the regulation occurs due to the constant breakdown voltage offered by the zener and so the variation in the line voltage or the load resistance should maintain the diode in the breakdown region. So let us see what are limits of V_{in} that would operate the diode in the breakdown region. To determine V_{in} (min):

we know $$V_z = V_o = V_{in}(\text{min})\ R_L / (R_s + R_L)$$

$$V_{in}(\text{min}) = (R_s + R_L)V_o / R_L$$

To Determine V_{IN} (max):

$$V_{in}(\text{max}) = V_s\ (\text{max}) + V_z = I_s\ (\text{max})\ R_s + V_z + [I_z\ (\text{max}) + I_L]\ R_s + V_z$$

Load Regulation Assume that the input is fixed but there is variation in the load resistance. Since the input is fixed the input current is a constant but due to varying load the I_L varies and hence the zener current varies. Though there is a variation in the load current, there is no variation in the load voltage since $V_L = V_z$ and V_z is a constant for I_{min} and I_{max} in the breakdown region. If the load is minimum, the current through it is maximum and the current through the zener is minimum. Similarly, if the load is maximum, then the current through the load is minimum and that through the diode is maximum. As long as the current through the diode is within the limits, the diode is operated in the breakdown region and the voltage is regulated. Now let us discuss the minimum and maximum range of R_L that would maintain the diode in the breakdown region.

To determine the minimum value of R_L:

When R_L is minimum, I_L is maximum and I_z is minimum, so

$$V_o = V_z = V_{in}\ R_L\ (\text{min})/R_s + R_L(\text{min})$$

$$R_L(\text{min}) = V_z\ R_s / [V_{in} - V_z]$$

Therefore, I_L (max) = V_o / R_L(min)

To determine the maximum value of R_L:

It is known when R_L is high the load current is low and so the diode current will be maximum.

Therefore, $I_s = I_z$ (max) + I_L(min)

I_L (min) = $I_s - I_z$ (max)

R_L (max) = V_o / I_L (min)

2.15.2 Series Voltage Regulator

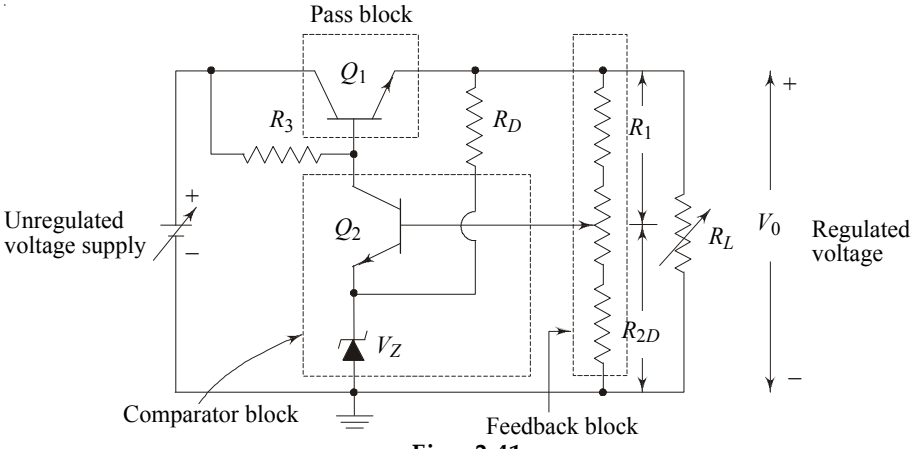


Fig. 2.41

Series voltage regulator consists of following main block (shown in figure);

1. Pass block
2. Comparator block
3. Feedback block

Pass Block It is generally designed with a power transistor capable of handling higher current for voltage regulation purpose.

Feedback Block It is generally a simple voltage divider network, consisting of two resistors and voltage is tapped at the center of these two. Since it is connected at the load side and is in parallel with the load resistance, it is capable of taking part of the output and feeding it to one of the input terminals of the comparator.

Comparator Block It is a simple comparator capable of comparing the feedback signal from the load with respect to the standard zener diode (reference voltage).

Experiment (Voltage Regulator)

Aim: ***Design and Construct a Shunt and Series Voltage Regulator and Find the Following Plots:***

1. Line regulation.
2. Load regulation.

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
Voltmeter	(0-10) V	1

Circuit Diagram:

Shunt Regulator:

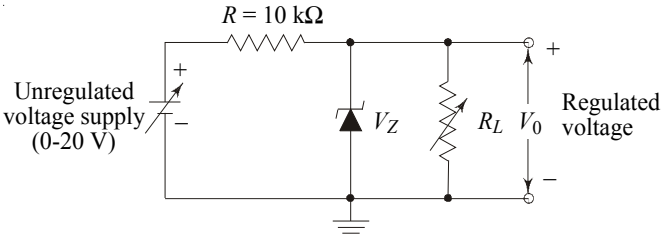


Fig. 2.42

Series Regulator:

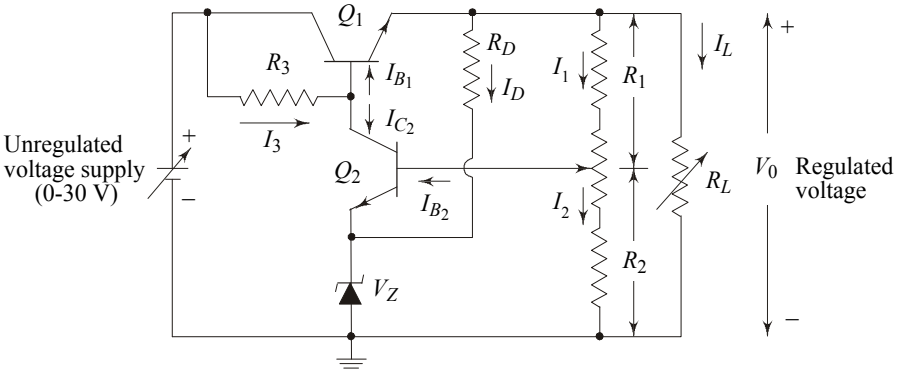


Fig. 2.43

Design:

Series Regulator:

Given: V_L = 10 V; I_L = 10 mA; V_z = 5.2 V;

β_1 (h_{fe_1}) of power transistor (pass element) = measure from multimeter.

$\beta_2(h_{fe_2})$ of comparator transistor = measure from multimeter.

Load resistor is given by,

$R_L = V_L / I_L$ = ? (Load should be more than this value)

Assume, current through diode, $I_D = I_L/10$

Current though feedback network, $I_1 = \dfrac{I_L}{10}$

Therefore, the value of R_{B2} is given by,

$$R_1 = \frac{V_L - (V_{BE2} + V_Z)}{I_1}$$

R_1 = ?

$$V_{BE2} + V_Z = \frac{V_L}{R_1 + R_2} \times R_2$$

Find, $R_2 = ?$

Zener diode resistance can be calculated by,

$$R_D = \frac{(V_L - V_Z)}{I_D}$$

Since, $I_{E1} = I_L + I_1 + I_D$

$I_{C1} \simeq I_{E1} = ?$

Therefore, $I_{B1} = I_{E1}/\beta_1$

To find the controlling resistance, $R_3 = \dfrac{\left[V_{in(MAX)} - (V_{BE1} + V_L)\right]}{I_3}$

where, $I_3 = I_{C2} + I_{B1}$

Procedure:

Line Regulation:

1. Connect the circuit as per the designed circuit diagram.
2. Connect the load resistance (any value above designed) of higher wattage (say 1 kΩ/ 1watt).
3. Vary the input DC supply in regular steps.
4. Note down the corresponding output voltage using a voltmeter.
5. Plot the graph: V_{in} vs V_0

Load Regulation:

1. For the same circuit shown, fix the input DC supply voltage (say, 12 V) more than the regulating value.
2. Replace the fixed resistance by a decade resistance box.
3. Vary the load in regular steps.
4. Note down the corresponding output voltage across the load using voltmeter.

Note: Above said procedure holds good for shunt regulator also. As far as the design is concerned, zener diode should be selected according to the required regulated output voltage.

Graph:

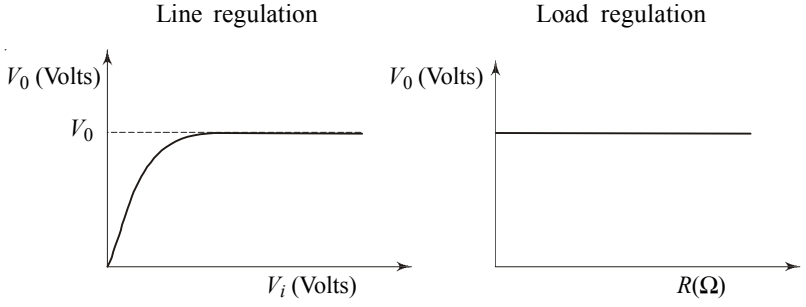


Fig. 2.44

Result:

Line Regulation: (R_L = constant)

Input Voltage (V)	Output Voltage (V)

Load Regulation: (V_{in} = constant)

Load constant (Ω)	Output Voltage (V)

Experiment (DIAC)

Aim: To study the characteristic of DIAC

Equipment required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
DC voltmeter	(0-30) V	1
DC ammeter	(0-10) mA	1

Circuit diagram

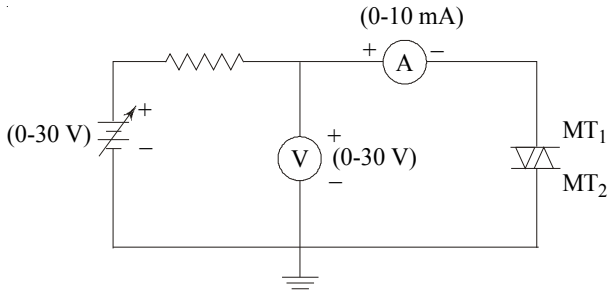


Fig. 2.45

Procedure:

1. Connections are made as per circuit diagram.
2. Vary the power supply in regular steps and note down the corresponding current and voltage of the DIAC.
3. Reverse the DIAC terminal.
4. Repeat the procedure 2.
5. Plot the graph: Voltage (V) V/S current (mA)

Tabular column

Forward biased		Reverse biased	
Voltage (Volts)	Current (mA)	Voltage (Volts)	Current (mA)

Model graph

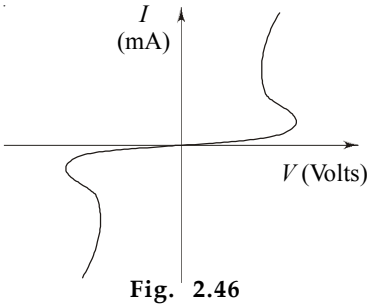


Fig. 2.46

DIAC

DIAC is a bidirectional switch, which has two terminals MT_1 and MT_2. Rising the applied voltage more than the break over voltage affects the conduction of DIAC. When the anode-2 is made more positive than anode-1, current start conducting from anode-2 to anode-1. The sudden rush of current results in the small voltage across the device. Hence immediately after the break over point, the voltage drops down. When the node-1 is made more positive than anode-2, the current start conducting from anode-1 to anode-2.

OBJECTIVE QUESTIONS

1. What is the difference between the drift and the diffusion?
2. Explain reverse saturation current.
3. What is meant by early effect?
4. Compare the electro-static deflection with magneto-static deflection system in CRO.
5. What is difference between static and dynamic resistance in case of diode?
6. What is necessary in having diode linear piece-wise characteristics?
7. How do you define barrier potential?
8. Is reverse saturation current independent of forward and reverse bias? Why?
9. State the main application of a zener diode.
10. What is difference between zener diode and conventional rectifying diode?
11. What is difference between diode and photo-diode?
12. Write the diode equation.
13. Why should the temperature be mentioned in degree kelvin?
14. What is the biasing condition for a transistor in active region?
15. What is the biasing condition for a transistor in cut-off region?
16. What is the biasing condition for a transistor in saturation region?
17. Why is a transistor so called ?
18. Explain the relative doping rate of transistor layers.
19. Explain the relative area of each transistor layers.
20. Give some examples for transistor operating in active region.
21. Give some examples for transistor operating in saturation and cut-off region.
22. What are dependent and independent variables in BJT model?
23. Explain base spreading resistance.
24. What is the difference between h_{FE} and h_{fe}?

25. Draw the ebers-moll model for a transistor and explain.
26. Define punch-through.
27. What is the basic working principle of a photo-transistor?
28. What is meant by bipolar junction transistor?
29. What are the main features of selecting *h*-parameters for BJT modeling?
30. Write some distinguished characteristics of a FET over BJT.
31. What are the advantages of a FET?
32. What are the disadvantages of a FET?
33. List out the family of FET.
34. Why is FET called so? Explain.
35. Explain pinched-off voltage.
36. Draw the low-frequency small signal FET model.
37. Draw the low-frequency small signal BJT model.
38. Distinguish between enhancement type FET and depletion type FET.
39. Give some examples of FET application.
40. Explain voltage-variable resistor in FET.
41. What is the main application of VVR in FET?
42. Why is *n*-channel superior to *p*-channel FET?
43. Mention two disadvantages of CMOS.
44. What is EMOSFET?
45. Why are MOSFETs not handled with the bare hand?
46. What is the main difference between diode rectification and silicon controlled rectification?
47. Mention few more applications of SCR.
48. Give some examples of UJT application.
49. Explain negative resistance region in UJT.
50. What are the applications of UJT?
51. Explain the two-transistor analogy of SCR.
52. n-channel MOSIETS are most preferred than p-channel, why?
53. What is the main advantage of CMOS technology?
54. Explain operation of DIAC.
55. What are the applications of DIAC.

3 AMPLIFIERS AND OSCILLATORS

3.1 THE BASIC AMPLIFIER

The common-emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification.

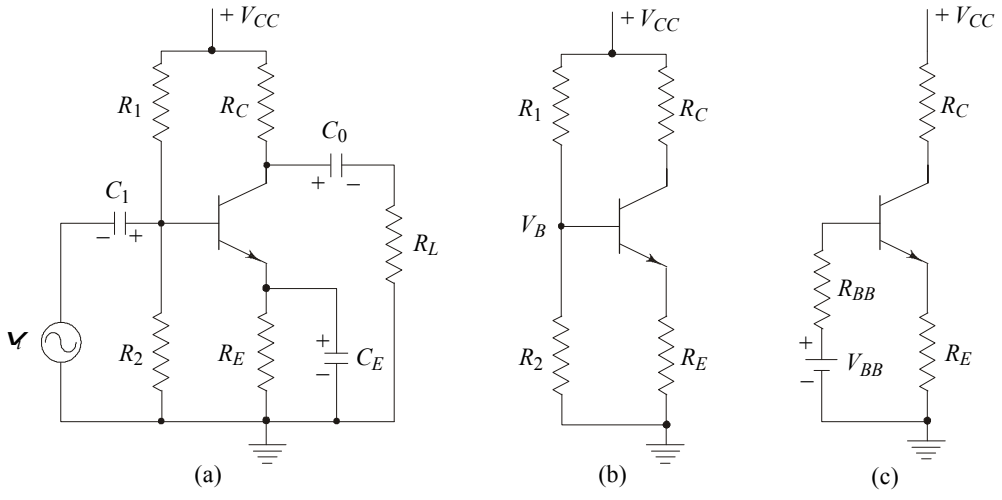


Fig. 3.1

Since a capacitor acts as an open circuit for DC, the above circuit is redrawn as where resistors R_1, R_2, R_C, R_E and V_{CC} are all affecting the biasing condition. It is so designed that the transistor operates linearly and a maximum peak-to-peak in the output is possible. Resistors R_1 and R_2 form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and, ensure that the emitter base junction is operating in the proper region.

In order to operate the transistor as an amplifier, the biasing is done in such a way that the operating point should be in the active region. As for using the transistor as a switch, the operating point should oscillate between, cut off region and saturation region.

On simplification Fig. (3.1b) reduces to Fig. 3.1(c), where

$$R_{BB} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{BB} = \frac{V_{CC} R_2}{R_1 + R_2}$$

3.1.1 Quiscent Operating Point Calculation

Applying KVL to output loop of Fig. 3.1(c), we get

$$V_{CC} = V_{CE} + I_C R_C + I_E R_E$$

Since $I_C \simeq I_E$ (as I_B is negligibly small),

$$V_{CC} = V_{CE} + (R_C + R_E)\, I_C \tag{1}$$

In order to find the DC load line. Set the following boundary conditions.

Boundary conditions 1: When $V_{CE} = 0$;

The equation (1) reduces to

$$I_C = \frac{V_{CC}}{R_C + R_E} \tag{2}$$

Boundary condition 2: When $I_C = 0$:

The equation (1) reduces to

$$V_{CE} = V_{CC} \tag{3}$$

The AC load line is the line joining two extreme boundary conditions in the output characteristic of common emitter configuration,

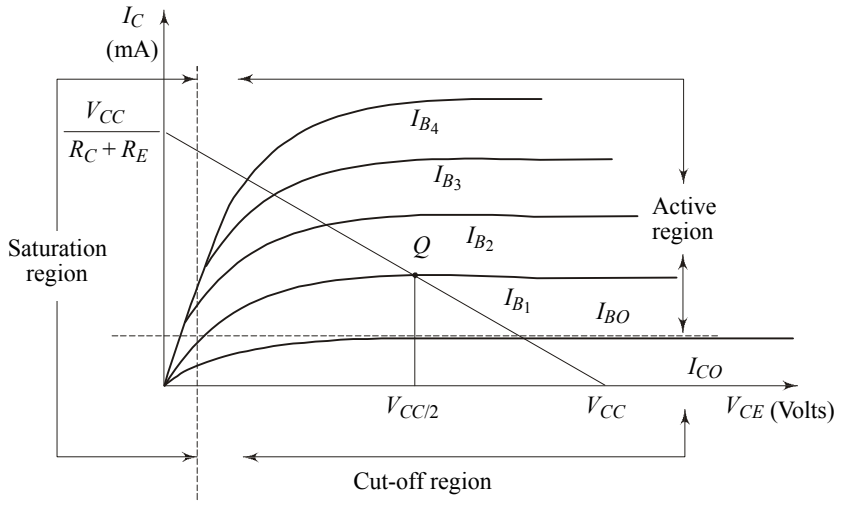


Fig. 3.2

The load line defines the operating point of the circuit. When the collector current becomes zero ($V_{CE} = V_{CC}$), the transistor is said to be 'cut-off'. When V_{CE} is less than 0.1 V to 0.2 V, the transistor is said to be at 'saturation'. During saturation, the current in the transistor is maximum. Thus when I_B increases, V_{CE} decreases and vice versa.

For an amplifier, the Q point is placed so that the load line is bisected (midway). Therefore, in practical design, the V_{CE} is always set to $V_{CC}/2$. This will confirm that the Q point always

swings within the active region. This limitation can be explained by *maximum handling capacity*. Output is produced without any clipping or distortion for the maximum input signal. If so, reduce the input signal magnitude.

The Bypass Capacitor The emitter resistor R_E is required to obtain the DC quiescent stability. However, the inclusion of R_E in the circuit causes a decrease in amplification at higher frequencies. In order to avoid such a condition, it is bypassed by a capacitor so that it acts as a short circuit for AC and contributes stability for DC quiescent condition. Hence, a capacitor is connected in parallel with emitter resistance.

$$X_{CE} << R_E$$

$$\frac{1}{2\pi f C_E} << R_E$$

$$C_E >> \frac{1}{2\pi f R_E}$$

The Coupling Capacitor An amplifier amplifies the given AC signal. In order to have noiseless transmission of signal (without DC), it is necessary to block DC, i.e., the direct current should not enter the amplifier or load. This is usually accomplished by inserting a coupling capacitor between any two stages.

$$X_{CC} << (R_i \parallel h_{ie})$$

$$\frac{1}{2\pi f C_C} << R_i \parallel h_{ie}$$

$$C_c >> \frac{1}{2\pi f (R_i \parallel h_{ie})}$$

Frequency Response Emitter bypass capacitors are used to short-circuit the emitter resistor and thus increase the gain at high frequency. These coupling and bypass capacitors cause the fall off in the low frequency response of the amplifier because their impedance becomes large at low frequencies. The stray capacitors are effectively open circuits.

In the mid frequency range, the large capacitors are effective short circuits and the stray capacitors are open circuits, so that no capacitance appears in the mid frequency range. Hence, the midband gain is maximum.

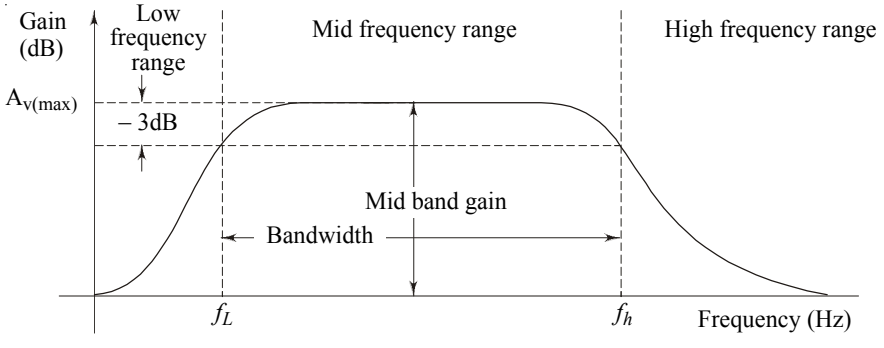


Fig 3.3 Frequency response of an amplifire

At the high frequencies, the bypass and coupling capacitors are replaced by short circuits and stray capacitors and the transistor determine the response.

In the usual application, midband frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain ($|A_m|$). These are shown as f_L and f_H, and are called as the 3dB frequencies or simply the lower and higher cut off frequencies respectively. The difference between higher cut-off frequency and lower cut-off frequency is referred to as bandwidth ($f_H - f_L$)

Test for Active Region

1. According to our design, $V_{CC} = I_C R_C + V_{CE} + I_E R_E$.
2. Since, $V_{CE} = V_{CC}/2$ (transistor active), after applying biasing voltage (V_{CC}), drop across collector to emitter should be half of biasing voltage.
3. If it is not satisfied, connect a potentiometer in series with R_{B2} whose value should be ± 1 kΩ with respect to R_{B2}.
4. Vary potentiometer such a way that drop across emitter and the collector of the transistor is half of the biasing voltage.
5. If any non-linearity occurs in the output waveform, a negative feedback is introduce in the circuit. This can be done by connecting a potentiometer in the emitter side whose value is above the designed value. *(Top terminal of the potentiometer should be connected to the emitter terminal of the transistor, center terminal should be connected to the positive terminal of the capacitor and the lower terminal should be connected to the ground of the circuit)*.
6. On the other hand, by reducing the amplifier gain, we can reduce the non-linearity in the output waveform. This can be done by replacing the fixed collector resistor (R_C) by a potentiometer of the same order and vary it in the opposite direction.

Calculation of Input Impedance and Output Impedance

To calculate input impedance

Connect a potentiometer in series with the signal generator as shown in the figure. Connect a ac voltmeter across the amplifier set the input signal of the specified magnitude (say 50 mV) at mid band frequency. Now vary the value of potentiometer such that the value of ac voltmeter (rms value) measures half the voltage of signal generator. Now measure the resistance value potentiometer which is equal to input impedance of the given amplifier circuit. During this process set the biasing voltage to zero.

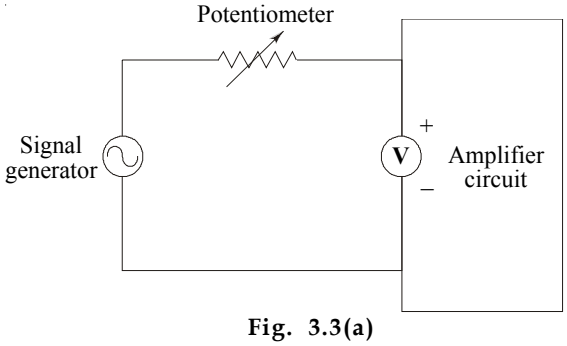


Fig. 3.3(a)

To Calculate output impedance

Set the biasing voltage to zero. Connect a ac ammeter (0-10 mA) in series with the signal generator connected as shown in

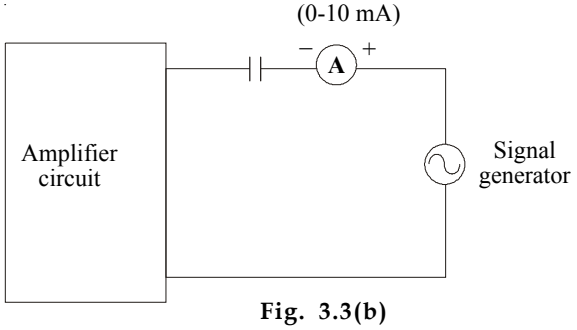


Fig. 3.3(b)

figure. Apply any finite value of voltage at mid frequency range. Measure the ammeter reading. The ratio of voltage applied to the current measured is the value of output impedance.

3.1.2 RC Coupled Amplifier

Experiment:

Aim: ***To Design and Impliment the RC Coupled Amplifier Circuit and to Find:***

1. Cut off frequencies
2. Band width
3. Mid band gain
4. Input/output impedance

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

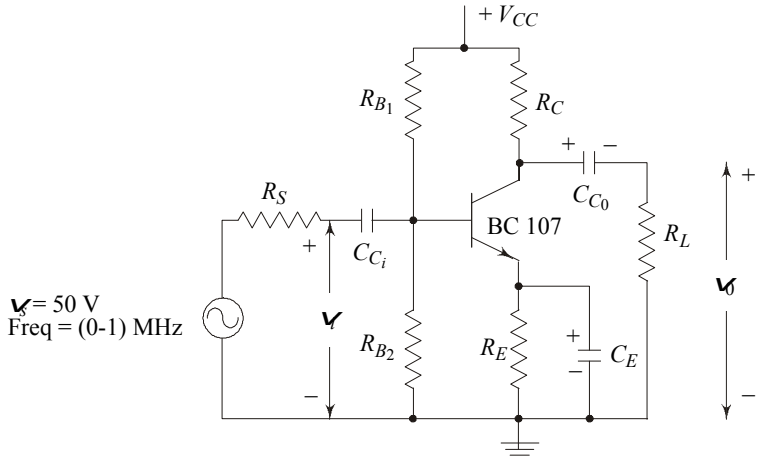


Fig. 3.4

Design:

Given data: V_{CC} = 15 V; I_C = 1 mA; f_L = 100 Hz; Stability factor = [10];
h_{fe} = from transistor manual; A_{vs} = 50 dB; I_E = 1.2 mA

Gain formula is given by,

$$A_V = \frac{-h_{fe}\ R_{Leff}}{Z_i} \tag{1}$$

Assuming, $V_{CE} = \frac{V_{cc}}{2}$ (transistor active)

Effective load resistance is given by, $R_{leff} = R_C \parallel R_L$

Emitter resistance is given by, $r_e = \dfrac{26 \text{ mV}}{I_E}$

$$h_{ie} = \beta r_e$$

where, r_e is internal resistance of the transistor.

$$h_{ie} = h_{fe}\, r_e$$

$$V_E = \frac{V_{CC}}{10}$$

On applying KVL to output loop, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

where, $V_E = I_E R_E$

Find $R_C = ?$

From equation (1), Find $R_L = ?$

Since I_B is very small when compared with I_C,

$$I_C \simeq I_E$$

$$R_E = \frac{V_E}{I_E}$$

$$V_B = V_{BE} + V_E$$

$$V_B = V_{CC}\, \frac{R_{B2}}{R_{B1} + R_{B2}}$$

stability factor, $S = 1 + \dfrac{R_B}{R_E}$

Find $R_B = ?$

$$R_B = R_{B1} \parallel R_{B2}$$

Find R_{B1} and R_{B2}

Input impedence, $Z_i = (R_B \parallel h_{ie})$

Output impedence, $Z_o = R_C \parallel R_L$

Input coupling capacitor is given by, $X_{Ci} = \dfrac{Z_i}{10}$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

Output coupling capacitor is given by, $X_{C0} = \dfrac{R_c \,||\, R_L}{10}$

$$X_{C0} = \frac{1}{2\pi f C_0}$$

Find $C_0 = ?$

By-pass capacitor is given by, $X_{CE} = \dfrac{R_E}{10}$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set V_s = 50 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedance (given in page 137)
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.

Tabular Column:

v_s = 50 mV

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log(v_0/v_s)

Model Graph: (Frequency Response)

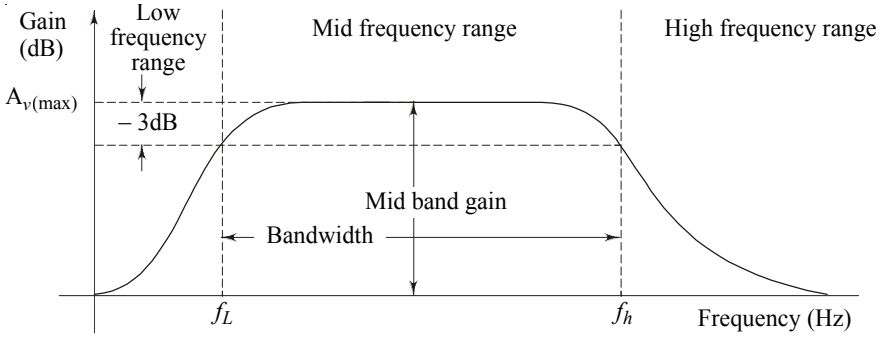


Fig. 3.5

Result:

	Theoretical	Practical
Input impedance	$Z_i = R_{BB} \parallel h_{ie}$	
Output impedance	$Z_0 = R_C \parallel R_L$	
Gain(Midband)		
Band width		

3.1.3 Two Stage RC–Coupled Amplifier

Experiment:

Aim: ***To Design and Test a two Stage RC Coupled Amplifier Circuit and to Find:***

1. Band width
2. Mid band gain
3. Input /output impedance

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20) MHz	1
Function generator	(0-1)MHz	1

Circuit Diagram:

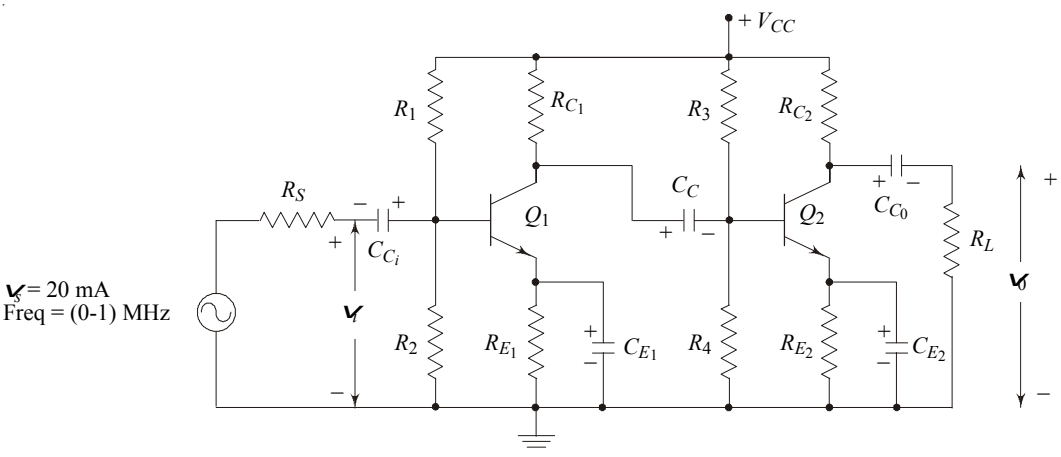


Fig. 3.6

Design:

Given data: $A_{V_2} = 10$ dB; $A_{V_1} = 20$ dB; $f_L = 100$Hz; $S = [10]$

$I_{E_1} = 3$ mA; $I_{E_2} = 1$ mA

h_{fe1} and h_{fe2} from transistor data manual

$$A_{V_2} = \frac{-h_{fe_2} R_{Leff}}{Z_{i_2}}$$

$R_{leff} = R_{C_2} \parallel R_L$

$h_{fe_2} = 200$ (from multimeter)

$r_{e_2} = 26 \times 10^{-3} / I_{E_2} = 26$

$h_{ie_2} = h_{fe_2} \times r_{e_2} = 200 \times 26 = 5.2$ kΩ

From dc bias analysis, on applying KVL to the output loop, we get

$$V_{CC} = I_{C2}R_{C_2} + V_{CE_2} + V_{E_2}$$

$$V_{CE_2} = V_{CC}/2;\ V_{E2} = V_{CC}/10;\ I_{C_2} = 1\times10^{-3}\text{A}$$

$$R_{C_2} = ?$$

Since I_B is very small when compare with I_C

$$I_{C_2} \simeq I_{E_2}$$

Find, $R_L \parallel R_{C_2}$

Since, R_{C_2} is known, calculate R_L.

$$V_{E_2} = I_{E_2}R_{E_2}$$

Calculate $R_{E_2} = ?$

$$S = 1 + \frac{R_{B_2}}{R_{E_2}}$$

Find $R_{B_2} = ?$

$$R_{B_2} = R_3 \parallel R_4$$

$$V_{B_2} = V_{CC}\frac{R_4}{R_3 + R_4}$$

$$V_{B_2} = V_{BE_2} + V_{E_2}$$

Find $R_3 = ?$

Therefore, find R_4

$$Z_{i_2} = h_{ie_2} \parallel R_{B_2}$$

Find, $Z_{i_2} = ?$

$$R_{Leff_1} = Z_{i_2} \parallel R_{C_1}$$

Find R_{Leff1} from the gain formula given above

$$A_{V_1} = \frac{-h_{fe_1}R_{Leff_1}}{Z_{i_1}}$$

Find $R_{C_1} = ?$

On applying KVL to the first stage, we get

$$V_{CC} = I_{C_1}R_{C_1} + V_{CE_1} + V_{E_1};\ V_{CE_1} = \frac{V_{CC}}{2}$$

Find $R_{E_1} = ?$

$$S = 1 + \frac{R_{B_1}}{R_{E_1}}$$

Find $R_{B_1} = ?$

$$R_{B_1} = R_1 \parallel R_2$$

$$V_{B_1} = V_{CC} \frac{R_2}{R_1 + R_2}$$

$$V_{B_1} = V_{BE_2} + V_{E_2}$$

Find $R_1 = ?$

Therefore, find R_2

Output impedence, $Z_{o_2} = R_{C_2} \parallel R_L$

$$Z_{i_1} = h_{ie_1} \parallel R_{B_1}$$

Total gain including source resistance is given by,

$$A_{VT} = A_{V_1} \times A_{V_2} \text{ [In dB, } A_V = A_{V_1} + A_{V_2}$$

$$X_{Ci} = \frac{Z_i}{10}$$

$$X_{ci} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

$$X_{co} = (R_C \parallel R_L)/10$$

$$X_{co} = \frac{1}{2\pi f C_0}$$

Find $C_o = ?$

$$X_{CE} = R_E/10$$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set v_s = 20 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency
5. Find the input and output impedance:

   Input impedance,

$$Z_i = \frac{v_i R_S}{v_S + v_i}$$

Output impedance,

$$Z_0 = \frac{\left(V_{\text{load}} - V_{\text{no load}}\right)}{V_{\text{no load}}} \times R_L$$

6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output.

Tabular Column:

v_s = 20 mV

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log(v_0/v_s)

Model Graph: (Frequency Response)

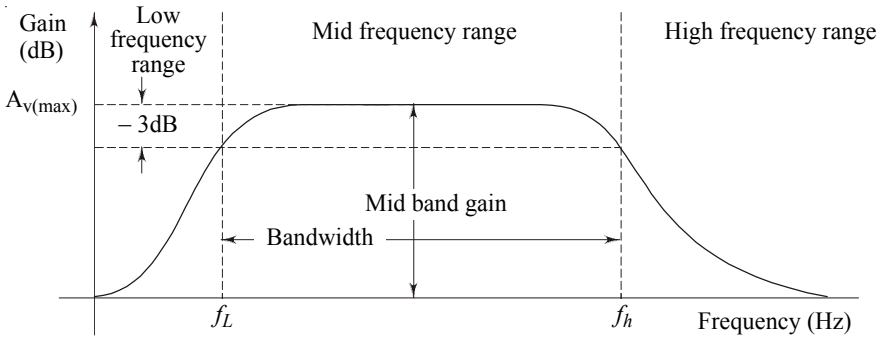


Fig. 3.7

Result:

	Theoretical	Practical
Input impedance	$Z_i = R_{BB_1} \parallel h_{ie_1}$	
Output impedance	$Z_0 = R_{C_2} \parallel R_{L_2}$	
Gai n(Mid band)		
Band width		

3.1.4 Emitter Follower (Common Collector Amplifier)

Experiment:

Aim: ***Design and Test a Common Collector Current Amplifier and Find the Following Parameters:***

1. Current gain
2. Voltage gain

3. Bandwidth
4. Input and output impedance

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

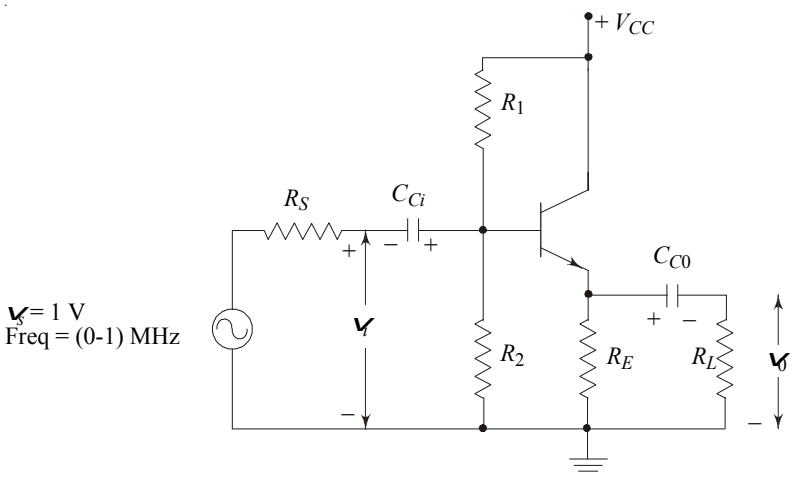


Fig. 3.8

Design:

Given data: V_{CC} = 12 V; f_L = 100 Hz; I_E = 1 mA; S = [1-10]; R_L = 4.7KΩ; $\beta = h_{fe}$

$h_{ie} = \beta r_e$; A_V = 30 dB

where, r_e is internal resistance of the transistor.

$$r_e = \frac{26 \text{ mV}}{I_E}$$

$$h_{ie} = h_{fe}\, r_e$$

$$A_V \leq 1 = \frac{R_E}{R_E + Z_b}$$

$$A_I = h_{fe}\, \frac{R_E}{R_E + Z_b}$$

where $Z_b = \beta r_e + (1 + \beta)\, R_E$

From DC bias analysis, on applying KVL to the output loop, we get

$$V_{CC} = V_{CE} + V_E;\ V_{CE} = V_{CC}/2$$

$$R_{Eeff} = ?$$

$$V_E = I_E \, R_{Eeff}$$

$$R_{Eeff} = R_E \parallel R_L$$

Find R_E (R_L is given)

$$S = 1 + \frac{R_B}{R_E}$$

Find $R_B = ?$

$$R_B = R_1 \parallel R_2$$

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2} = \frac{V_{CC} \, R_B}{R_1}$$

$$V_B = V_{BE} + V_E$$

Find $R_1 = ?$

Therefore, find $R_2 = ?$

$$Z_i = h_{ie} + (1 + h_{fe}) \, R_E$$

Find, $Z_i = ?$

$$Z_{ieff} = Z_i \parallel R_{BB}$$

$$R_0 = R_e \parallel \left(\frac{R_s \parallel R_s + h_{ie}}{h_{fe}} \right)$$

Find $Z_0 = ?$

$$X_{Ci} = \frac{Zi_{eff}}{10}$$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

$$X_{CE} = R_E/10$$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set v_s = 1 V (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.

4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output.

Tabular Column:

v_s = 1V

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log(v_0/v_s)

Model Graph: (Frequency Response)

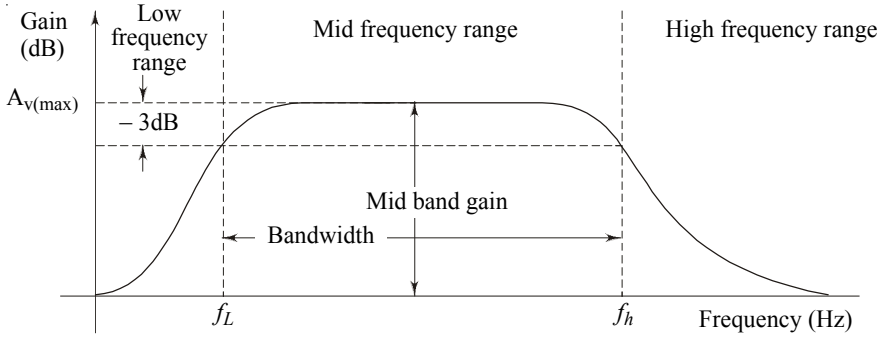


Fig. 3.9

Result:

	Theoretical	Practical
Input impedance	$Z_{ieff} = Z_i \parallel R_{BB}$	
Output impedance	$Z_{0eff} = R_E \parallel r_e \parallel R_L$	
Gain (Midband)		
Band width		

3.1.5 Darlington Pair (Common Collector Amplifier)

Experiment:

Aim: ***Design and Test a Darlington Current Amplifier and Find the Following Parameters:***

1. Current gain
2. Voltage gain
3. Bandwidth
4. Input and output impedance

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30)V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

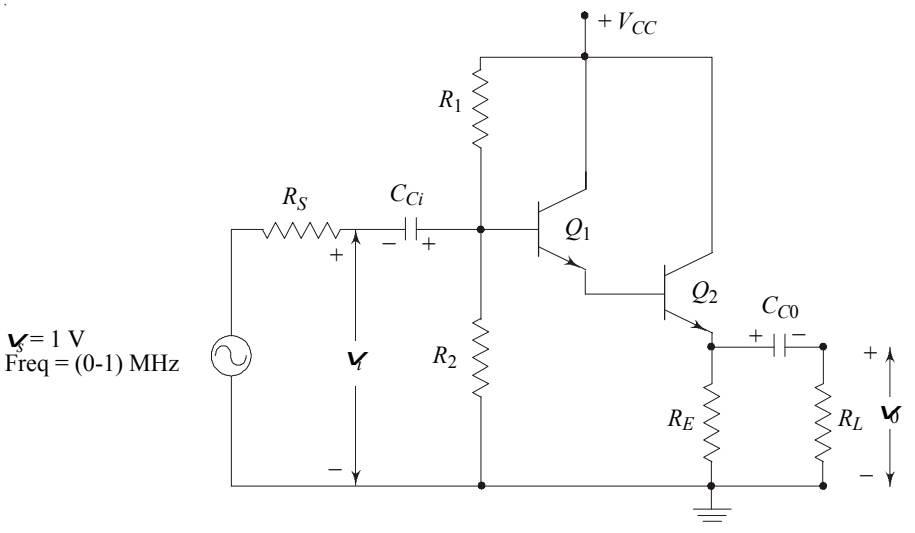


Fig. 3.10

Design:

Given data: $V_{CC} = 12$ V; $f_L = 50$ Hz; $I_E = 1$ mA; $S = [1 = 10]$; $R_L = 4.7$ KΩ

$$A_V \leq 1,\ A_I = A_{I_1} \times A_{I_2}$$

Since $h_{fe_1} = h_{fe_1};\ A_I = (h_{fe})^2$

From DC bias analysis, on applying KVL to the output loop, we get

$$V_{CC} = V_{CE} + V_E;\ V_{CE} = V_{CC}/2$$

$$R_{Eeff} = ?$$

$$V_E = I_E\, R_{Eeff}$$

$$R_{Eeff} = R_E \parallel R_L$$

Find R_E (R_L is given)

$$S = 1 + \frac{R_B}{R_E}$$

Find $R_B = ?$

$$R_B = R_1 \parallel R_2$$

$$V_B = V_{CC}\,\frac{R_2}{R_1 + R_2} = \frac{V_{CC}\ R_B}{R_1}$$

$$V_B = V_{BE} + V_E$$

Find $R_1 = ?$

Therefore, find $R_2 = ?$

$$Z_{i_1} = 2h_{ie} + (1 + h_{fe_1})R_E$$

Find, $Z_{i_1} = ?$

$$Z_{ieff} = Z_{i_1} \parallel R_{BB}$$

$$Z_0 = R_E \parallel \left[\frac{(R_s \parallel R_B) + 2h_{ie}}{h_{fe}^2}\right]$$

Find $Z_0 = ?$

$$X_{Ci} = \frac{Z_{ioff}}{10}$$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

$$X_{CE} = R_E/10$$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set v_s = 1 V (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output.

Tabular Column:

v_s = 1 V

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Model Graph: (Frequency Response)

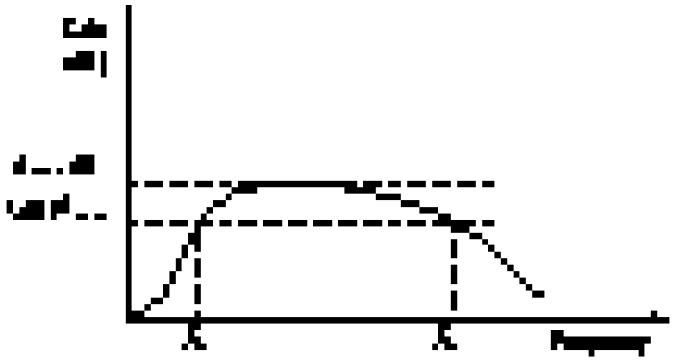


Fig. 3.11

Result:

	Theoretical	Practical
Input impedance		
Output impedance		
Gain (Mid band)		
Band width		

3.1.6 Cascode Amplifier

Experiment:

Aim: ***Design and Test the Cascode Emplifier for the Given Specification and Find the Following Parameters:***

1. Mid band gain.
2. Input and output impedance.

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

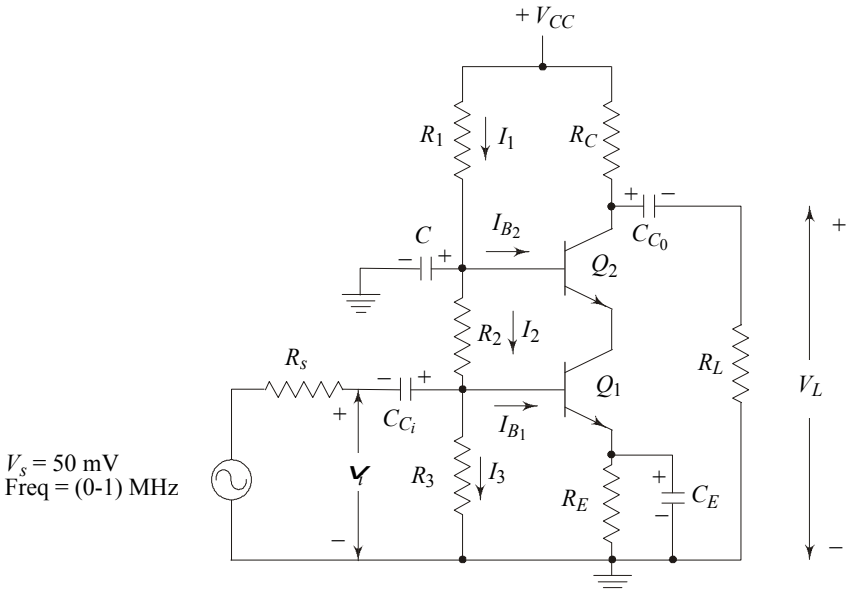


Fig 3.12

Design:

Given data: V_{CC} = 15V; $I_{E_1} = I_{E_2}$ = 1 mA; A_{V_T} = 100; f_L = 1 kHz; R_L = 4.7 KΩ; $\beta_1 = \beta_2$ = 100; Stability factor = [2-10]

$$R_s = 600\ \Omega$$

Assume, $V_{CE_1} = V_{CE_2} = V_{CC}/3$ (transistor active)

Effective load resistance is given by, $R_{Leff} = R_C \parallel R_L$

Emitter resistance is given by, $r_{e_1} = 26\ \text{mV}/I_{E_1}$

$$h_{ie_1} = \beta_1\ r_{e_1}$$

Since $\beta_1 = \beta_2$; $I_{E_1} = I_{E_2}$;

$$r_{e_1} = r_{e_2}$$

Gain is given by $A_{V_1} = V_{0_1}/V_i \approx -\ R_L\ /\ r_{e_1}$

With $R_L = r_{e_2} = h_{ib_2}$ of transistor–2 and $A_{V_1} = -\ r_{e_2}\ /\ r_{e_1} = -\ 1$

$$A_{V_2} = R_{Leff}\ /r_{e_2} = ?$$

Total gain is given by,

$$A_{V_T} = A_{V_1}\ A_{V_2} = 100 \text{ (given)}$$

Since A_{V_1} is calculated, calculate A_{V_2} from the above formula.

Calculate R_C from $R_{Leff} = R_C \parallel R_L$.

On applying KVL to output loop, we get

$$V_{CC} = I_C R_C + V_{CE_2} + V_{CE_1} + I_E R_E$$

where, $V_E = I_E R_E$

Find $R_E = ?$

Since $\beta_1 = \beta_2 = 100$

$$I_{B_1} = I_{C_1}/\beta_1 = I_{B_2}$$

Assume $R_3 = 4.7\ \text{K}\Omega$; $I_3 = V_{B_1}/R_3$

Find $I_3 = ?$

$$I_2 = I_3 + I_{B_1}$$

Find $I_2 = ?$

$$R_2 = [V_{B_2} - V_{B_1}]/I_2 = ?$$

$$I_1 = I_2 + I_{B_2}$$

Find $I_1 = ?$

$$R_1 = [V_{CC} - V_{B_2}]/I_1$$

Find $R_1 = ?$

Coupling and by-pass capacitors can be thus found out by,
Input coupling capacitor is given by, $X_{C_2} = (h_{ie_2} \parallel R_2 \parallel R_3)/10$

$$X_{C_2} = \frac{1}{2\pi f C_2}$$

Find $C_2 = ?$

Input coupling capacitor is given by, $X_{C_1} \simeq (h_{ie_1} \parallel R_1 \parallel R_2)/10$

$$X_{C1} = \frac{1}{2\pi f C_1}$$

Find $C_1 = ?$

Output coupling capacitor is given by, $X_{C_0} = (R_C \parallel R_L)/10$

$$X_{C_0} = \frac{1}{2\pi f C_0}$$

Find $C_0 = ?$

By-pass capacitor is given by, $X_{CE} = R_E/10$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set e_s = 50 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.

Tabular Column:

e_s = 50 mV

Frequency	e_0 (volts)	Gain = e_0/e_s	Gain (dB) = 20 log (e_0/e_s)

Model Graph: (Frequency Response)

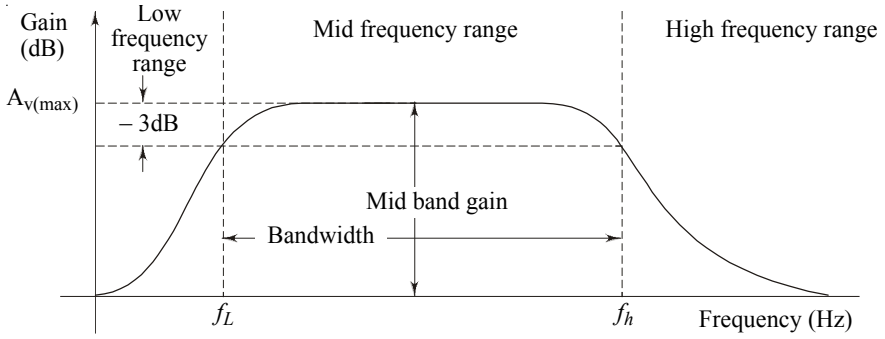


Fig. 3.13

Result:

	Theoretical	Practical
Input impedance		
Output impedance		
Gain (Midband)		
Band width		

3.1.7 Field Effect Transistor

Experiment:

Aim: ***To Determine the Parameters of the Single-Stage JFET Amplifier (Common-Drain Amplifier)***

1. Band width.
2. Mid band gain.
3. Input and output impedance.

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

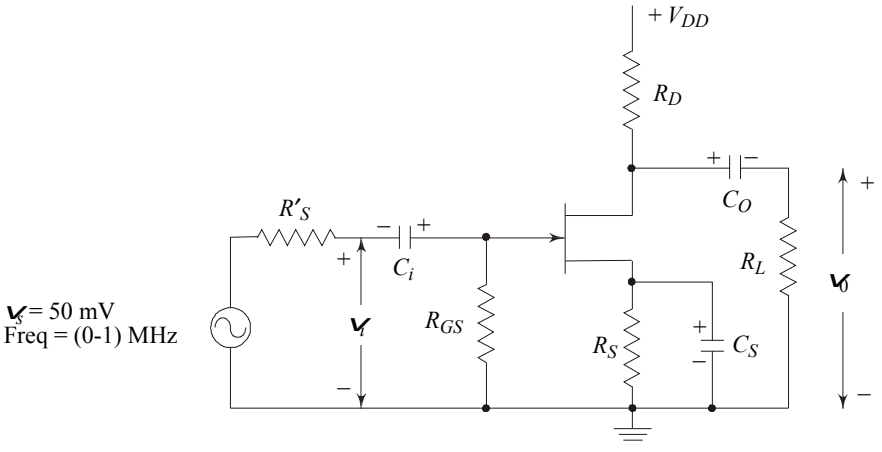


Fig. 3.14

Design:

Given data: $I_{DSS} = 10$ mA; $V_P = -4$ V; $f_L = 50$ Hz; $V_{DD} = 12$ V; $R_S' = 680\ \Omega$

From the DC bias condition,

$$I_D = I_{DSS}/2 = ?$$

For which $$I_D = I_{DSS}\ [1-(V_{GS}/V_P)]^2$$

Find $$V_{GS} = ?$$

$$V_{DS} = \frac{V_{DD}}{2}$$

$$V_{DD} = I_D R_D + V_{DS} + V_S$$

Since $$I_D = I_S\ (I_G = 0)$$

$$\therefore \quad V_{DD} = I_D\ (R_D + R_S) + \frac{V_{DD}}{2}$$

$$\therefore \quad (R_D + R_S) = \frac{V_{DD} - V_{DD/2}}{I_D}$$

Assume $$R_S = 500\ \Omega$$

Find R_D = ?

Find, $g_{m0} = 2I_{DSS} / |V_P|$ = ?

The value of g_m at the bias voltage is given by,

$$g_m = g_{m0}[1 - (V_{GS}/V_P)]$$

Find g_m = ?

$$r_m = 1/g_m$$

Find r_m = ?

With R_S completely by-passed, the largest amplifier gain is given by,

$$A_V = - R_D/r_m$$

Find A_V = ?

For which R_{G_1} = open and R_{GS} = 100 MΩ

Coupling and by-pass capacitors can be thus found out

Input coupling capacitor is given by, $X_{Ci} = R_{GS}$ /10

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find C_i = ?

Output coupling capacitor is given by, $X_{C0} = (R_D \parallel R_L)/10$

$$X_{C0} = \frac{1}{2\pi f C_0}$$

Find C_0 = ?

By-pass capacitor is given by, $X_{CS} = R_S/10$

$$X_{CS} = \frac{1}{2\pi f C_S}$$

Find C_S = ?

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set V_s = 50 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances.

6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.

Tabular Column:

v_s = 50 mV

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Graph: (Frequency Response)

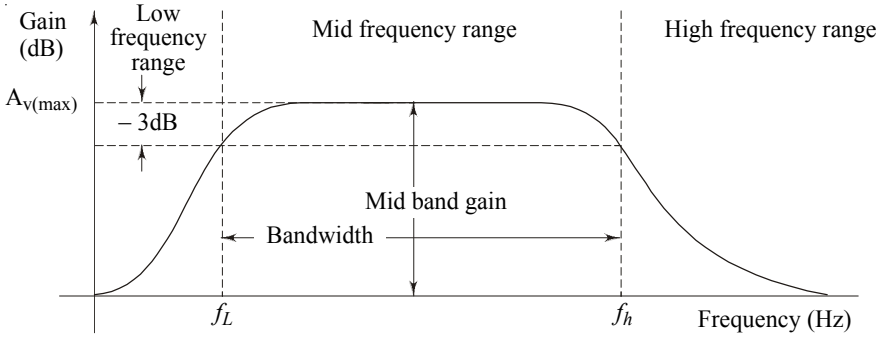


Fig. 3.15

Result:

	Theoretical	Practical
Input impedance	$Z_I = R_G$	
Output impedance	$Z_0 = R_S \parallel r_m$	
Gain (Midband)	$(R_S \parallel R_L)/r_m + (R_S \parallel R_L)$	
Band width	∞	

3.1.8 Differential Amplifier

Experiment:

Aim: ***To Construct the Differential Amplifier for Dual Input Balanced Output and Unbalanced Output in the Common Mode and Differential Mode Configuration and Study the Output Waveform and to Find Common-Mode Rejection Ratio (CMRR)***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30)V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

Single Input Unbalanced Output

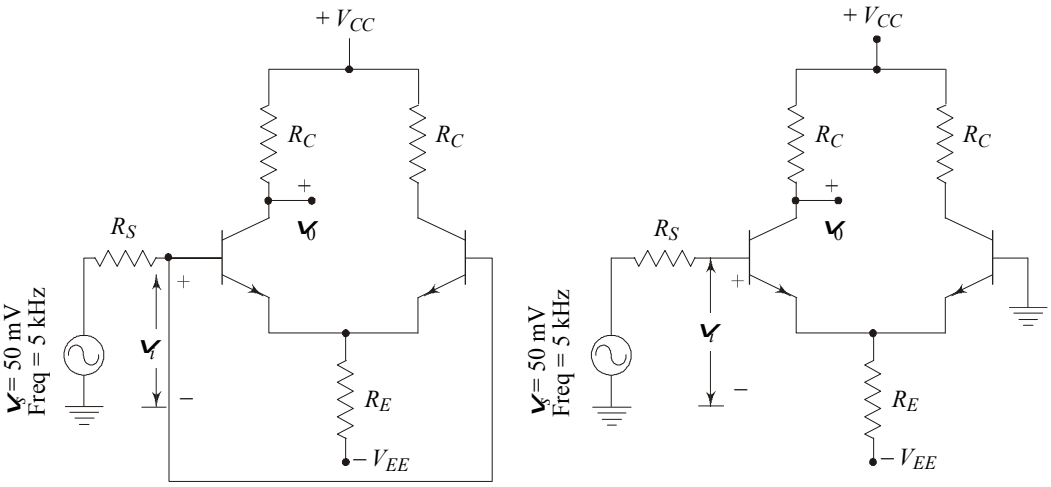


Fig. 3.16

Single Input Balanced Output

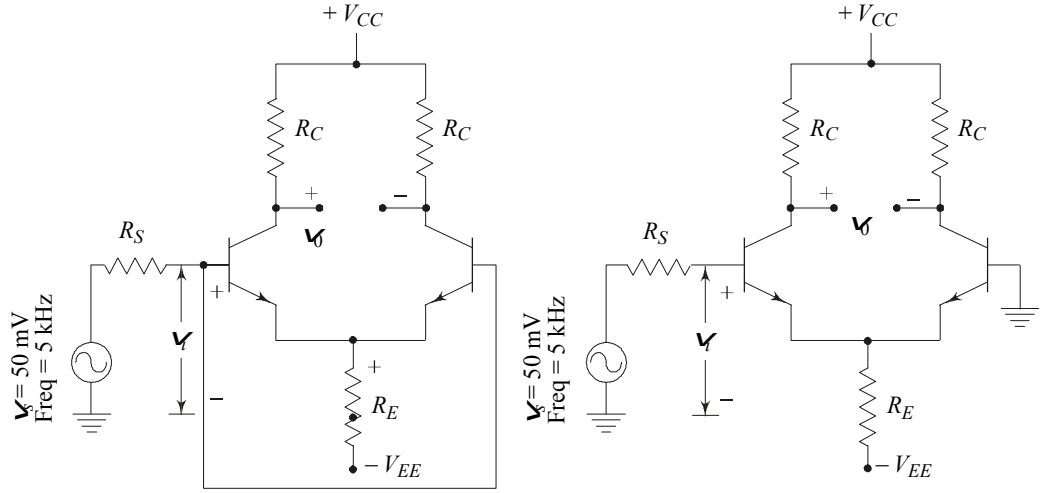


Fig. 3.17

Design for Dual input imbalanced output

Given: A_c = 0.1, A_d = 100; I_E = 1 mA

Differential gain is given by, $A_d = \frac{R_c}{2r_e}$

But $$r_e = \frac{26 \times 10^{-3}}{I_E}$$

Therefore, $$R_C = r_e A_d$$

$$CMRR = \frac{A_d}{A_C}$$

Emitter resistance can be calculated as,

$$R_E = \frac{R_C - A_C r_e}{2 A_C}$$

Design for Dual input balanced output

Differential gain is given by, $A_d = \frac{R_C}{2r_e}$

$$r_e = \frac{26 \times 10^{-3}}{I_E}$$

$$R_C = r_e A_d$$

$$CMRR = \frac{A_d}{A_C}$$

Emitter resistance can be calculated as,

$$R_E = \frac{2R_C - A_C r_e}{2 A_C}$$

Procedure:

1. Connect the circuit as per the circuit diagram (common-mode configuration).
2. Set v_s = 50 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
8. Differential gain must be calculated only at mid gain bandwidth.

Tabular Column:

v_s = 50 mV

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Model Graph: (Frequency Response)

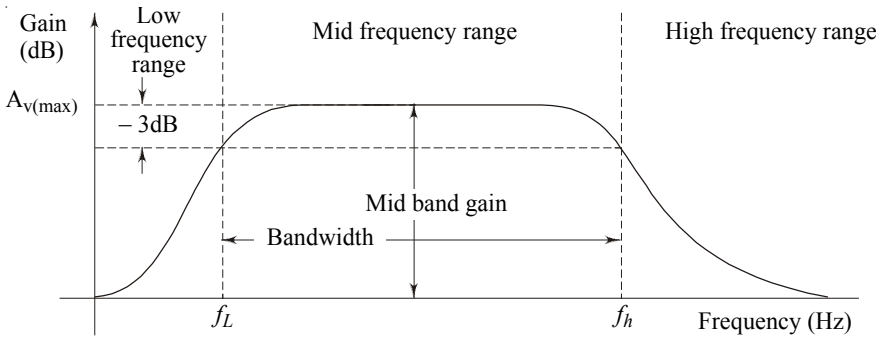


Fig. 3.18

Result:

	Theoretical	Practical
Input impedance		
Output impedance		
Gain(Mid band)		
Band width		

3.2 POWER AMPLIFIER

The amplifiers have either a transistor or tube as an active device. The devices are biased in such a way that they operate in the active region to provide amplification.

Depending on the choice of the operating point, the amplifier can be classified as *Class A, Class B, Class AB, Class C,* etc.,

Choice of *Q*-point is done by considering the transfer characteristic of the device which relates the input and output.

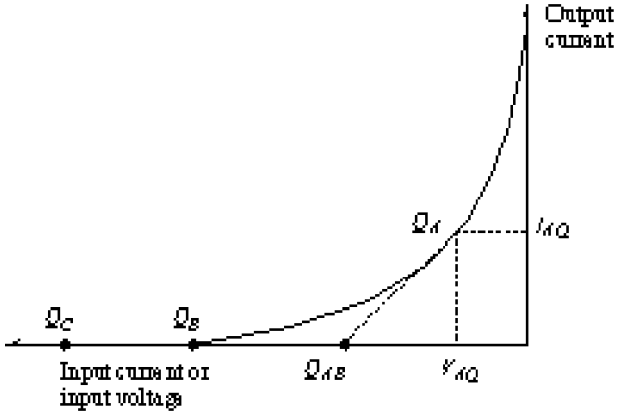


Fig. 3.19

If the *Q*-point is chosen in the linear region of the characteristic, the current and voltage vary linearly around their quiescent values.

At point Q_A, there exists a current in the circuit until V_{AQ} reduces to a very small value. Thus an amplifier in which the current does not become zero for any part of the cycle and which has a linear operation is known as a *class-A amplifier*.

At point Q_B, the output current reduces to zero, which indicates that the transistor is at cut-off. Hence for the positive swing of the input, the transistor is turned ON, and it results in an output current. During the negative half-cycle, the reverse bias is increase and thereby the device does not conduct. Thus only for one-half cycle the current flows while during the next half-cycle, the device is at cut-off. Amplifier operated with a *Q*-point at cut-off is known as a *class-B amplifier*.

In *class C amplifier* operation, the device is biased much to the left of V_{BQ}. In this case, there is no quiescent current. Even during the positive half-cycle, the output current flows only when the input signals exceeds V_{BQ} and therefore it flows for a period less than half a cycle.

Thus only in class A operation, the input is reproduced as such and there is a distortion produced only if the transfer characteristic is not linear in the range of the input signal. In case of class B and class C amplifier, the output is distorted as it conducts for half a cycle.

In class B and class C operation, current flows for half or less than half a cycle, the average power dissipation is low, and hence the efficiency is increased.

Generally, in case of small-signal amplifier, the magnitude of signal voltage and current are relatively small, the power handling capacity and power efficiency are low. On the other hand, large or power amplifier, primarily provide sufficient power to an output load to drive any power devices, typically a few watts to tens of watts. The main features of a power amplifier are the circuits, power efficiency, power handling capacity and impedance matching with respect to other devices.

Types:

Power amplifiers are divided into many types depending on their conduction time over a cycle. They are:

1. Class-A power amplifier.
2. Class-B power amplifier.
3. Class-AB power amplifier.
4. Class-C power amplifier.
5. Class-D power amplifier.
6. Class-S power amplifier.

3.2.1 Class-A Power Amplifier

The output signal varies for a full (360°) cycle of the input. In this case, the *Q*-point is biased almost at the half of the DC load line. A class-A amplifier, with DC bias at one half of the supply voltage, uses a good amount of power to maintain bias, even with no signal applied. This results in very poor efficiency. When very little AC power is delivered to the load a large amount of power is dissipated in the collector resistance (R_C). This results in a maximum efficiency of only 25%. By replacing the collector resistance (R_C) by a large inductor (also called a choke), the maximum efficiency can be increased to 50%.

DC Analysis To find the *Q*-point, apply KVL to the collector circuit, then

$$V_{CC} = V_{CE} + i_C R_E \tag{1}$$

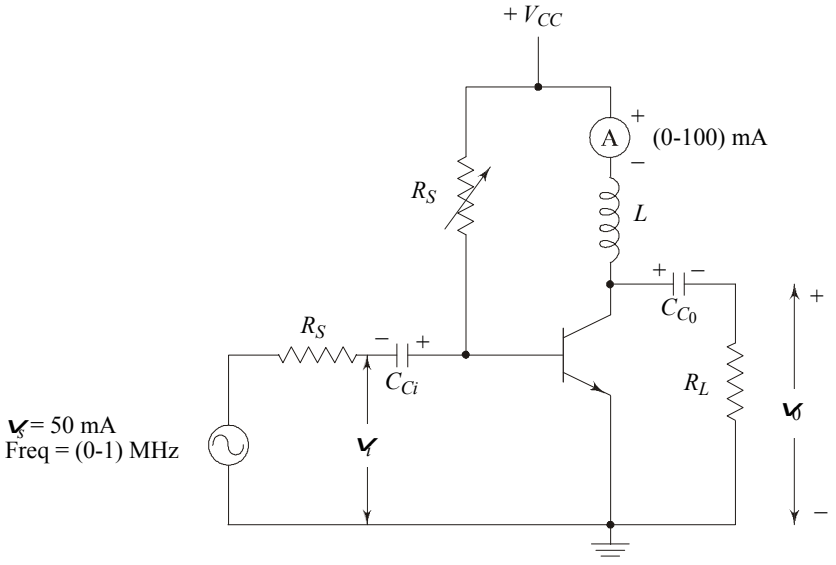


Fig. 3.20

(Emitter resistance should be kept as small as possible in order to minimize bias stability power loss)

The inductor acts as a short-circuit element for DC. Let us consider only AC voltage drop, this yields the AC load line equation,

$$v_{ce} = -i_C R_E = I_L R_L \tag{2}$$

$$i_C - I_{CQ} = -1/R_L\ [v_{ce} - V_{CEQ}] \tag{3}$$

Therefore, at maximum symmetrical swing, we get

$$i_{C\max} = 2I_{CQ} \text{ when } v_{ce} = 0\text{V}$$

Then, $$I_{CQ} = V_{CEQ}/R_L \tag{4}$$

Substituting (4) in (1) at the Q-point gives

$$I_{CQ} = V_{CC}/[R_L + R_E]$$

Since $$R_E << R_L$$

$$I_{CQ} = V_{CC}/R_L$$

Supply power, $$P_{ac} = I_{CQ}\ V_{CC} \simeq V_{CC}^2/R_L$$

This is constant and independent of signal current as long as the distortion is neglected.

Power transferred to load,

$$P_L = I_{CQ}^2\ R_L/2 = V_{CC}^2/2R_L$$

Collector dissipation,

$$P_C = P_{CC} - P_L$$

Thus, the maximum power dissipated in the collector occurs when the maximum power is dissipated by the load;

$$P_{C\max} = V_{CC}^2/2R_L$$

The maximum power dissipated by the collector when no signal is present,

$$P_{C\max} = V_{CC}^2/R_L = V_{CEQ}\, I_{CQ}$$

Efficiency Efficiency of operation of the inductor-coupled amplifier for a sinusoidal signal is,

$$\eta = P_L / P_{CC} = 50\%$$

Figure of Merit A figure of merit for a power amplifier is the ratio of maximum collector dissipation to maximum power dissipated in the load,

$$\eta = P_{L\max} / P_{C\max} = 2$$

Experiment (Class-A Power Amplifier)

Aim: ***To Design and Construct a Class-A Power Amplifier and to Determine its Efficiency***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30)V	1
CRO	(0-20)MHz	1
Function generator	(0-1)MHz	1

Circuit Diagram:

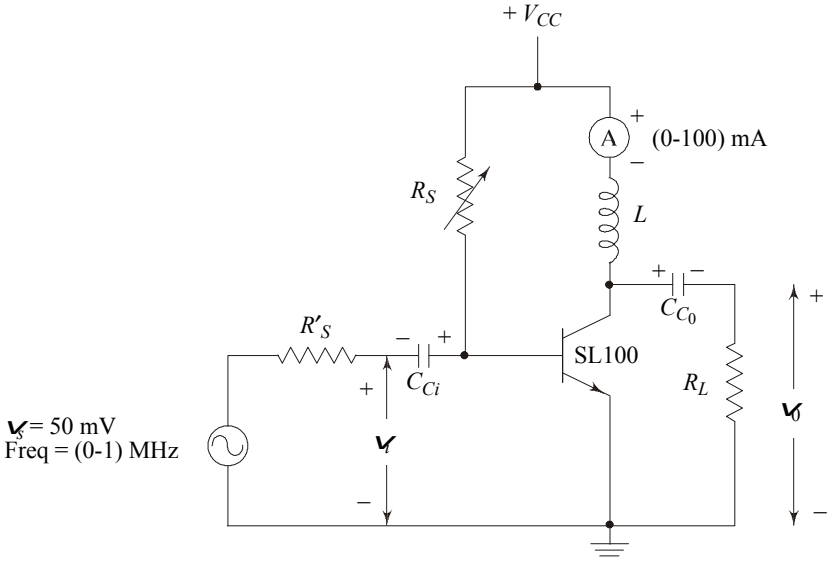


Fig. 3.21

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set v_s = 50 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency
5. Find the input and output impedances.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
8. Calculate the efficiency, $\eta = P_0/P_{in}$

Tabular Column:

v_s = 50 mV

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)	η

Model Graph: (Frequency Response)

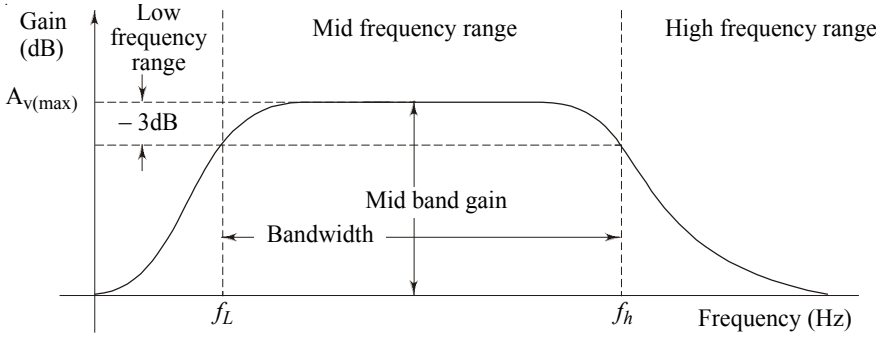


Fig. 3.22

Result:

	Theoretical	Practical
Gain (Midband)		
Band width		

3.2.2 Class-B Power Amplifier

Class-B operation is provided when the DC bias of the transistor is just off. This is essentially no bias and the transistor conducts for only one-half of the signal cycle. In order to obtain output signal for the full cycle of the signal, two transistors should be connected such a way that each transistor conducts on opposite half-cycle. Since one part of the circuit pushes the signal high during one-half cycle and the other part pulls the signal low, such a circuit is referred to as a '**push-pull**' circuit.

Block Diagram

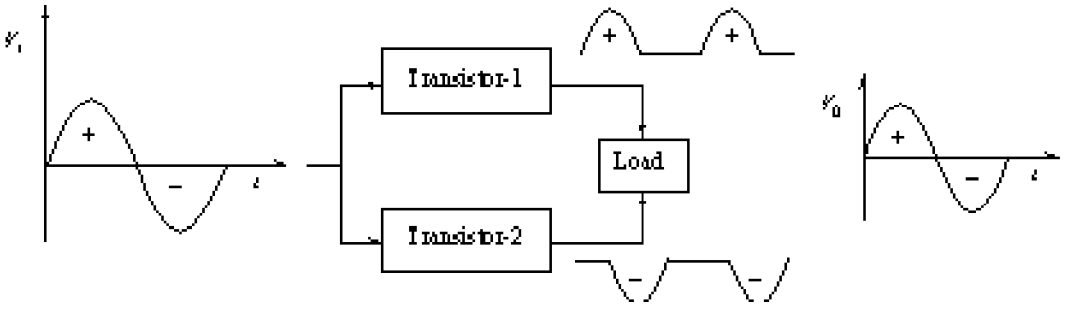


Fig. 3.22A

When an AC signal is applied to the above circuit, with each half operating on alternate half-cycle, the load receives a signal for the full AC signal. The power transistors are used in the push-pull configuration in order to have better power for the load. The class-B operation provides a better efficiency (78.5%) when compared with class-A (50%) operation.

DC Analysis The DC power supplied to the load by an amplifier is given by,

$$P_i(\text{dc}) = V_{CC}\, I_{\text{dc}}$$

I_{dc} = average DC current drawn from the power supply.

where, $I_{\text{dc}} = 2I_P/\pi$

I_P = peak value of the output current waveform.

Therefore, $P_i(\text{dc}) = V_{CC}\,(2/\pi)\, I_P$

AC Analysis Output power is given by,

$$P_0(\text{ac}) = V_{lp-p}^2/8R_L$$

The efficiency of the class-B amplifier can be calculated using the following equation:

$$\eta = P_0(\text{ac})/P_i(\text{dc}) \times 100\%$$

The maximum efficiency that a class-B operation can have is given by,

$$\eta = 78.5\%$$

The power dissipated by the output transistor (individual) is given by,

$$P_Q = [P_0(\text{ac}) - P_i(\text{dc})]/2$$

Disadvantages The main disadvantage of the class-B operation is *'cross-over distortion'*.

Actually, both the transistors never switch off or switch on at the zero voltage condition. Therefore, the output voltage does not follow the input around the zero voltage regions. This problem can be overcome by using class-AB

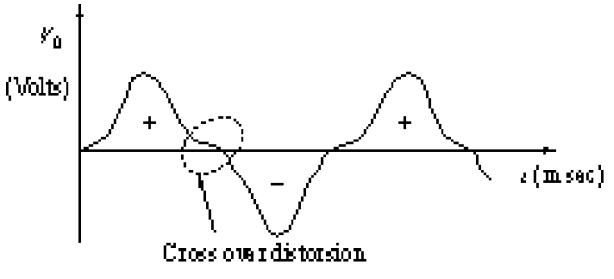


Fig. 3.22B

operation. In case of class-AB operation, the transistor may be biased at a DC level above the zero-base current level of the class-B operation and above one-half the supply voltage level of class-A operation.

Experiment (Class-B Power Amplifier)

Aim: ***To Design and Construct a Class-B (Complementary Symmetry) Power Amplifier and to Determine its Efficiency***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

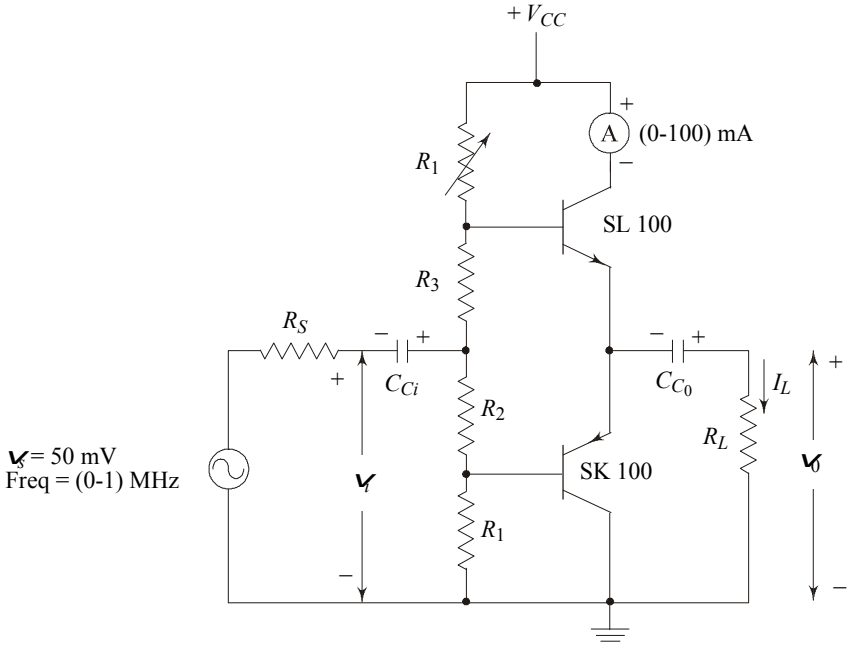


Fig. 3.23

Design:

Given $V_{CC} = 15$ V; $R_L = 470\ \Omega$; $f_L = 500$ Hz; $R_S = 680\ \Omega$

Output voltage is same as the input voltage since two transistors are in CC-mode. Therefore, load voltage is given by,

$$V_L(\text{ac}) = 15 \text{ V}$$

Output power, $P_0(\text{ac}) = V_L^2\ (\text{ac})/2\ R_L = ?$

$$I_L(\text{ac}) = V_L(\text{ac})/R_L = ?$$

The DC current is given by,

$$I_{\text{dc}} = 2/\pi[I_L(\text{ac})] = ?$$

Therefore, the power supplied to the circuit is,

$$P_i(\text{dc}) = V_{CC} I_{\text{dc}} = ?$$

Circuit efficiency, $\eta = P_0(\text{ac})/P_i(\text{dc}) = ?$

Power dissipation by each transistor is given by,

$$P_Q = [P_0(\text{ac}) - P_i(\text{dc})]/2 = ?$$

At DC biasing condition:

$$V_{CE_1} = V_{CE_2} = V_{CC}/2 = ?$$
$$V_{B_1} = V_{BE_1} + V_{CE_2} = ?$$
$$R_1 = [V_{CC} - V_{B_1}]/I_1$$

If I_1 is assumed (say 5 mA), find R_1 = ?

$$R_2(V_{CC}/2)/(R_1 + R_2) = V_{CC}/2 + V_{BE_2}$$

Find R_2 = ?

Input coupling capacitor is given by, $X_{Ci} = Z_{ieff}/10$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find C_i = ?

Output coupling capacitor is given by, $XC_0 = R_L/10$

$$X_{C0} = \frac{1}{2\pi f C_0}$$

Find C_0 = ?

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set V_s = 50 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
8. Calculate the efficiency, $\eta = P_0/P_{in}$.

Tabular Column:

V_s = 50 mV

Frequency	e_0 (volts)	Gain = e_0/e_s	Gain (dB) = 20 log (e_0/e_s)	η

Model Graph: (Frequency Response)

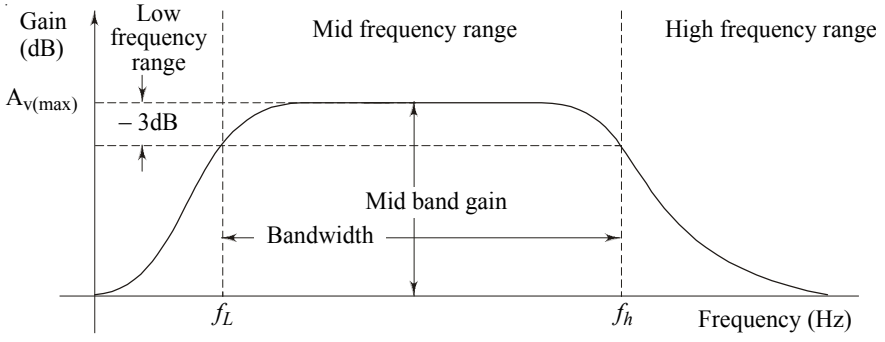


Fig. 3.24

Result:

	Theoretical	Practical
Input impedance		
Output impedance		
Gain (Midband)		
Band width		

3.2.3 Class-C Power Amplifier

In class-C operation, the transistor is biased such a way that it operates for less than 180° of the input signal cycle of output signal for the resonant frequency. This has a limitation of having one fixed frequency. The main application of a class-C operation is in communication.

Experiment (Class-C Power Amplifier)

Aim: ***To Design and Construct a Class-C Amplifier and to Determine its Efficiency***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30)V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

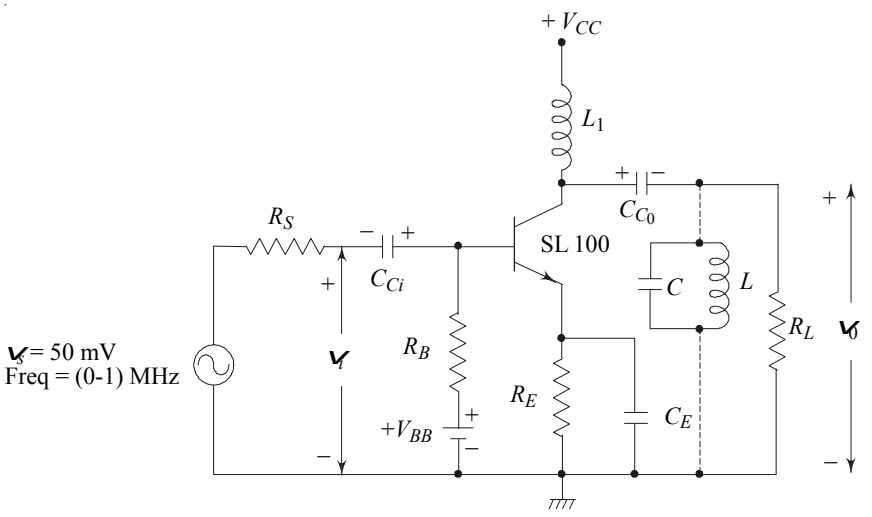


Fig. 3.25

Design:

Given V_{CC} = 15 V; R_L = 470 Ω; f_L = 1 kHz; I_C = 10 mA; $P_{C\max}$ = 4 watt; R_s = 680 Ω

Assume L_1 = 1 Henry; R_S = 680 Ω; R_B = 10 kΩ; V_{BB} = (0-5) V

$$R_L = V_{CC}/I_{C\max} = ?$$

$$P_{C\max} = V_{CEQ}\, I_{CQ}$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

If f_0 is 10 kHz, C = 0.001 μf

Find L = ?

Input coupling capacitor is given by, $X_{Ci} = \{[h_{ie} + (1 + h_{fe})\, R_E] \parallel R_B\}/10$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find C_i = ?

Output coupling capacitor is given by, $X_{C0} = R_L/10$

$$X_{C0} = \frac{1}{2\pi f C_0}$$

Find C_0 = ?

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set V_s = 50 mV (say), using the signal generator.

3. Keeping the input voltage constant, vary the frequency from 0 Hz to1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: fain (dB) vs frequency.
5. Find the input and output impedances
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
8. Calculate the efficiency, $\eta = P_0/P_{in}$.

Tabular Column: v_s = 50 mV

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Model Graph: (Frequency Response)

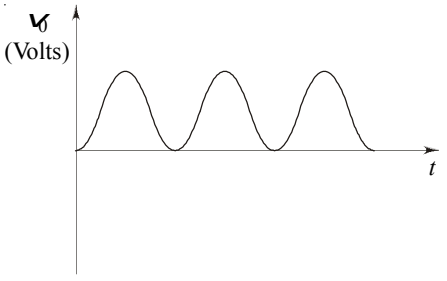


Fig. 3.26

Result:

	Theoretical	Practical
Input impedance		
Output impedance		
Gain (Midband)		
Band width		

3.3 FEEDBACK AMPLIFIER

Feedback amplifier is generally used for feeding a portion of the output signal being feedback into the input signal.

Feedback Connection

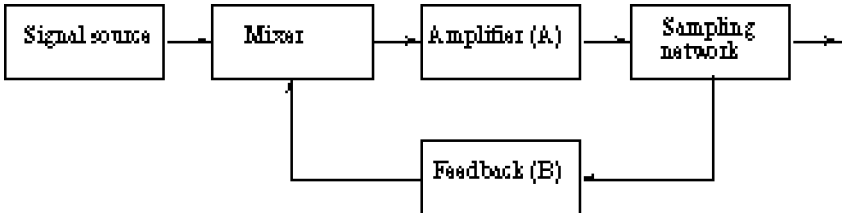


Fig. 3.27

Signal Source This block is either a voltage source (V_S) in series with a source resistance (R_S) or a current source (I_S) in parallel with a source resistance (R_S).

Mixer This block is either a series input from the feedback network (β) or a parallel input from the feedback network (β). In case of series mixer, feedback voltage (V_f) comes in series with the source voltage (V_S). In case of parallel mixer, feedback current (I_f) comes in parallel with the source current (I_S).

Basic Amplifier (A) This block can be any of the following amplifiers.

1. Voltage amplifier.
2. Current amplifier.
3. Trans-conductance amplifier.
4. Trans-resistance amplifier.

Sampling Network This block is either a series output to the feedback network (β) or a parallel output to the feedback network (β). If it is parallel outputing to β-network, it is called voltage sampling or else current sampling.

Feedback Network This block is a two-port network usually containing resistors, capacitors or inductors.

Note The basic amplifier without feedback can be designed by considering the following rule:

Generally, the transistor is modeled using *h*-parameter, which contains input circuit and output circuit.

To Find the Input Circuit:

1. Voltage sampling: Set $V_0 = 0$ V (short-circuit the output terminal)
2. Current sampling: Set $I_0 = 0$ A (open-circuit the output loop)

To Find the Output Circuit:

1. Shunt/parallel mixer: Set $V_i = 0$ V (short-circuit the input terminal)
2. Series mixer: Set $I_i = 0$A (open-circuit the input loop)

Feedback amplifier can be broadly divided into positive feedback and negative feedback depending on the feeding method. If the feedback signal is of opposite polarity to the input signal, negative feedback results. If the feedback signal is of the same polarity to the input signal, positive feedback results.

Positive Feedback: (Re-generative feedback)

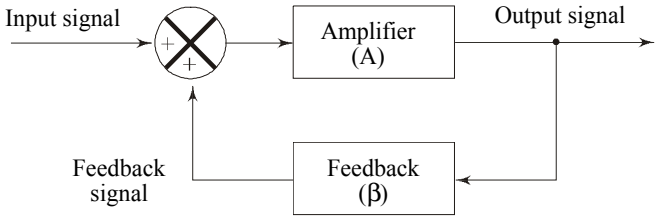


Fig. 3.28

Negative Feedback: (De-generative feedback)

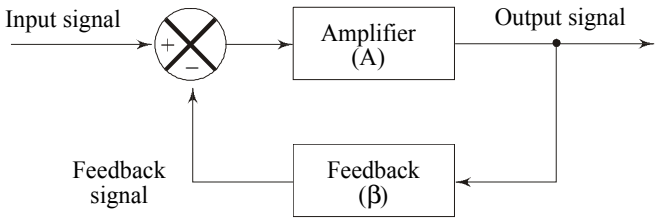


Fig. 3.29

Negative Feedback Features

1. Higher input impedance.
2. Better stability.
3. Lower output impedance.
4. Reduced noise.
5. Better linearity.
6. Improved frequency response (better bandwidth).

Negative feedback can be classified as follows:

1. Voltage amplifier (voltage-series feedback)
2. Current amplifier (current-shunt feedback)
3. Trans-conductance amplifier (current-series feedback)
4. Trans-resistance amplifier (voltage-shunt feedback)

Fundamental Assumption

1. The input signal is transmitted to the output only through amplifier (A) and not through feedback network (β).
2. The feedback signal is transmitted to the input only through feedback network (β) and not through amplifier (A).
3. The feedback factor (β) is independent of the load and the source resistance.

3.3.1 Feedback Classification: (Block Diagram)

1. *Voltage-Series Feedback*

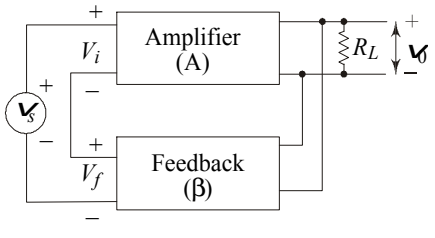


Fig. 3.30

Effect of Feedback

Output resistance : Decreases
Input resistance : Increases
Gain : Voltage amplifier: Decreases

Bandwidth : Increases
Distortion : Decreases

2. *Current-Shunt Feedback*

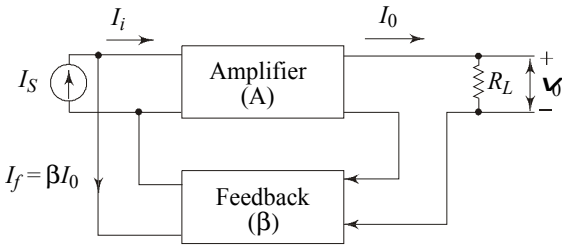


Fig. 3.31

Effect of Feedback

Output resistance : Increases
Input resistance : Decreases
Gain : Current amplifier: Decreases
Bandwidth : Increases
Distortion : Decreases

3. *Current-series Feedback*

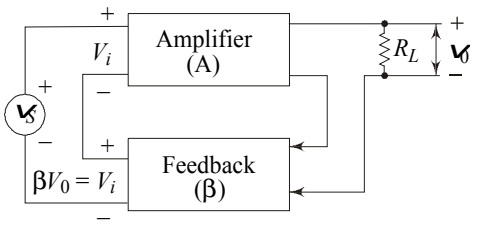


Fig. 3.32

Effect of Feedback

Output resistance : Increases
Input resistance : Increases
Gain : Trans-conductance amplifier: Decreases
Bandwidth : Increases
Distortion : Decreases

4. *Voltage-Shunt Feedback*

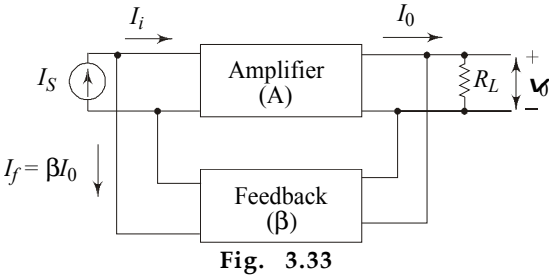


Fig. 3.33

Effect of Feedback

Output resistance	: Decreases
Input resistance	: Decreases
Gain	: Trans-resistance amplifier: Decreases
Bandwidth	: Increases
Distortion	: Decreases

3.3.2 Current-Series Feedback Amplifier

Experiment:

Aim: ***To Design and Test the Current-Series Feedback Amplifier and to Calculate the Following Parameters with and Withot Feedback.***

1. Mid band gain.
2. Bandwidth and cut-off frequencies.
3. Input and output impedance.

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20)MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

Without Feedback

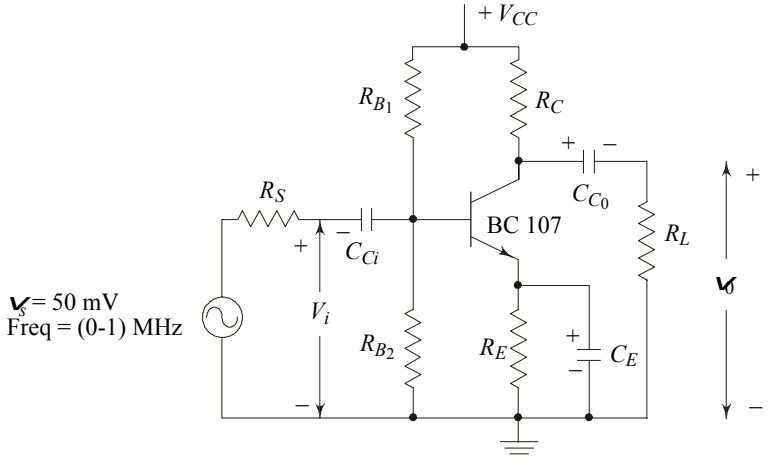


Fig. 3.34

With Feedback

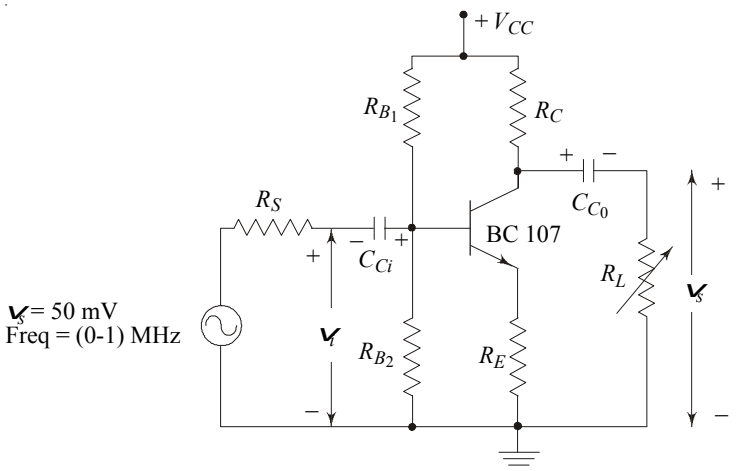


Fig. 3.35

Design (Without Feedback):

Given data: V_{cc} = 15V; I_c = 1 mA; f_L = 1 kHz; Stability factor = [2-10]; R_S = 680 Ω

A_V = 50 dB; I_E = 1.2 mA; β = 0.9

Gain formula is given by,

$$A_V = \frac{-h_{fe}R_{Leff}}{Z_i}$$

Assume, $V_{CE} = V_{CC}/2$ (transistor active)

Effective load resistance is given by, $R_{leff} = R_C \parallel R_L$

Emitter resistance is given by, $r_e = 26\text{ mV}/I_E$

$$h_{ie} = \beta r_e$$

Where, r_e is internal resistance of the transistor.

$$h_{ie} = h_{fe}\, r_e$$

$$V_E = V_{CC}/10$$

On applying KVL to output loop, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

where, $V_E = I_E R_E$

Find R_C = ?

Since I_B is very small when compare with I_C,

$$I_C \simeq I_E$$

$$R_E = V_E/I_E = ?$$

$$V_B = V_{BE} + V_E$$

$$V_B = V_{CC} \frac{R_{B_2}}{R_{B_1} + R_{B_2}}$$

$$S = 1 + \frac{R_B}{R_E}$$

Find $R_B = ?$

$$R_B = R_{B_1} \parallel R_{B_2}$$

Find R_{B_1} and R_{B_2}

Input impedence, $Z_i = (R_B \parallel h_{ie})$

Coupling and by-pass capacitors can be thus found out.

Input coupling capacitor is given by, $X_{Ci} = \frac{Z_i}{10}$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

Output coupling capacitor is given by, $X_{c0} = (R_C \parallel R_L)/10$

$$X_{C0} = \frac{1}{2\pi f C_0}$$

Find $C_0 = ?$

By-pass capacitor is given by, $X_{CE} = R_E/10$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

Design (Feedback):

Remove the emitter capacitor (C_E)

$$\beta = -1/R_E$$

$$G_m = \frac{-h_{fe}}{[(h_{ie} + R_E) \parallel R_B]}$$

$$D = 1 + \beta G_m$$

$$G_{mf} = G_m / D$$

$$A_{Vf} = G_{mf\ Leff}$$

$$Z_{if} = Z_i D$$

$$Z_{0f} = Z_0 D$$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set v_s = 50 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
8. Remove emitter resistance (R_E), i.e., feedback loop, and follow the same procedures (1 to 7).

Tabular Column:

With Feedback:

v_s = 50 mV

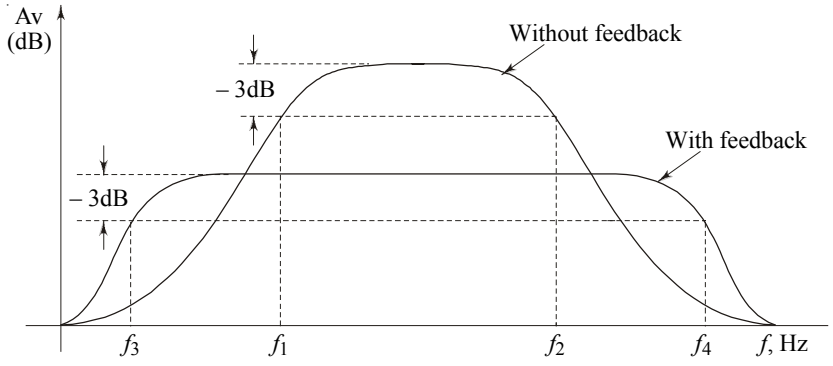
Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Without Feedback:

v_s = 50 mV

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Model Graph: (Frequency Response)



$f_2 - f_1$ = Band width of without feedback circuit

$f_4 - f_3$ = Band width of with feedback circuit

Fig. 3.36 Frequency response

Result:

	Theoretical		Practical	
	With F/B	Without F/B	With F/B	Without F/B
Input impedance	$Z_i = R_{BB} \|\| h_{ie}$	$Z_{if} = Z_i\ D$		
Output impedance	$Z_0 = R_C \|\| R_L$	$Z_{0f} = Z_0\ D$		
Gain (Midband)				
Band width				
Transconductance (Gm)				

3.3.3 Voltage-Series Feedback Amplifier

Experiment:

Aim: ***To Design and Test the Voltage-Series Feedback Amplifier and to Calculate the Following Parameters with and Without Feedback***

1. Mid band gain.
2. Bandwidth and cut-off frequencies.
3. Input and output impedance.

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram: Without Feedback

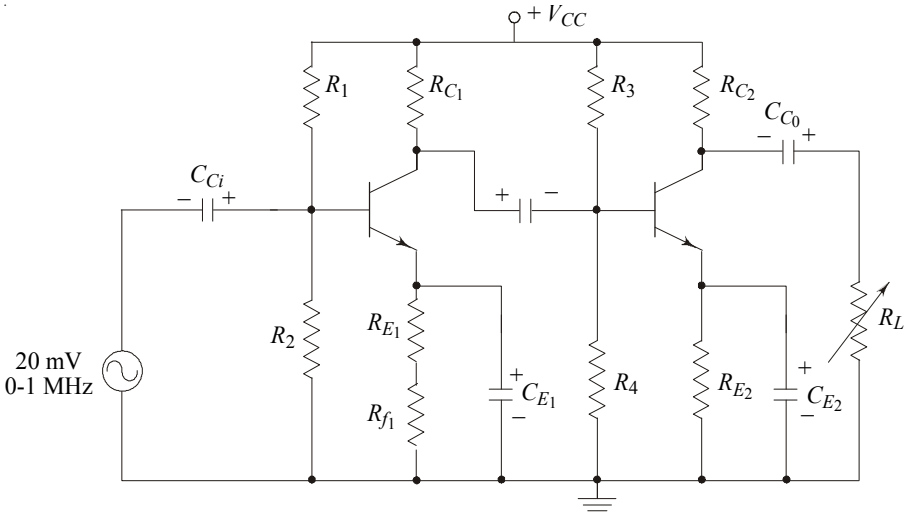


Fig. 3.37

With Feedback

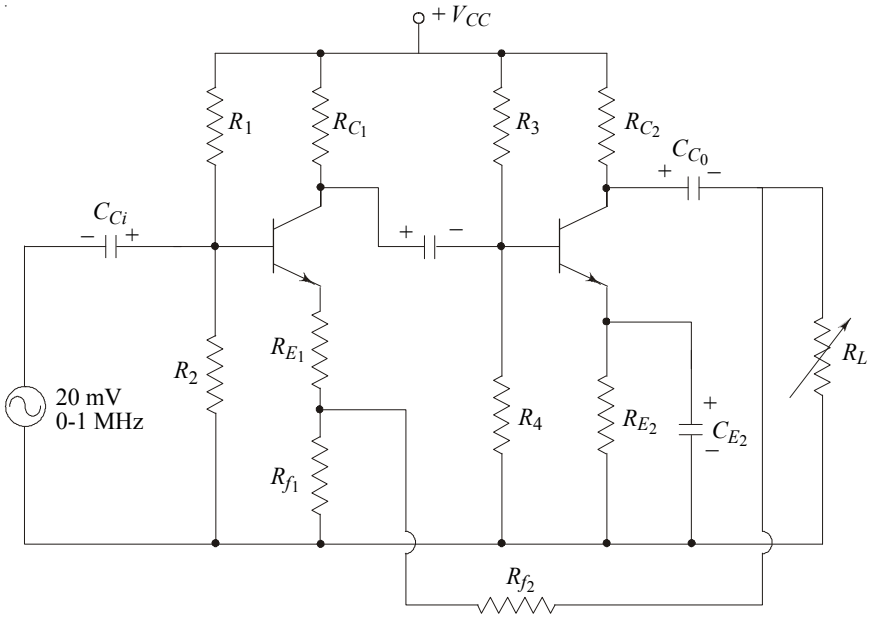


Fig. 3.38

Given: V_{CC} = 12 V, AV_1 = 30 dB; AV_2 = 20 dB; I_{E_1} = 3 mA; I_{E_2} = 2 mA; S = 110; β = 0.05; $h_{fe_1} = h_{fe_2} = 200$

Without feedback design: Analysis of second stage

For active operation of a transistor,

$$V_{CE} = \frac{V_{CC}}{2},\ V_E = \frac{V_{CC}}{10}$$

$$V_{CC} = I_{C_2} R_{C_2} + V_{CE_2} + V_{E_2}$$

$$R_{C_2} = ?$$

$$R_{E_2} = \frac{V_{E_2}}{I_{E_2}} = ?$$

$$V_{B_2} = V_{BE_2} + V_{E_2}$$

$$R_{B_2} = (S - 1)\ R_E$$

$$R_B = R_3 \parallel R_4$$

Calculate $R_3 = ?;\ R_4 = ?$

$$Z_i = R_{B_2} \parallel h_{ie_2}$$

$$A_{V_2} = \frac{-h_{fe_2}\ R_{Leff_2}}{Z_{i_2}}$$

$$R_{Leff_2} = R_{c_2} \parallel R_L = Z_{0_2}$$

$$R_L = ?$$

$$h_{ie_2} = r_e \times h_{ie_2}$$

$$r_e = \frac{26 \text{ mV}}{I_E}$$

Analysis of first stage

$$A_{V_1} = \frac{-h_{fe_2} R_{Leff_1}}{Z_{i_1}}$$

$$R_{ieff} = R_{C_1} \parallel Z_{i_2}$$

$$R_{C_1} = ?$$

$$V_{CC} = I_{C_1} R_{C_1} + V_{CE_1} + V_{E_1}$$

$$R_{E_1} = ?$$

$$V_{B_1} = V_{BE_1} + V_{E_1}$$

$$R_{B_1} = (S - 1) R_{E_1}$$

$$R_{B_1} = R_1 \parallel R_2$$

Calculate $R_1 = ?, R_2 = ?$

$$\beta = \frac{R_{f_1}}{R_{f_1} + R_{f_2}}$$

Assume, $R_{f_2} >. R_{f_1}$

$A_V = A_{V_1} \times A_{V_2}$ [In dB, $A_V = A_{V_1} + A_{V_2}$]

$D = 1 + A\beta$

$$Z_{of} = \frac{Z_0}{D}$$

$$Z_{if} = Z_i/D$$

$$A_{Vf} = A_V/D$$

To calculate capacitors

$$X_{CE_2} = \frac{R_{E_2}}{10} = \frac{1}{2\pi f C_{E_2}}$$

$$C_{E_2} = ?$$

$$X_{CO_2} = \frac{Z_{i_2}}{10} = \frac{1}{2\pi f C_{E_2}}$$

$$C_{O_2} = ?$$

$$X_{C_i} = \frac{Z_{0_1}}{10} = \frac{1}{2\pi f C_{i_1}}$$

$$C_{i_1} = ?$$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set v_s = 1 V (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
8. Shift the emitter resistance (R_E) to the collector (in series with R_C) and follow the same procedures (1 to 7).

Tabular Column:

With Feedback:

v_s = 1 V

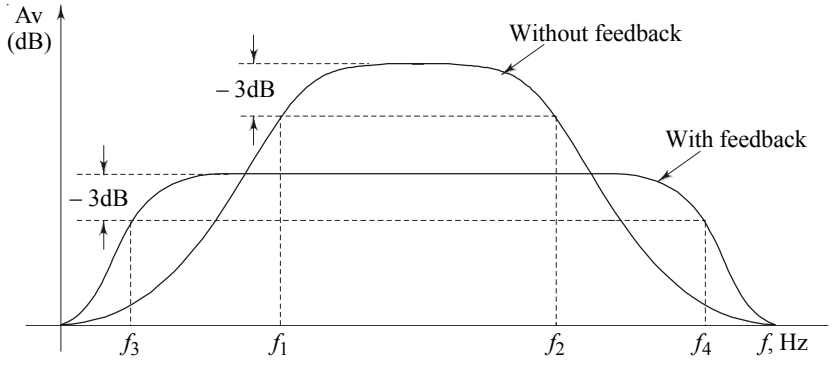
Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Without Feedback:

v_s = 1 V

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Model Graph: (Frequency Response)



$f_2 - f_1$ = Band width of without feedback circuit

$f_4 - f_3$ = Band width of with feedback circuit

Fig. 3.39

Result:

	Theoretical		Practical	
	With F/B	Without F/B	With F/B	Without F/B
Input impedance	$Zi_{eff} = Z_i = R_{BB}$	$Z_{if} = Z_i\ D$		
Output impedance	$Z_0 = R_E \parallel R_L$	$Z_{0f} = Z_0\ D$		
Gain (Midband)				
Band width				

3.3.4 Current-Shunt Feedback Amplifier

Experiment:

Aim: ***To Design and Test the Current-Series Feedback Amplifier and to Calculate the Following Parameters with and Without Feedback***

1. Mid band gain.
2. Bandwidth and cut-off frequencies.
3. Input and output impedance.

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30)V	1
CRO	(0-20) MHz	
Function generator	(0-1) MHz	1

Circuit Diagram:

Without Feedback

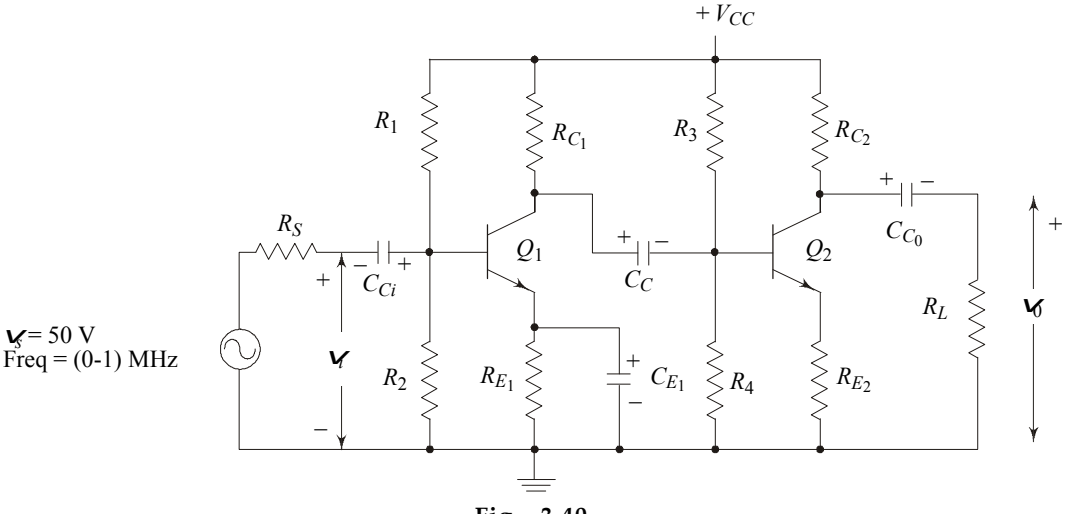


Fig. 3.40

With Feedback

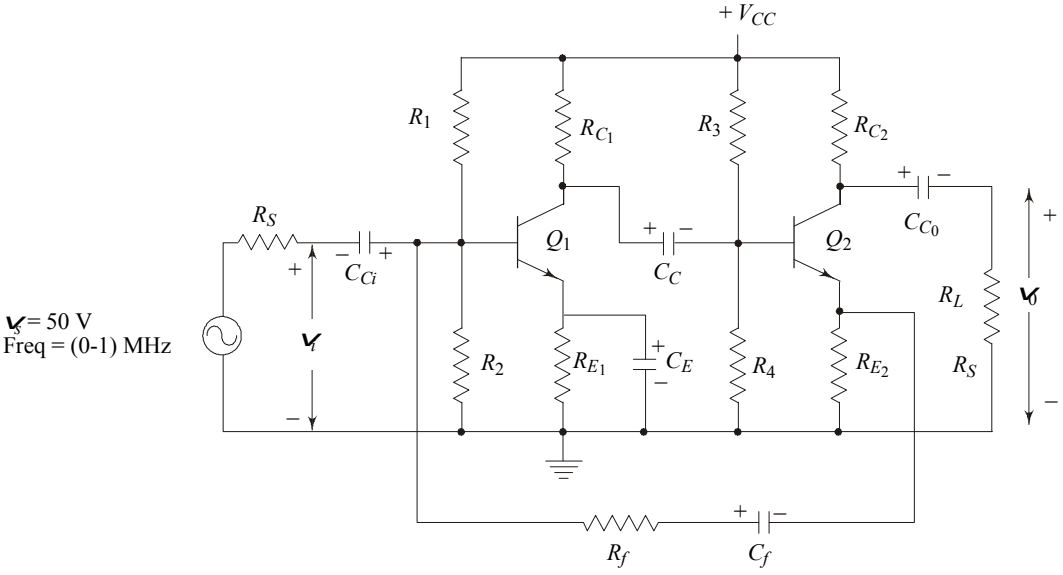


Fig. 3.41

Design (Without Feedback):

Given data: V_{CC} = 15 V; I_{C_1} = 1 mA; f_L = 1 kHz; Stability factor = [2-10]; R_S = 680 Ω

R_L = 4.7 kΩ; A_{V_1} = 10 dB; A_{V_2} = 20 dB; I_{C_2} = 5 mA

$r_{e_2} = 26 \times 10^{-3} / I_{E_2} = 26$

$h_{ie_2} = h_{fe_2} \times r_{e_2} = 200 \times 26 = 5.2$ kΩ h_{fe_2} = 200 (from multimeter/transistor data manual)

From DC bias analysis, on applying KVL to the output loop, we get

$$V_{CC} = I_{C_2} R_{C_2} + V_{CE_2} + V_{E_2}$$

$V_{CE_2} = V_{CC}/2$; $V_{E_2} = V_{CC}/10$; $I_{C_2} = 1 \times 10^{-3}$ A

R_{C_2} = ?

$$V_{E_2} = I_{E_2} R_{E_2}$$

Calculate R_{E_2}.

Since I_B is very small when compare with I_C

$$I_{C_2} \simeq I_{E_2}$$

$$A_{V_2} = \frac{-h_{fe_2} R_{Leff}}{h_{ie_2} + (1 + h_{fe_2}) R_{E2}}$$

$$R_{Leff} = R_{C_2} \parallel R_L$$

Find, $R_L \parallel R_{C_2}$ from above equation.

Since, R_{C_2} is known, calculate R_L.

$$S = 1 + \frac{R_{B2}}{R_{E_2}}$$

Find $R_{B_2} = ?$

$$R_{B_2} = R_3 \parallel R_4$$

$$V_{B_2} = V_{CC} \frac{R_3}{R_4 + R_3}$$

$$V_{B_2} = V_{BE_2} + V_{E_2}$$

Find $R_3 = ?$

Therefore, find $R_4 \rightarrow Z_{i_2} = R_{B_2} \parallel [h_{ie_2} + (1 + h_{fe_2})\, R_{E_2}]$

Find, $Z_{i_2} = ?$

$$R_{Leff_1} = Z_{i_2} \parallel R_{C_1}$$

Find R_{Leff_1} from the gain formula given above

$$A_{V_1} = \frac{-h_{fe_1} R_{Leff}}{Z_{i_1}}$$

Find $R_{Leff_1} = R_{C_1} \parallel Z_{i_2}$

On applying KVL to the first stage, we get

$$V_{CC} = I_{C_1} R_{C_1} + V_{CE_1} + V_{E_1};\ \ V_{CE_1} = \frac{V_{CC}}{2}$$

Find $R_{E_1} = ?$

$$S = 1 + \frac{R_{B_1}}{R_{E_1}}$$

Find $R_{B_1} = ?$

$$R_{B_1} = R_1 \parallel R_2$$

$$V_{B_1} = V_{CC} \frac{R_2}{R_1 + R_2} = \frac{V_{CC}\ R_{B_1}}{R_1}$$

$$V_{B_1} = V_{BE_1} + V_{E_1}$$

Find $R_1 = ?$

Therefore, find R_2

$$Z_{i_1} = h_{ie_1} \parallel R_{B_1}$$

Total gain including source resistance is given by,

$$X_{Ci} = \frac{Z_{i_1}}{10} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

$$X_{C_0} = (R_{C_2} \parallel R_{L_2})/10 = \frac{1}{2\pi f C_0}$$

Find $C_0 = ?$

$$X_{CE} = R_E/10 = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

Design (With Feedback):

Assume $R_f = 48\ \text{k}\Omega$

$$X_{Cf} = R_f/10 = \frac{1}{2\pi f C_f}$$

$$C_f = ?$$

$$\beta = -R_{E_2}/[R_f + R_{E_2}]$$

$$D = 1 + \beta A_I$$

where,

$$A_I = h_{fe_1} \times h_{fe_1} \times \frac{R_{C_1} \parallel R_{B_2}}{Z_{i_2} + \left(R_{C1} \parallel R_{B_2}\right)}$$

$$A_{If} = A_I/D$$

$$A_{Vf} = A_{If}\,(R_C \parallel R_L)/R_S$$

$$Z_{if} = Z_i/D$$

$$Z_{0f} = Z_0 D$$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set v_s = 50 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
8. For feedback condition, connect feedback resistance (R_f) in series with feedback capacitor (C_f), i.e., feedback loop, and follow the same procedures (1 to 7).

Tabular Column:

With Feedback:

v_s = 50 mV

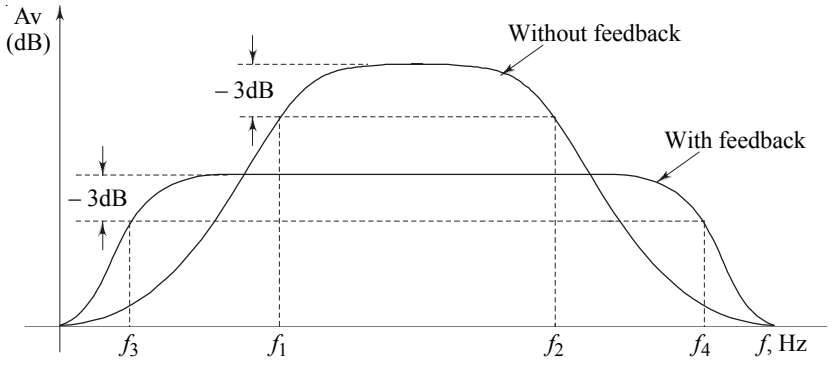
Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Without Feedback:

v_s = 50 mV

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Graph: (Frequency Response)



$f_2 - f_1$ = Band width of without feedback circuit

$f_4 - f_3$ = Band width of with feedback circuit

Fig. 3.42

Result:

	Theoretical		Practical	
	With F/B	Without F/B	With F/B	Without F/B
Input impedance	$Z_i = R_{BB} \|\| h_{ie}$	$Z_{if} = Z_i D$		
Output impedance	$Z_0 = R_C \|\| R_L$	$Z_{0f} = Z_0 D$		
Gain (Midband)				
Band width				
Current gain A_I				

3.3.5 Voltage-Shunt Feedback Amplifier

Experiment:

Aim: ***To Design and Test the Voltage-Shunt Feedback Amplifier and to Calculate the Following Parameters with and Without Feedback***

1. Mid band gain.
2. Bandwidth and cut-off frequencies.
3. Input and output impedance.

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30)V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

Without Feedback

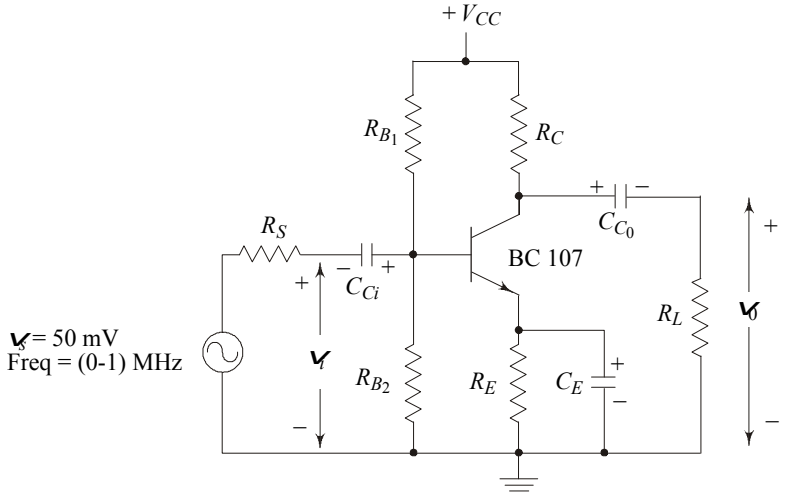


Fig. 3.43

With Feedback

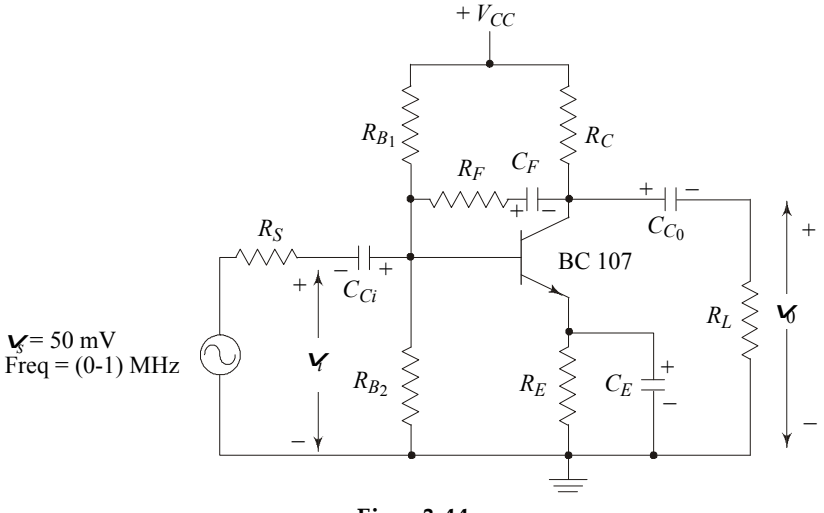


Fig. 3.44

Design (Without Feedback):

Given data: V_{CC} = 15 V; I_C = 1 mA; Av; f_L = 1 kHz; Stability factor = [2-10];
R_S = 680 Ω

A_V = 40 dB

Gain formula is given by,

$$A_V = \frac{-h_{fe}R_{Leff}}{Z_i}$$

Assume, $V_{CE} = V_{CC}/2$ (transistor active)

Effective load resistance is given by, $R_{leff} = R_C \parallel R_L$

Emitter resistance is given by, r_e = 26 mV/ I_E

$$h_{ie} = \beta r_e$$

where, r_e is internal resistance of the transistor.

$$h_{ie} = h_{fe}\, r_e$$

$$V_E = V_{CC}/10$$

On applying KVL to output loop, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

where, $V_E = I_E R_E$

Find R_C = ?

Since I_B is very small when compared with I_C,

$$I_C \simeq I_E$$

$$R_E = V_E/I_E$$

$$V_B = V_{BE} + V_E$$

$$V_B = V_{CC}\frac{R_{B_2}}{R_{B_1} + R_{B_2}}$$

$$S = 1 + \frac{R_B}{R_E}$$

Find R_B = ?

$$R_B = R_{B_1} \parallel R_{B_2}$$

Find R_{B_1} and R_{B_2}

Input impedence, $Z_i = (h_{ie} \parallel R_B)$

Coupling and by-pass capacitors can be thus found out.

Input coupling capacitor is given by, $X_{Ci} = \dfrac{Z_i}{10}$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

Output coupling capacitor is given by, $X_{C_0} = (R_C \parallel R_L)/10$

$$X_{C_0} = \frac{1}{2\pi f C_0}$$

Find $C_0 = ?$

By-pass capacitor is given by, $X_{CE} = R_E/10$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

Design (With Feedback):

Connect the feedback resistance (R_f) and feedback capacitor (C_f) as shown in the figure.

$$X_{Cf} = R_f/10$$

$$C_f = R_f/2\pi f \times 10$$

Assume, $R_f = 68\ \text{k}\Omega$ (large value)

$$\beta = -1/R_f$$

Trans-resistance, $$R_m = \frac{-h_{fe}\left(R_B \parallel R_f\right)\left(R_C \parallel R_f\right)}{\left(R_B \parallel R_f\right) + h_{ie}}$$

$$D = 1 + \beta R_m \qquad R_{mf} = R_m/D$$

$$A_{Vf} = R_{mf}/R_S \qquad Z_{if} = Z_i/D$$

$$Z_{0f} = Z_0/D$$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set v_s = 50 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
8. Remove emitter resistance (R_E), i.e., feedback loop, and follow the same procedures (1 to 7).

Tabular Column:

With Feedback:

v_s = 50 mV

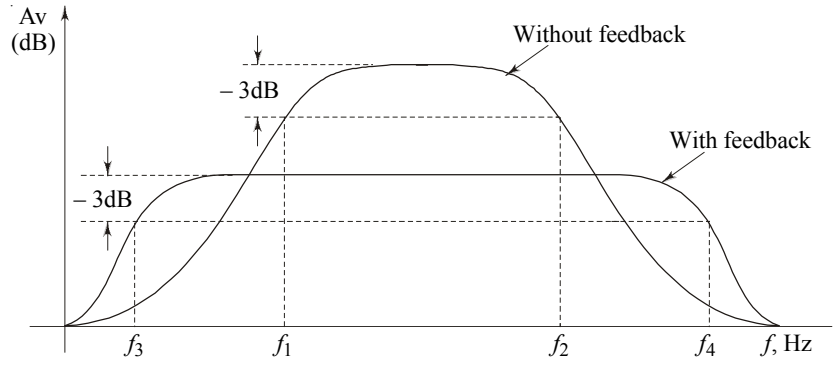
Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Without Feedback:

v_s = 50 mV

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Graph: (Frequency Response)



$f_2 - f_1$ = Band width of without feedback circuit

$f_4 - f_3$ = Band width of with feedback circuit

Fig. 3.45

Result:

	Theoretical		Practical	
	With F/B	Without F/B	With F/B	Without F/B
Input impedance	$Z_i = R_{BB} \| h_{ie}$	$Z_{if} = Z_i D$		
Output impedance	$Z_0 = R_C \| R_L$	$Z_{0f} = Z_0 D$		
Gain (Midband)				
Band width				

3.4 OSCILLATORS

An oscillator is an amplifier with positive feedback. i.e., a part of the output feedback to the input (in-phase). The closed-loop gain, $A\beta > 1$. In an oscillator, the value of loop gain, $A\beta > 1$,

when the power is first turned on. Some of the free electrons pick up extra energy due to ambient temperature and start moving randomly in different directions and generate a noise voltage. This noise voltage contains frequencies of all harmonics that are amplified and feedback to the input in-phase with the original signal. This in turn increases the magnitude of the input voltage. This repeats for several cycles, resulting in an input voltage. This again repeats for several cycles, resulting in a signal of many frequencies. Due to the resonance in the tank circuit (*RC* / *RL* / *LC*), a particular frequency signal is selected and the remaining signals are suppressed completely. In this way, we get oscillation at only one frequency. After the output voltage reaches a desired level, the value of $A\beta$ automatically decreases to the unity, and the output amplitude remains constant. In order to have better stability and the above mentioned condition, a negative feedback is introduced (emitter resistance parallel with a capacitor in the amplifier circuit).

Generally, *RC*-coupled amplifier is used for the amplification purpose (discrete circuit). This will introduce a phase difference of 180°. For the oscillation, a positive feedback should be introduced. This can be obtained by connecting a tank circuit in such a way that it will introduce the remaining 180° phase shift to complete 360° or 0° between input and output voltage.

Oscillators can identified in many frequency ranges like audio oscillators, *RF* oscillators, microwave oscillators, etc.

3.4.1 Wein-Bridge Oscillator

The wein-bridge oscillator generally finds its prime application in audio frequency range. It is also preferred for low-frequency applications.

The wein-bridge oscillator uses a lead-lag network as a feedback network.

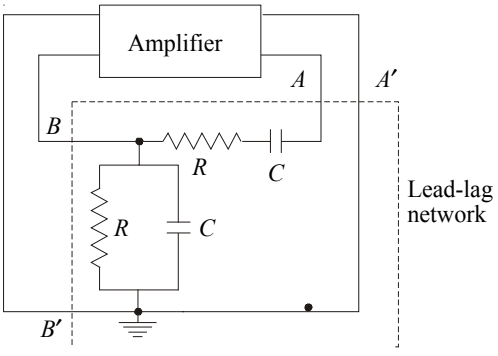


Fig. 3.46

At very low frequencies, the phase angle is positive and the circuit acts like a lead network. At very high frequencies, the phase angle is negative and the circuit acts like a lag network. In between, there is a resonant frequency with 0°-phase shift. The lead-lag network acts as a resonant circuit. Hence, the circuit oscillates to a particular frequency.

The amplifier follows simple *RC*-coupled amplifier design, which we already explained. Let us consider the feedback (lead-lag) network.

Design (Feedback Network):

$$\beta = \frac{V_0(s)}{V_i(s)}$$

$$V_0(s) = \frac{V_i(s)\left[R \,||\left(\frac{1}{Cs}\right)\right]}{\left[R + \left(\frac{1}{Cs}\right)\right] + \left[R \,||\left(\frac{1}{Cs}\right)\right]}$$

$$\frac{V_0(s)}{V_i(s)} = \frac{1}{3 + j\left[RC\omega - \left(\frac{1}{RC\omega}\right)\right]} \qquad (1)$$

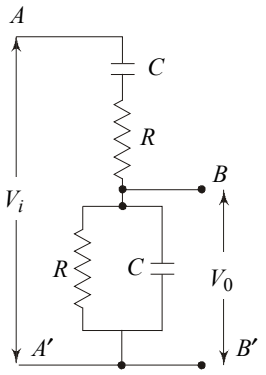


Fig. 3.47

Equating imaginary part to zero, we get

$$RC\omega - (1/RC\omega) = 0$$

where, $\omega = 1/RC$

$$f_0 = \frac{1}{2\pi RC}$$

Substituting $\omega = 1/RC$ in equation (1), we get

$$\beta(s) = \frac{V_0(s)}{V_i(s)} = \frac{1}{3}$$

Since, $A = 1/\beta(s) = 3$

Experiment (Wein-Bridge Oscillator)

Aim: ***To Design and Construct a Wein-Bridge Oscillator for a Given Cut-Off Frequency***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20) MHz	1

Circuit Diagram:

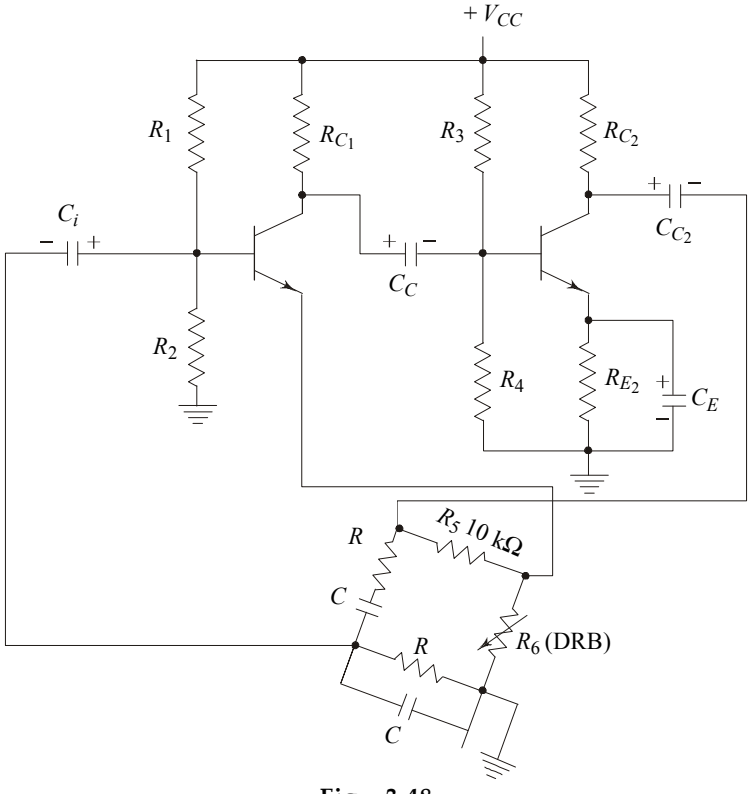


Fig. 3.48

Design:

Given $V_{CC} = 12$ V; $f_0 = 2$ kHz; $S = [0–10]$; $f_L = 100$ Hz; $I_{C_1} = I_{C_2} = 1$mA

When the bridge is balanced,

$$f_0 = \frac{1}{2\pi RC}$$

Assume, $C = 0.1$ μF

Find, $f_0 = ?$

Given data: $V_{CC} = 15$ V; $I_{C_1} = I_{C_2} = 1$ mA; $A_{V_T} = 3$; $A_{V_1} = 2$; $A_{V_2} = 1$; $f_L = 50$ Hz;

stability factor = [10]

$$A_{V_2} = \frac{-h_{fe_2} R_{Leff}}{Z_{i_2}}$$

$$R_{leff} = R_{C_2} \parallel R_L$$

$$h_{fe_2} = 200 \text{ (from multimeter)}$$

$$r_{e_2} = 26 \times 10^{-3}/I_{E_2} = 26$$

$$h_{ie_2} = h_{fe_2} \times r_{e_2} = 200 \times 26 = 5.2 \text{ kW}$$

From dc bias analysis, on applying KVL to the output loop, we get

$$V_{CC} = I_{C_2} R_{C_2} + V_{CE_2} + V_{E_2}$$

$$V_{CE_2} = V_{CC}/2;\ V_{E_2} = V_{CC}/10;\ I_{C_2} = 1 \times 10^{-3}\text{A}$$

$$R_{C_2} = ?$$

Since I_B is very small when compare with I_C

$$I_C \simeq I_E$$

$$A_{V_2} = \frac{-h_{fe_2} R_{Leff}}{Z_{i_2}}$$

Find, $R_L \parallel R_{C2}$ from above equation.

Since R_{C2} is known, calculate R_L.

$$V_{E_2} = I_{E_2} R_{E_2}$$

Calculate R_{E_2}

$$S = 1 + \frac{R_{B_2}}{R_{E_2}}$$

Find $R_{B_2} = ?$

$$R_{B_2} = R_3 \parallel R_4$$

$$V_{B_2} = V_{CC} \frac{R_4}{R_3 + R_4}$$

$$V_{B_2} = V_{BE_2} + V_{E_2}$$

Find $R_3 = ?$

Therefore, find R_4

$$Z_{i_2} = h_{ie_2} \parallel R_{B_2}$$

Find, $Z_{i_2} = ?$

$$R_{Leff_1} = Z_{i_2} \parallel R_{C_1}$$

Find R_{Leff1} from the gain formula given above

$$A_{V_1} = \frac{-h_{fe_1} R_{Leff_1}}{Z_{i_1}}$$

Find $R_{Leff_1} = ?$

On applying KVL to the first stage, we get

$$V_{CC} = I_{C_1} R_{C_1} + V_{CE_1} + V_{E_1};\ V_{CE_1} = \frac{V_{CC}}{2};\ V_{E_1} = \frac{V_{CC}}{10}$$

Find $R_{C_1} = ?$

Since $I_{C_1} \simeq I_{E_1}$

Find $R_6 = R_{E_1} = ?$

$$S = 1 + \frac{R_{B_1}}{R_{E_1}}$$

Find $R_{B_1} = ?$

$$R_{B_1} = R_1 \| R_2$$

$$V_{B_1} = V_{CC} \frac{R_2}{R_1 + R_2}$$

$$V_{B_1} = V_{BE_2} + V_{E_2}$$

Find $R_1 = ?$

Therefore, find $R_2 = ?$

$$Z_{i_1} = h_{ie_1} \parallel R_{B_1}$$

$$R_5 = R_L - R_6$$

$$X_{Ci} = \frac{Z_{i_1}}{10}$$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

$$X_{C0} = (R_{C_2} \parallel R_{L_2})/10$$

$$X_{C0} = \frac{1}{2\pi f C_0}$$

Find $C_0 = ?$

$$X_{CE} = R_{E_2}/10$$

$$X_{CE} = \frac{1}{2\pi f C_{E_2}}$$

Find $C_E = ?$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare it with its theoretical frequency.

Result:

	Theoretical	Practical
Frequency		

3.4.2 RC Phase Shift Oscillator

Phase shift oscillator consists of an amplifier with three-lead network in the feedback path. Since an amplifier introduces 180° phase shift between input and output, the remaining 180° phase shift is compensated by connecting three RC combinations. [180°/3 = 60° each]. Phase shift oscillator finds application in low-frequency range. Let us consider the feedback path,

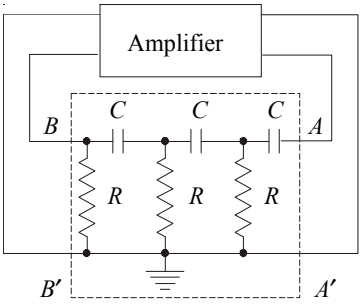


Fig. 3.49

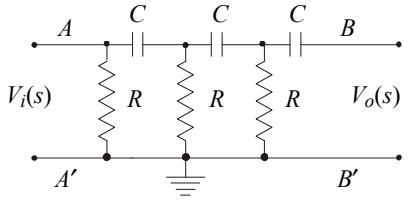


Fig. 3.50

$$RI = \text{V}$$

$$\begin{bmatrix} R + \frac{1}{Cs} & -R & 0 \\ -R & 2R + \frac{1}{Cs} & -R \\ 0 & -R & 2R + \frac{1}{Cs} \end{bmatrix} \begin{bmatrix} I_3 \\ I_2 \\ I_1 \end{bmatrix} = \begin{bmatrix} V_i(s) \\ 0 \\ 0 \end{bmatrix}$$

$$\Delta = \left[R + \frac{1}{Cs}\right]\left[\left(2R + \frac{1}{Cs}\right)^2 - R^2\right] + R\left[-2R^2 - \frac{R}{Cs}\right]$$

$$\Delta = \frac{6R^2}{Cs} + \frac{5R}{(Cs)^2} + R^3 + \frac{1}{(Cs)^3}$$

$$\Delta I_1 = \begin{bmatrix} R + \frac{1}{Cs} & -R & V_i(s) \\ -R & 2R + \frac{1}{Cs} & 0 \\ 0 & -R & 0 \end{bmatrix}$$

$$\Delta I_1 = V_i(s)\, R^2$$

$$I_1 = \Delta I_1 / \Delta$$

$$I_1 = \frac{V_i(s)R^2}{\left[\frac{6R^2}{Cs} + \frac{5R}{(Cs)^2} + R^3 + \frac{1}{(Cs)^3}\right]}$$

$$V_0(s) = RI_1 = \frac{V_i(s)R^3}{\left[\frac{6R^2}{Cs} + \frac{5R}{(Cs)^2} + R^3 + \frac{1}{(Cs)^3}\right]}$$

$$\beta = \frac{V_0(s)}{V_i(s)} = \frac{R^3}{\left[\frac{6R^2}{Cs} + \frac{5R}{(Cs)^2} + R^3 + \frac{1}{(Cs)^3}\right]}$$

$$\beta = \frac{1}{1 - \frac{5}{R^2C^2\omega^2} - j\left[\frac{6}{RC\omega} - \frac{1}{(RC\omega)^3}\right]} \tag{1}$$

Equating imaginary part to zero, we get,

$$\frac{6}{RC\omega} - \frac{1}{(RC\omega)^3} = 0$$

$$\frac{6}{RC\omega} = \frac{1}{(RC\omega)^3}$$

$$\omega = \frac{1}{\sqrt{6}RC} \tag{2}$$

$$f = \frac{1}{2\pi\sqrt{6}RC}$$

Substituting Equation (2) in Equation (1), we get

$$\beta(s) = \frac{1}{1 - \frac{5}{R^2C^2 \times \frac{1}{6R^2C^2}}}$$

$$\beta(s) = -\frac{1}{29}$$

$$A = \frac{1}{\beta} = -29$$

Experiment (RC Phase Shift Oscillator)

Aim: ***To Design and Construct a RC Phase Shift Oscillator for Given Operating Frequency, f_0.***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20) MHz	1

Circuit Diagram:

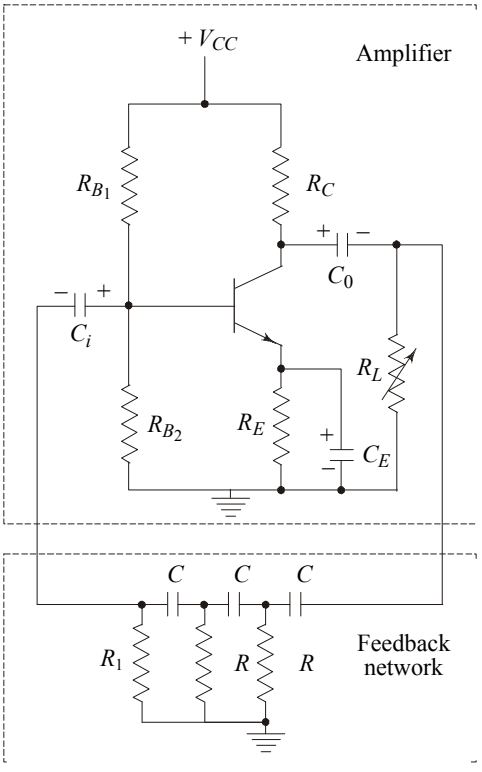


Fig. 3.51

Design:

Given $f_0 = 1$ kHz; $C = 0.01$ μF; $V_{CC} = 12$ V; $A_V = 29$; $S = 10$; $I_E = 5$ mA

$$f = \frac{1}{2\pi RC}$$

Find, $R = ?$

$$R_1 = (R_i - R)$$

$$R >> R_C$$

$$\beta(s) = -\frac{1}{29}$$

$$A = \frac{1}{\beta} = -29$$

Amplifier Design:

Gain formula is given by,

$$A_V = \frac{-h_{fe} R_{Leff}}{h_{ie}} \quad (A_V = 29, \text{ design given})$$

Assume, $V_{CE} = V_{CC}/2$ (transistor active)

Effective load resistance is given by, $R_{leff} = R_C \parallel R_L$

Emitter resistance is given by, $r_e = 26 \text{ mV}/I_E$

$$h_{ie} = \beta r_e$$

where, r_e is internal resistance of the transistor.

$$h_{ie} = h_{fe}\, r_e$$

$$V_E = V_{CC}/10$$

On applying KVL to output loop, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

where, $V_E = I_E R_E$

Find $R_C = ?$

Since I_B is very small when compare with I_C,

$$I_C \simeq I_E$$

$$R_E = V_E/I_E$$

$$V_B = V_{BE} + V_E$$

$$V_B = V_{CC} \frac{R_{B_2}}{R_{B_1} + R_{B_2}}$$

$$S = 1 + \frac{R_B}{R_E}$$

Find $R_B = ?$

$$R_B = R_{B_1} \parallel R_{B_2}$$

Find R_{B_1} and R_{B_2}

Input impedence, $Z_i = (h_{ie} \parallel R_B)$

Input coupling capacitor is given by, $X_{Ci} = \left(\frac{Z_i}{10}\right)$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

$$X_{C0} = \frac{1}{2\pi f C_0}$$

Find $C_0 = ?$

By-pass capacitor is given by, $X_{CE} = R_E/10$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare it with its theoretical frequency.

Result:

	Theoretical	Practical
Frequency	$f = \frac{1}{2\pi\sqrt{6RC}}$	

3.4.3 Hartely Oscillator

The Hartely and Colpitt oscillators find their prime application above audio range. It is a LC oscillator, that can be used for frequencies between 1 MHz to 500 MHz efficiently. Since this frequency range is beyond the allowed operating frequency range of most op-amps (μA 741), BJT or FET is typically used for the amplifier design.

As a whole, Hartely oscillator has two blocks:

1. Amplifier.
2. Feedback network.

Amplifier It is a simple RC coupled amplifier. Design requirement and details are given in the previous experiments.

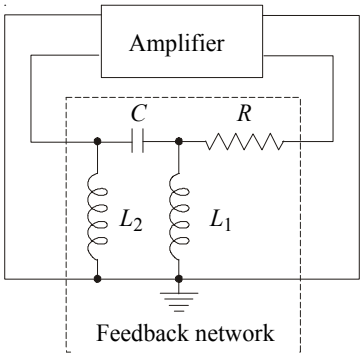


Fig. 3.52

Feedback Network Let us consider the feedback network,

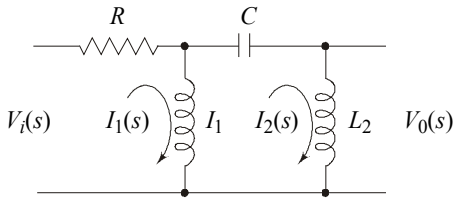


Fig. 3.53

$$RI = \mathrm{V}$$

$$\begin{bmatrix} R + L_1 s & -L_1 s \\ -L_1 s & (L_1 + L_2)s + \dfrac{1}{Cs} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_i(s) \\ 0 \end{bmatrix}$$

$$\Delta = [R + L_1 s]\left[(L_1 + L_2)s + \frac{1}{Cs}\right] - L_1^2 s^2$$

$$\Delta I_2(s) = \begin{bmatrix} R + L_1 s & V_i(s) \\ -L_1 s & 0 \end{bmatrix}$$

$$\Delta I_2(s) = V_i(s) L_1 s$$

$$I_2(s) = \frac{V_i(s)\, L_1 s}{(R + L_1 s)\left[(L_1 + L_2)s - \dfrac{1}{Cs}\right] + L_1^2 s^2}$$

$$V_0(s) = I_2\, L_2 s$$

$$\beta = \frac{V_0(s)}{V_i(s)} = \frac{-L_1 L_2 s^2}{Rs\, L_1 + Rs\, L_2 + L_1 L_2 s^2 + \dfrac{L_1}{C} + \dfrac{R}{Cs}}$$

$$\beta = \frac{-L_1 L_2 \omega^2}{jR\omega\,(L_1 + L_2) - L_1 L_2 \omega^2 + \dfrac{L_1}{C} - j\,\dfrac{R}{C\omega}} \tag{1}$$

Equating imaginary part to zero, we get

$$R\omega\,(L_1 + L_2) = \frac{R}{C\omega}$$

$$\omega = \frac{1}{\sqrt{C\,(L_1 + L_2)}} \tag{2}$$

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

Substituting Equation (2) in Equation (1), we get,

$$\beta(s) = \frac{1}{1 + \frac{L}{C} + \frac{C(L_1 + L_2)}{-L_1 L_2}}$$

$$\beta(s) = \frac{L_2}{L_1}$$

$$A = \frac{1}{\beta} = -\frac{L_1}{L_2}$$

3.4.4 Colpitt Oscillator

Colpitt oscillator has two blocks:

1. Amplifier.
2. Feedback network.

Amplifier It is a simple RC coupled amplifier. Design requirement and details are given in the previous experiments.

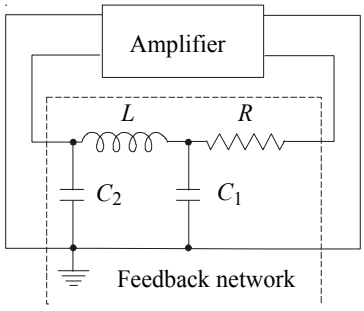


Fig. 3.54

Feedback Network Let us consider the feedback network,

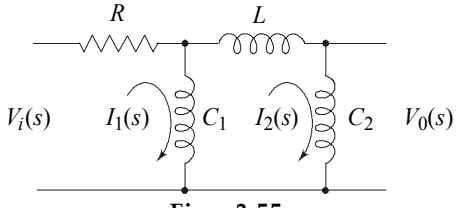


Fig. 3.55

$$RI = V$$

$$\begin{bmatrix} R + \frac{1}{Cs} & -\frac{1}{Cs} \\ -\frac{1}{C_1 s} & \left(\frac{1}{C_1 s} + \frac{1}{C_2 s} + Ls\right) \end{bmatrix} \begin{bmatrix} I_1(s) \\ I_2(s) \end{bmatrix} = \begin{bmatrix} V_i(s) \\ 0 \end{bmatrix}$$

$$\Delta = \left(R + \frac{1}{C_1 s}\right)\left(\frac{1}{C_1 s} + \frac{1}{C_2 s} + Ls\right) - \frac{1}{C_1^2 s^2}$$

$$\Delta I_2(s) = \begin{bmatrix} R + \frac{1}{Cs} & V_i(s) \\ -\frac{1}{C_1 s} & 0 \end{bmatrix}$$

$$\Delta I_2(s) = \frac{V_i(s)}{C_1 s}$$

$$I_2(s) = \frac{\Delta I_2(s)}{\Delta} = \frac{1}{R\left(\frac{1}{C_1 s} + \frac{1}{C_2 s} + Ls\right) + \frac{1}{C_1 C_2 s^2} + \frac{L}{C_1}}$$

$$V_0(s) = \frac{I_2(s)}{C_2 s}$$

$$\beta = \frac{V_0(s)}{V_i s} = \frac{1}{C_1 C_2 s^2 \left[\left(\frac{R}{C_1 s} + \frac{R}{C_2 s} + RLs\right) + \frac{1}{C_1 C_2 s^2} + \frac{L}{C_1}\right]}$$

$$\beta = \frac{1}{j\left(RC_2\omega + RC_1\omega - RC_1C_2L\omega^2\right) + 1 - LC_2\omega^2} \quad (1)$$

Equating imaginary part to zero, we get,

$$R\omega C_2 + RC_1\omega - RC_1C_2L\omega^2 = 0$$

$$\omega = \frac{1}{\sqrt{L}}\sqrt{\frac{C_1 + C_2}{C_1 C_2}} \quad (2)$$

$$f = \frac{1}{2\pi}\sqrt{\frac{C_1 + C_2}{LC_1C_2}}$$

Substituting Equation (2) in Equation (1), we get,

$$\beta(s) = \frac{1}{1 - LC_2\omega^2} = \frac{C_1}{C_2}$$

$$A = \frac{1}{\beta} = \frac{C_2}{C_1}$$

Experiment (Hartely and Colpitt Oscilltor)

Aim: ***To Design and Contruct the Given Oscillator at the Given Operting Frequency***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30)V	1
CRO	(0-20) MHz	1

Circuit Diagram:

Hartely Oscillator

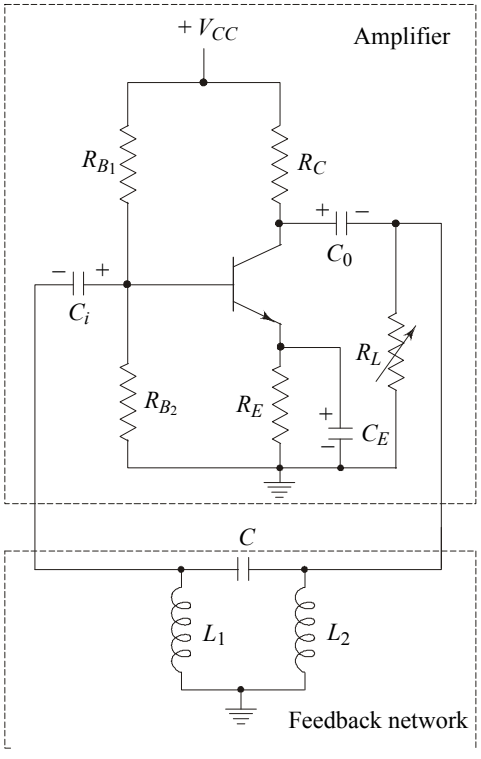


Fig. 3.56

Colpitt Oscillator

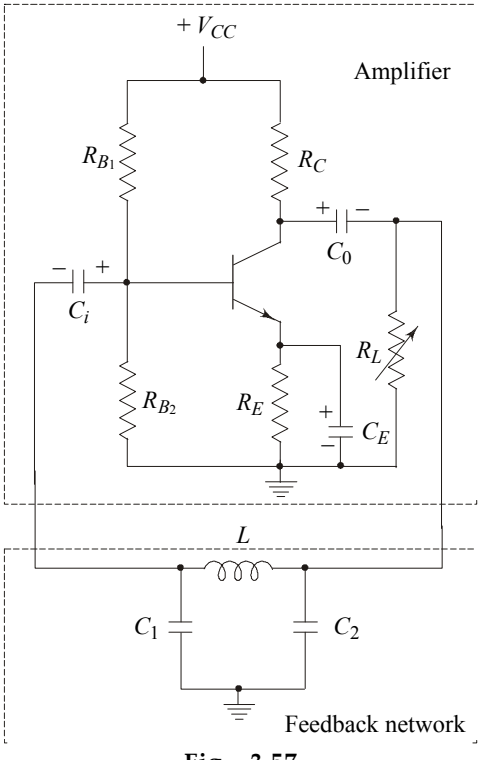


Fig. 3.57

Design of Feedback Network (Hartely Oscillator):

Given: $L_1 = 1$ mH; $f = 800$ kHz; $V_{CC} = 12$ V; $A_V = 50$; $f_L = 1$ kHz

$$A_V = \frac{1}{\beta} = \frac{-L_1}{L_2}$$

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

Find $C = ?$

Design of Feedback Network (Colpitt Oscillator):

Given: $C_1 = 0.1$ μF; $f = 800$ kHz; $V_{CC} = 12$ V; $A_V = 50$; $S = 10$; $I_E = 5$ mA; $f_i = 1$kHz

$$A_V = \frac{1}{\beta} = \frac{C_2}{C_1} \quad f_L = 1 \text{ kHz}$$

$$f = \frac{1}{2\pi}\sqrt{\frac{C_1 + C_2}{LC_1C_2}}$$

Find, $L = ?$

Amplifier Design (Common to Both Oscillators):

Gain formula is given by,

$$A_V = \frac{-h_{fe} R_{Leff}}{h_{ie}}$$

Assume, $V_{CE} = V_{CC}/2$ (transistor active)

Effective load resistance is given by, $R_{\text{leff}} = R_C \parallel R_L$

Emitter resistance is given by, $r_e = 26 \text{ mV}/ I_E$

$$h_{ie} = \beta r_e$$

where, r_e is internal resistance of the transistor.

$$h_{ie} = h_{fe}\, r_e$$

$$V_E = V_{CC}/10$$

On applying KVL to output loop, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

where, $V_E = I_E R_E$

Find $R_C = ?;\ R_L = ?$

Since I_B is very small when compare with I_C,

$$I_C \simeq I_E$$

$$R_E = V_E/I_E$$

$$V_B = V_{BE} + V_E$$

$$V_B = V_{CC} \frac{R_{B_2}}{R_{B_1} + R_{B_2}}$$

$$S = 1 + \frac{R_B}{R_E}$$

Find $R_B = ?$

$$R_B = R_{B_1} \parallel R_{B_2}$$

Find R_{B1} and R_{B2}

Coupling and by-pass capacitors can be thus found out.

Input impedence $Z_i = (h_{ie} \parallel R_B)$

Input coupling capacitor is given by, $X_{Ci} = \frac{Z_i}{10}$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

Output coupling capacitor is given by, $X_{C0} = (R_C \parallel R_L)/10$

$$X_{C0} = \frac{1}{2\pi f C_0}$$

Find $C_0 = ?$

By-pass capacitor is given by, $X_{CE} = R_E/10$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

Procedure:

1. Rig up the circuit as per the circuit diagrams (both oscillators).
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare it with its theoretical frequency.

Result:

	Theoretical		Practical	
	Hartely	Colpitt	Hartely	Colpitt
Frequency	$f_0 = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$	$f_0 = \frac{1}{2\pi}\sqrt{\frac{C_1 + C_2}{LC_1C_2}}$		

3.5 UJT RELAXATION OSCILLATOR

The negative resistance portion of the UJT characteristic is used in a relaxation oscillator.

Capacitor, C charges through resistor, R from V_{BB} until V_E reaches peak voltage V_P and the UJT turns on. Since UJT offers a low impedance path, capacitor, C discharges rapidly through R_1, giving a pulse of output voltage V_{B_1}. When V_E drops to about 2 V, the emitter ceases to conduct and the UJT switches off. Now as UJT offers high impedance to discharge, the capacitor again charges to peak until it turns on the UJT. This cycle repeats.

The frequency of oscillation depends upon the time constant RC and the UJT.

The period of oscillation is given by,

$$T = 1/f = RC \ln 1/(1-\eta)$$

η = intrinsic stand-off ratio.

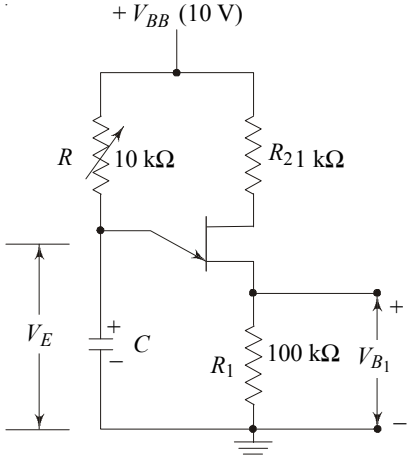


Fig. 3.58

The UJT may also be used in precision timing delay and current sensing circuit.

Experiment (Voltage Sweep Generator)

Aim: ***To Study the Operation of Voltage Sweep Generator and to Observe Output Waveform***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30)V	1
CRO	(0-20) MHz	1

Circuit Diagram:

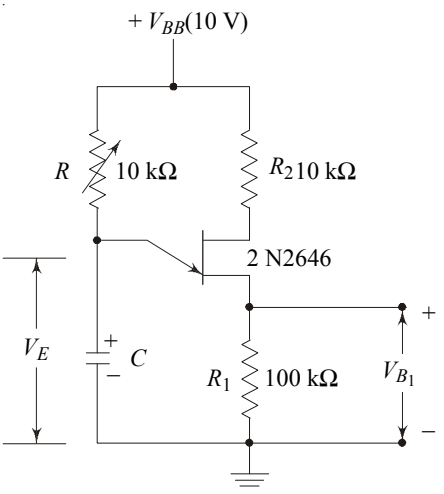


Fig. 3.59

Design:

Given: $V_V = 1.2$ V; $V_P = 5$ V; $V_{BB} = 12$ V; $T_{ON} = 0.5$ ms; $R_1 = 100\ \Omega$; $R_2 = 1$ kΩ

$$V_C(t) = V_f + (V_i + V_f)\, e^{-t/RC}$$

$$V_C(t) = V_P$$

$$V_f = V_{BB}$$

$$V_i = V_V$$

Find, $RC = ?$

Assume, $C = 0.01$ μF, find $R = ?$

Model Graph:

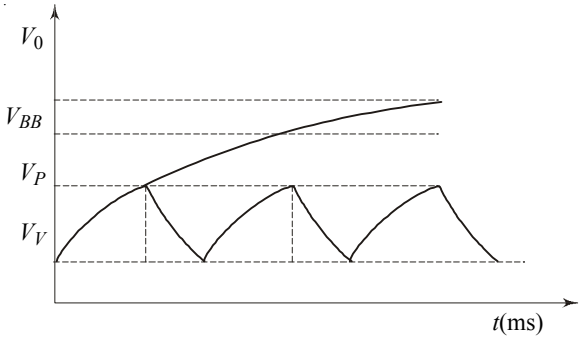


Fig. 3.60

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare it with its theoretical frequency.

Result:

	Theoretical	Practical
Frequency		

3.6 RF AMPLIFIER

Experiment

Aim: ***Design a RF Amplifier with Tuned Circuit to Resonate at 800 kHz and Bandwidth 20 kHz***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

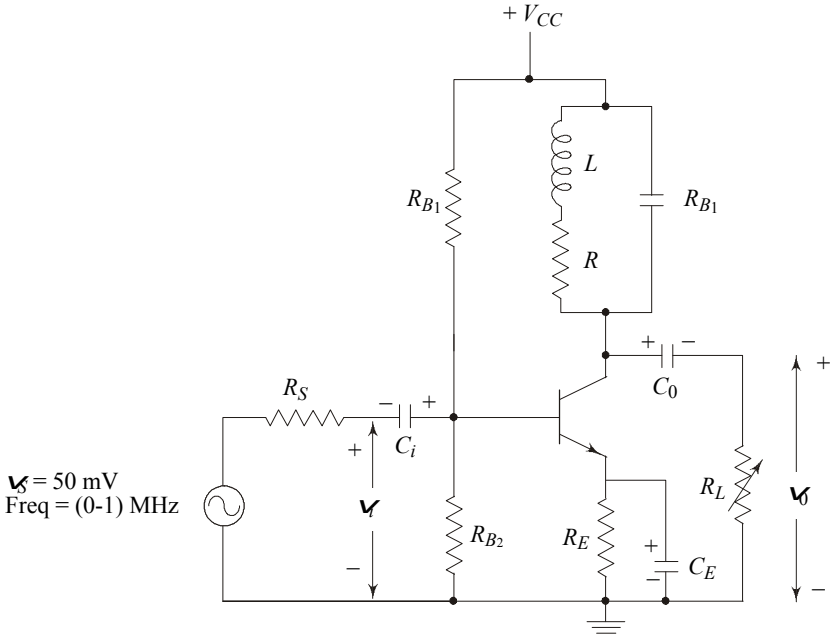


Fig. 3.61

Design:

Given data: V_{CC} = 15 V; I_C = 1 mA; A_V = 50; f_0 = 800 kHz; Stability factor = [2-10]; BW = 20 kHz; R_S = 680 Ω

Assume, $V_{CE} = V_{CC}/2$ (transistor active)

Emitter resistance is given by, $r_e = 26 \text{ mV}/I_E$

$$h_{ie} = \beta r_e$$

where, r_e is internal resistance of the transistor.

$$h_{ie} = h_{fe}\, r_e$$

$$V_{CC} = I_C R + V_{CE} + V_E$$

Find $V_E = ?$

(R value is given in the tuned circuit design)

where, $V_E = I_E R_E$

Find $R_E = ?$

Since I_B is very small when compare with I_C,

$$I_C \simeq I_E$$

$$V_B = V_{BE} + V_E$$

$$V_B = V_{CC} \frac{R_{B_2}}{R_{B_1} + R_{B_2}}$$

$$S = 1 + \frac{R_B}{R_E}$$

Find $R_B = ?$

$$R_B = R_{B_1} \parallel R_{B_2}$$

Find R_{B_1} and R_{B_2}

Coupling and by-pass capacitors can be thus found out.

Input coupling capacitor is given by, $X_{Ci} = \{[h_{ie} + (1 + h_{fe})R_E] \parallel R_B\}/10$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

Output coupling capacitor is given by, $X_{C_0} = (R_C \parallel R_L)/10$

$$X_{C_0} = \frac{1}{2\pi f C_0}$$

Find $C_0 = ?$

By-pass capacitor is given by, $X_{CE} = R_E/10$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

For a tuned circuit,

$$f_2 - f_1 = \text{bandwidth} = \frac{1}{2\pi} \frac{R}{L}$$

Assume, $L = 1$ mH; BW = 20 kHz

Then, find $R = ?$

$$\omega_0^2 = \frac{1}{LC} - \frac{R^2}{L^2}$$

Since, $\omega_0 = 2\pi f_0$, find $C = ?$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set e_s = 50 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.

Tabular Column:

e_s = 50 mV

Frequency	e_0 (volts)	Gain = e_0/e_s	Gain (dB) = 20 log (e_0/e_s)

Model Graph: (Frequency Response)

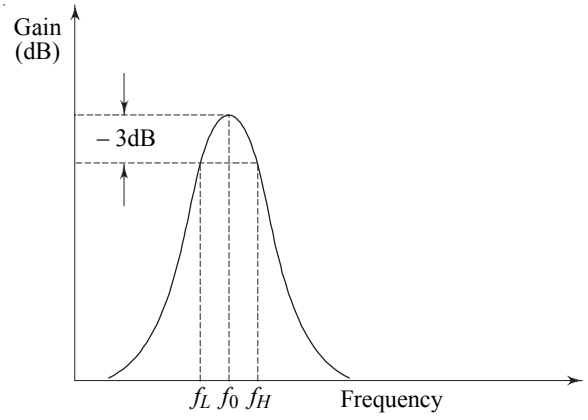


Fig. 3.62

Result:

	Theoretical	Practical
Input impedance	$Z_i = R_{BB} \mid\mid h_{ie}$	
Output impedance	$Z_0 = R_L$	
Gain (Midband)		
Band width		

3.7 SINGLE TUNED AMPLIFIER

Experiment:

Aim: ***To Design and Construct a Single Tuned Amplifier***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-30) V	1
CRO	(0-20) MHz	1
Function generator	(0-1) MHz	1

Circuit Diagram:

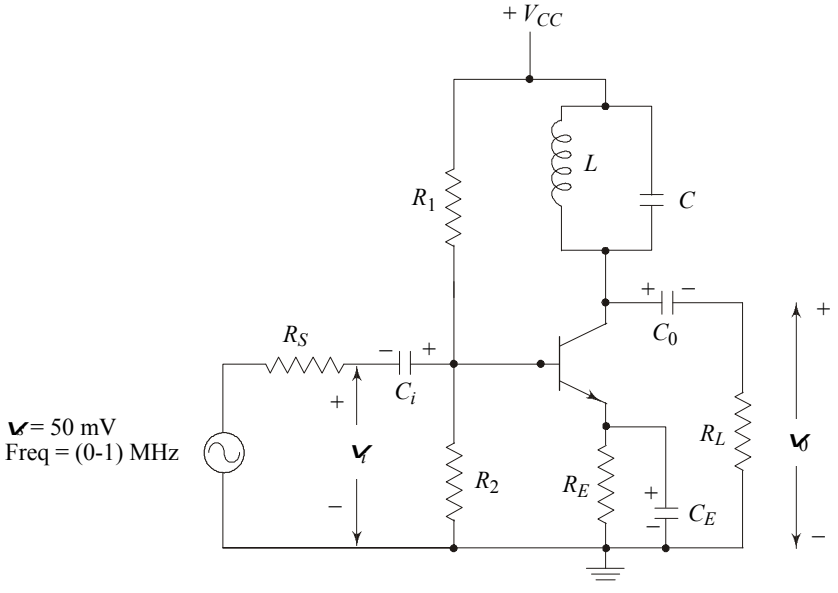


Fig. 3.63

Design:

Given $Q = 15;\ L = 1$ mH; $V_{CC} = 12$ V; $I_{CQ} = 1$ mA

Assume $V_{CEQ} = V_{CC}/2;\ V_{EQ} = V_{CC}/2$

$Q = R_L / \omega L$

Therefore, $R_L = ?$

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

Find $C = ?$

Assume $S = 5$

$V_E = I_E R_E$ ($I_{EQ} \simeq I_{CQ}$)

Therefore, $R_E = ?$

Assume $S = 5;$

$$S = 1 + \frac{R_B}{R_E}$$

Find $R_B = ?$

$V_B = V_E + V_{BE} = ?$

$R_B = R_1 \| R_2$

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2}$$

$Z_i = (R_B \| h_{ie})$

Solve for R_1 and R_2.

Input coupling capacitor is given by, $X_{Ci} = \frac{Z_i}{10}$

$$X_{Ci} = \frac{1}{2\pi f C_i}$$

Find $C_i = ?$

Output coupling capacitor is given by, $X_{C_0} = (R_C \| R_L)/10$

$$X_{C_0} = \frac{1}{2\pi f C_0}$$

Find $C_0 = ?$

By-pass capacitor is given by, $X_{CE} = R_E/10$

$$X_{CE} = \frac{1}{2\pi f C_E}$$

Find $C_E = ?$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set v_s = 50 mV (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph: gain (dB) vs frequency.
5. Find the input and output impedances.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.

Tabular Column:

v_s = 50 mV

Frequency	v_0 (volts)	Gain = v_0/v_s	Gain (dB) = 20 log (v_0/v_s)

Model Graph: (Frequency Response)

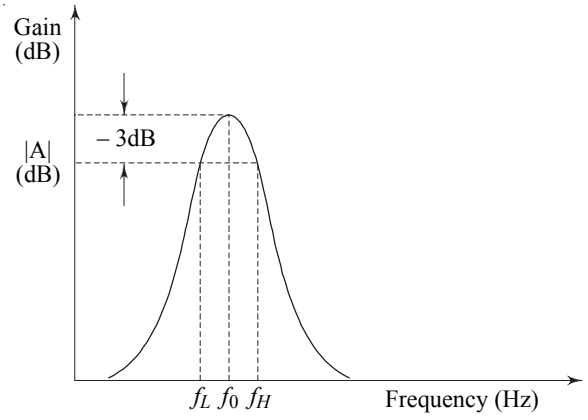


Fig. 3.64

Result:

	Theoretical	Practical
Input impedance		
Output impedance		
Gain (Midband)		
Band width		

Experiment Bi-stable Multivibrator

Aim: ***To design a bi-stable multivibrator and study the output waveform.***

Equipment Required:

Equipment	Range	Quantity
Dual power supply	(12-0-12) V	1
CRO	(0-20) MHz	1

Circuit Diagram:

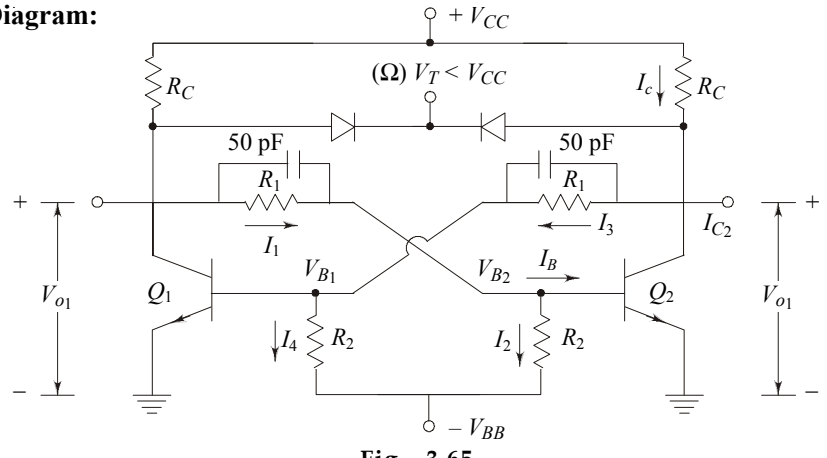


Fig. 3.65

Design

Given $V_{CC} = 12\text{V}$; $V_{BB} = -12$ V; $I_C = 2$ mA; $V_{C(\text{sat})} = 0.2$ V
$V_{BE(\text{sat})} = 0.7$ V

Assume Q_1 is cut-off, i.e. $V_{C1} = V_{CC}$ (+ 12 V)
Q_2 is in saturation (ON), i.e. $V_{C2} = V_{C(\text{sat})}$ (0.2 V)

Using superposition principle,

$$V_{B1} = V_{BB}\left(\frac{R_1}{R_1 + R_2}\right) + V_{C2}\left(\frac{R_2}{R_1 + R_2}\right) << 0.7$$

Let us consider $V_{B1} = -1$ V

Then
$$-1 = \frac{-12R_1}{R_1 + R_2} + \frac{0.2R_2}{R_1 + R_2}$$

Assume, $R_1 = 10$ kΩ such that it ensures a loop gain in excess of unity during the transition between states. The inequality

$$R_1 < h_{fe}\, R_c$$

$R_2 = 91.67$ kΩ

Test for conditions: Q_1 = cut-off ($V_{C1} = 12$ V)
Q_2 = saturation/(ON) ($V_{C2} = 0.2$ V)

Minimum base current, $I_{B(\text{min})}$ must be less than the base current (I_B) i.e.,

$$I_{B(\text{min})} < I_B$$

Calculate h_{fe} from multimeter (say = 200)

$$I_{B2(\text{min})} = \frac{I_{C2}}{h_{fe}} \qquad I_C = \frac{V_{CC} - V_{C2}}{R_C}$$

$$I_{C2} = I_C - I_3 \qquad R_C = \frac{V_{CC} - V_{C2}}{I_C} = \frac{12 - 0.2}{2 \times 10^{-3}} = 5.9\ \text{k}\Omega$$

$$I_{C2} = (2 - 0.12)\ \text{mA} = 1.88\ \text{mA} \qquad I_3 = \frac{V_{C2} - V_{BB}}{R_1 + R_2} = \frac{0.2 + 12}{(10 + 91.6)\text{k}} = 0.12\ \text{mA}$$

$$I_{B2(\text{min})} = \frac{1.88 \times 10^{-3}}{200} = 9.4\ \mu\text{A} \qquad I_1 = \frac{V_{C1} - V_{BE}}{R_C + R_1} = \frac{12 - 0.7}{(5.9 + 10)\text{k}} = 0.71\ \text{mA}$$

$$I_{B2} = I_1 - I_2$$

$$I_{B2} = (0.71 - 0.14)\ \text{mA} = 0.57\ \text{mA} \qquad I_2 = \frac{V_{BE} - V_{BB}}{R_2} = \frac{0.7 + 12}{91.6\ \text{k}} = 0.14\ \text{mA}$$

Since $I_{B2} > I_{B2(\text{min})}$, Q_2 is ON
$C_1 = 25$pF (Commutative capacitor)

Procedure

1. Connect the circuit as per circuit diagram.
2. Switch on the regulated power supply and observe the output wave form at the collector of Q_1 and Q_2.
3. Sketch the waveform.
4. Apply a threshold voltage V_T (pulse voltage) and observe the change of states of Q_1 and Q_2.
5. Sketch the waveform.

Experiment Monostable Multivibrator

Aim: ***To design a monostable multivibrator and study the output waveform.***

Equipment Required:

Equipment	Range	Quantity
CRO	0-20 MHz	1
Power Supply	(0-30) V	2

Circuit Design:

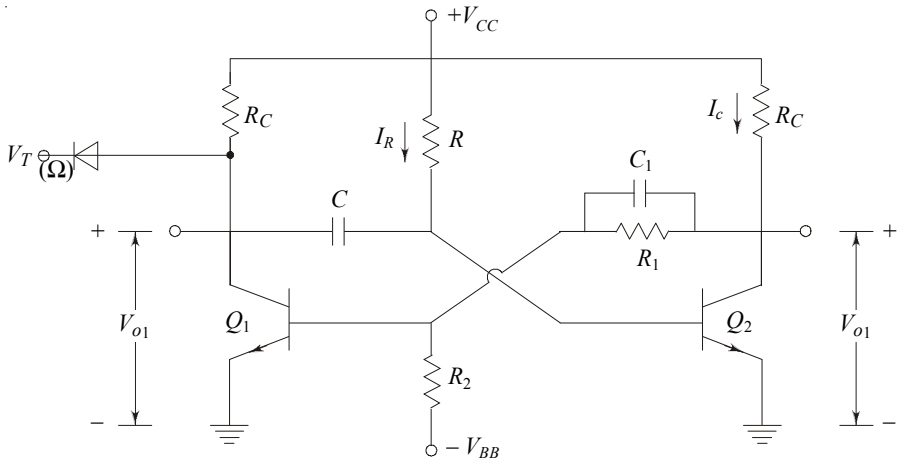


Fig. 3.66

Design

Given V_{CC} = + 12 V; V_{BB} = – 2 V; I_C = 2 mA; $V_{CE(\text{sat})}$ = 0.2 V; h_{FE} = 200; f = 1 kHz

$$R_C = \frac{V_{CC} - V_{CE(\text{sat})}}{I_C} \qquad \text{(assuming } Q_2 \text{ is in saturation)}$$

$$R_C = \frac{12 - 0.2}{2 \times 10^{-3}} = 5.9 \text{ k}\Omega$$

$$I_{B2(\text{min})} = \frac{I_{C2}}{h_{FE}} = \frac{2 \times 10^{-3}}{200} = 10 \text{ } \mu\text{A}$$

Select $I_{B2} > I_{B2(\min)}$ (say 25 μA)

$$\text{then } R = \frac{V_{CC} - V_{BE(\text{sat})}}{I_{B2}} = \frac{12 - 07}{25 \times 10^{-6}} = 452 \text{ k}\Omega$$

$$T = 0.69\ RC \left(T = \frac{1}{f} \right)$$

$$1 \times 10^{-3} = 0.69 \times 452 \times 10^{+3}\ C$$

$$C = 3.2 \text{ nF}$$

$$V_{B1} = \frac{V_{BB} R_1}{R_1 + R_2} + \frac{V_{CE(\text{sat})} R_2}{R_1 + R_2}$$

Since Q_1 is off state, $V_{B1} \leq 0$.

Then $$\frac{V_{BB} R_1}{R_1 + R_2} = \frac{V_{CE(\text{sat})} R_2}{R_1 + R_2}$$

$$V_{BB}\ R_1 = V_{CE(\text{sat})}\ R_2$$

$$+ 2R_1 = 0.2R_2$$

$$R_2 = \frac{+ 2R_1}{0.2}$$

Assume $R_1 = 10$ kΩ. Then $R_2 = 100$ kΩ

$C_1 = 25$ pF (commutative capacitor)

Procedure

1. Connect the circuit as per the circuit diagram.
2. Switch on the power supply.
3. Observe the waveform at collectors of Q_1 and Q_2 and plot it.
4. Trigger the monostable multivibrator with a pulse and observe the change in waveform.
5. Plot the waveform and observe the changes before and after triggering the input to the circuit.

Experiment Astable Multivibrator

Aim: ***To design a astable multivibrator and study the output waveform.***

Equipment Required:

Equipment	Range	Quantity
CRO	0-20 MHz	1
Power supply	(0-30) V	1

Circuit Diagram:

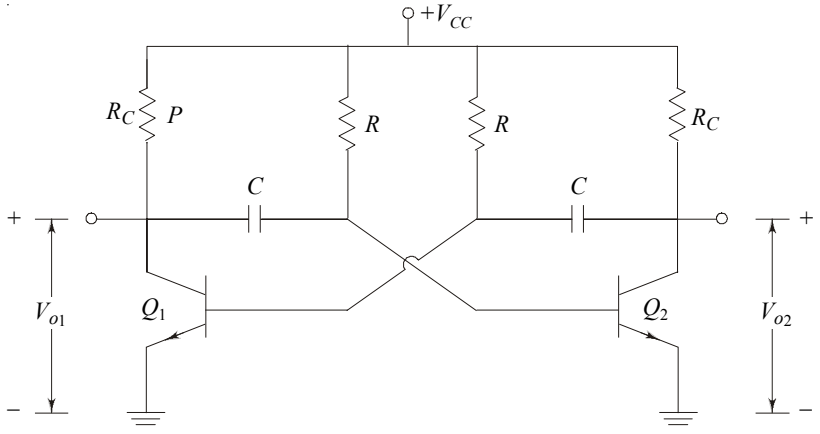


Fig. 3.67

Design

$$V_{CC} = +\ 10\ \text{V};\ h_{fe} = 200;\ f = 1\ \text{kHz};\ I_C = 2\ \text{mA}$$

$$R \le h_{fe}\ R_C$$

$$R_C = \frac{V_{CC} - V_{C2(\text{sat})}}{I_C} = \frac{10 - 0.2}{2 \times 10^{-3}} = 4.9\ \text{k}\Omega$$

$$R \le 200 \times 4.9 \times 10^3 = 980\ \text{k}\Omega$$

$$T = 1.38\ RC$$

$$1 \times 10^{-3} = 1.38 \times 980 \times 10^3 \times C$$

$$C = 0.74\ \text{nF}$$

Procedure

1. Connect the circuit as per the circuit diagram.
2. Switch on the power supply.
3. Observe the waveform both at bases and collectors of Q_1 and Q_2.
4. Plot the waveform.

Schmitt Trigger

Aim: ***To design and test the Schmitt trigger for the given LTP and UTP***

Instrument required:

Name of the component	Range	Quantity
Signal Generator	0-1 MHz	1
CRO	0-20 MHz	1
Power supply	0-30 V	1

Circuit diagram:

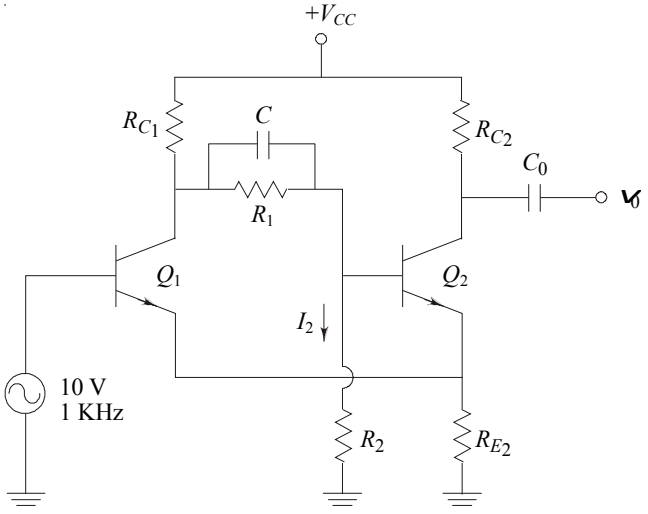


Fig. 3.68

Given: $V_{CC} = 10$ V; $h_{fe} = 200$; $I_C = 5$ mA; UTP = 5 V; LTP = 1 V

$$V_{B2} = V_{BE} + V_E$$

At UTP, $V_{B2} = 5$

Therefore, $V_{E2} = V_{B2} - V_{BE} = ?$

$$R_{E2} = \frac{V_{E2}}{I_{E2}} = ?$$

Assume Q_1 is OFF and Q_2 is in saturation,

$$V_{CE\ (sat)} = 0.2 \text{ V}$$

$$V_{CC} = I_{C2} R_{C2} + V_{CE2} + V_{E2}$$

$$R_{C2} = ?$$

Assume $$I_2 = \frac{I_E}{10} = ?$$

$$R_2 = \frac{V_{B2}}{I_2} = ?$$

$$I_{B2} = I_{C2}/h_{fe}$$

$$R_{C1} + R_1 = \frac{V_{CC} + V_{B2}}{I_2 + I_{B2}} = ?$$

Now assume, Q_1 is in saturation, and Q_2 is OFF

$$V_{B2} = \text{LTP} = 1 \text{ V}$$

$$I_1 = \frac{V_{B2}}{R_2}$$

$$I_{C1} = I_{E2}$$

$$V_{CC} = R_{C1}\,(I_{C1} + I_1) + I_1R_1 + I_1R_2$$

$$R_{C1} = ?$$

$$R_1 = ?$$

$$R = R_1 \parallel (R_1 + R_{C1})$$

Triggering time, $t_{trig} = \dfrac{1}{t_{trig}}$

$$t_{trig} = 2.3\ RC$$

$$C = ?$$

Procedure:

1. Connect the circuit diagram as per diagram.
2. Apply input sinusoidal input (10 V; 1 KHz).
3. Connect the output of the circuit to channel-1 and input signal to channel-2 of CRO.
4. Identity the cross-over point of square-wave with respect to input signal, which gives the value of UTP and LTP. Positive wave cross-over point define UTP and negative wave cross-over point define LTP.
5. Plot both input and output in a same graph.

Result

Frequency	Theoretical	Practical
UTP	5 V	
LTP	1 V	

OBJECTIVE QUESTIONS

1. Define amplification.
2. What is biasing? Why it is necessary?
3. Mention the different types of biasing.
4. Mention the applications of CE amplifier. Justify.
5. Mention the applications of CC amplifier. Justify.
6. Mention the applications of CB amplifier. Justify.
7. Compare the characteristics of CE-amplifier, CC-amplifier, and CB-amplifier.
8. What is a driver circuit?
9. What are the major applications of a power amplifier?
10. What is single tuned amplifier?
11. What are the physical applications of a feedback amplifier?
12. Universal biasing technique is preferred over any other biasing technique. Why?
13. Why is negative feedback used in RC-coupled amplifier?
14. What type of feedback is preferred in oscillators?
15. How does oscillation start in oscillators?
16. Define over-damping and under-damping conditions.

17. List out the applications of oscillators.
18. Which oscillator is very suitable for audio range applications?
19. Which oscillator is suitable for RF range applications?
20. Which oscillator is suitable for low frequency applications?
21. What is RF amplifier? How is it different from RC-coupled amplifier?
22. What are the advantages of FET amplifier over conventional transistor amplifier?
23. Define push-pull concept.
24. What are the advantages of push-pull amplifier? How?
25. Define class-S and class-D power amplifier.
26. Power amplifiers are used at the last stage of the module. Give reason.
27. What are the uses of biasing resistance?
28. What must be the voltage across the transistor, when it is operated as an amplifier?
29. What must be the voltage across the transistor, when it is operated as a switch?
30. How do you eliminate the non-linearity in the RC-coupled amplifier?
31. What are the factors, which influence the higher cut-off frequency?
32. What the components, which influence the lower cut-off frequency?
33. How do you test the transistor for active region condition?
34. How do you test the transistor for switching condition?
35. What are the applications of saw-tooth waveform, which is generated by UJT?
36. Cascade CE-amplifier with CC-amplifier, and study the characteristic behaviours.
37. What are parameters affected when two different amplifiers are cascaded?
38. Study the characteristics of different feedback amplifier.
39. What is the main advantage of differential concept over coventinal amplifier concept?

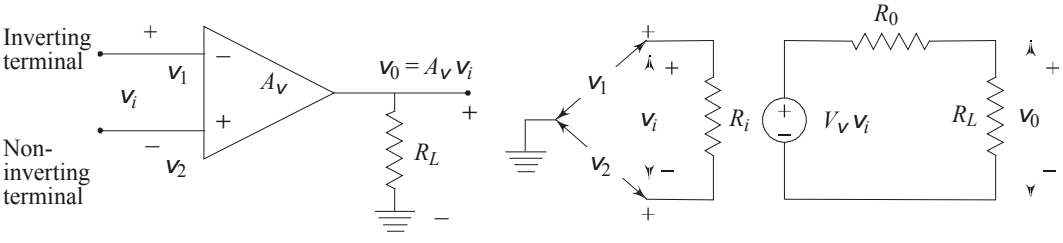
4 INTEGRATED CIRCUITS

4.1 OPERATIONAL AMPLIFIER

The operation amplifier is a direct-coupled high gain amplifier to which feedback is added to control its overall response characteristics. It is often referred to as the basic linear integrated circuit.

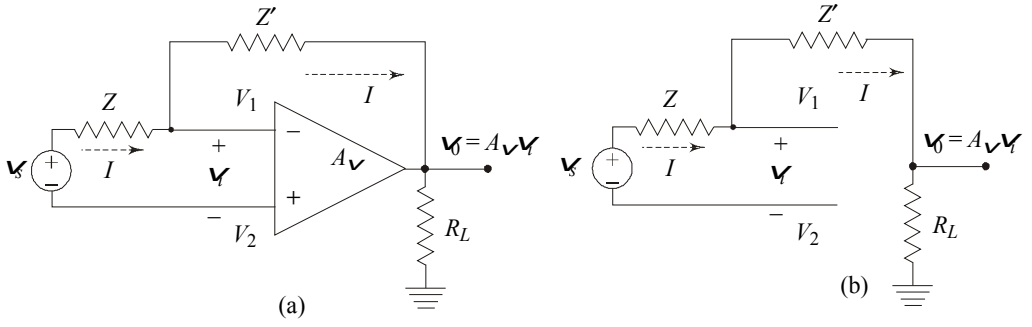
4.2 OP-AMP CHARACTERISTICS

Properties	Ideal	Typical
Open loop gain	∞	Very high ($\geq 10^4$)
Open loop bandwidth	∞	Very high
Common-mode rejection ratio	∞	High (≥ 70 dB)
Input resistance	∞	High (≥ 10 MΩ)
Output resistance	0	Low (< 500 Ω)
Off-set voltage and current	0	Low(< 10 mV, < 0.2 nA)



(a) **Fig. 4.1** (b)

Figure (4.1a) shows the ideal op-amp with feedback impedance Z and Z' and the positive terminal grounded.



(a) (b)

Fig. 4.2

Let us find an expression for voltage gain with feedback. Since input impedance, $Z_i = \infty$, the current I through Z also passes through Z', as indicated in Fig. 4.2(a). We also note that $v_i = v_0 / A_v = 0$ as $A_v \Rightarrow \infty$.

The voltage gain, $$A_v = \frac{V_0}{V_s} = \frac{IZ'}{IZ} = \frac{Z'}{Z}$$

At the input of the amplifier, there exists a virtual ground or short circuit. The term *virtual ground* is used to imply that although the feedback from the output to the input through Z' serves to keep the voltage, v_i, zero, no current actually flows into the short. This situation is shown with a heavy double-ended arrow as in Fig. (4.2b).

Block Diagram: Typical op-amp

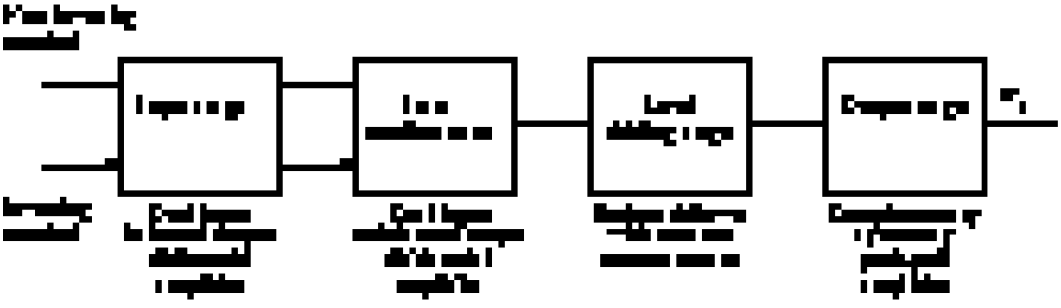


Fig. 4.3

Since the op-amp is a multistage amplifier, it can be represented by a block diagram as shown in Fig. 4.3. The input stage is a dual input balanced output differential amplifier. This stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the op-amp. The intermediate stage is usually another differential amplifier, which is driven by the output of the first stage. In most amplifiers, the intermediate stage is dual input unbalanced output (single ended). Because, direct coupling is used, the DC voltage at the output of intermediate stage is well above the ground potential. Therefore, generally the level shifting circuit is used after the intermediate stage, to shift the DC level at the output of the intermediate stage downwards to zero volts, with respect to the ground. The final stage is usually a push-pull complementary amplifier output stage. The output stage increases the output voltage swing and rises the current supplying capability of the op-amp. A well-designed output stage also provides low output resistance.

Some Definitions

Input Offset Voltage It is defined as the voltage that has to be applied between the op-amp input terminals to obtain a zero voltage.

Slew Rate It is defined as the maximum rate of change of the output voltage with a large amplitude step voltage applied at the input.

Common Mode Rejection Ratio This is a measure of the ability of an op-amp to reject signals that are simultaneously present at both inputs.

$$\text{CMMR} = \frac{\text{Differential mode gain } (A_d)}{\text{Common mode gain } (A_c)}$$

Bandwidth It is defined as the maximum frequency at which a full sized undistorted sinewave can be obtained at the op-amp output.

Input Bias Current Input bias current (I_{iB}) is the average of the currents that flow into the inverting and non-inverting input terminals of the op-amp.

$$I_{iB} = \frac{I_{\text{INV}} + I_{\text{NON - INV}}}{2}$$

An op-amp is a high gain differential amplifier having the following characteristics:

1. Voltage gain is infinity.
2. Input impedance is infinity.
3. Output impedance is zero.
4. Bandwidth is infinity.
5. CMRR is infinity.
6. PSRR is zero.
7. Offset voltage and current are zero.
8. Drift in characteristics due to temperature is zero.

An op-amp has 2 inputs, one inverting and the other non-inverting. It exhibits perfect balance when the voltages at both input terminals are equal. As it performs mathematical functions like addition, subtraction, integration and differentiation, the amplifier is called an *Operational Amplifier*. Due to its above characteristics, it finds application in many fields like medicine, communication, industries, etc.

Experiment (Characteristics of op-amp)

Aim: ***To Determine the Following Characteristics of an op-amp***

1. Input off-set voltage
2. Slew rate
3. Common mode rejection mode
4. Band width
5. Input bias current

Equipments Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1
Regulated power supply	(0-30) V	1
Dual power supply	(12-0-12) V	1

Procedure:

Input off-set voltage:

1. Connections are made as per the circuit diagram.
2. Switch on the dual power supply and note down the output voltage from the CRO.
3. Calculate the input offset voltage from the given formula,

$$V = V_0 \left(\frac{R_1}{R_2 + R_1} \right)$$

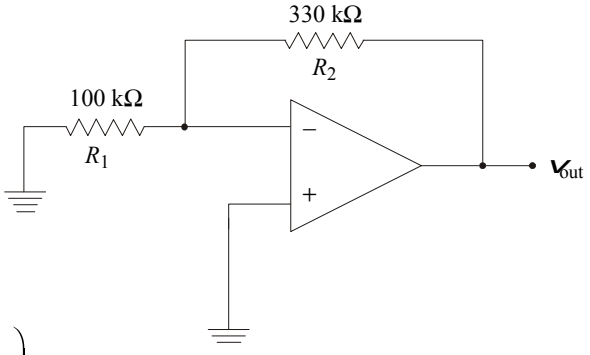


Fig. 4.4

Slew rate:

1. Connections are made as per the circuit diagram.
2. Give a sinusoidal input of 1 V_{pp}; 1 kHz.
3. Switch on the dual power supply.
4. Vary the input frequency and observe the output.
5. Note down the value of the input frequency at which the output gets distorted.
6. Determine the slew rate from the given formula,

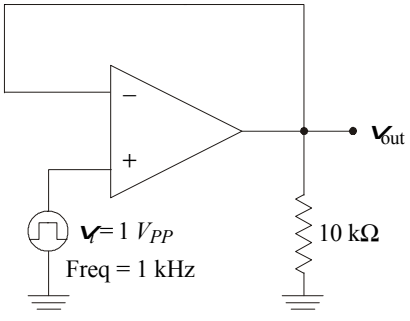


Fig. 4.5

$$\text{Slew rate: } \frac{2\pi f V_m}{10^{-6}} V/\mu s$$

7. Repeat the above procedure by giving square wave input.
8. Increase the frequency till the output becomes a triangular wave.
9. Find the slew rate from the given formula,

$$\text{SR: } \frac{\Delta V_0}{\Delta t}$$

Common mode rejection ratio:

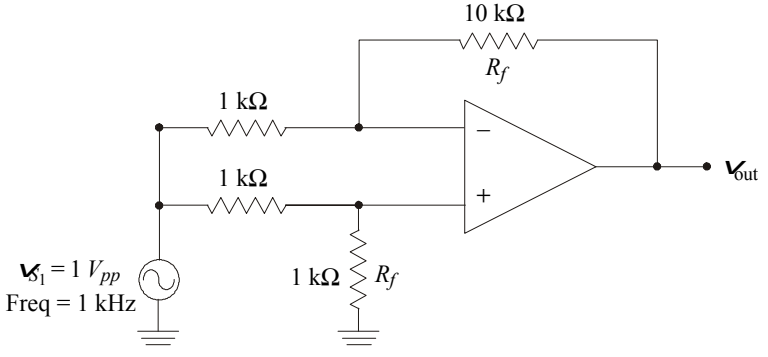


Fig. 4.6

1. Connections are made as per the circuit diagram.
2. Give a sinusoidal input of 1 V_{pp} 1 kHz.
3. Switch on the dual power supply.
4. Note down the output voltage from the CRO.
5. Determine the CMRR by the following procedure.

$$\text{Common Mode Gain} = A_C = \frac{V_0}{V_i}$$

$$\text{Differential Mode Gain} = A_d = \frac{R_2}{R_1}$$

$$\text{CMRR} = 20 \log \left(\frac{A_d}{A_c} \right)$$

Band width:

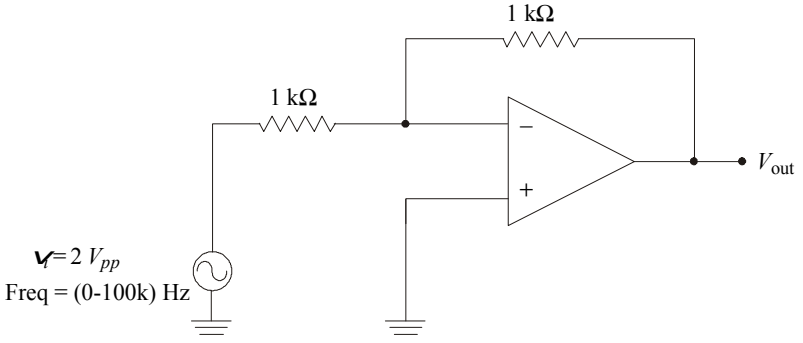


Fig. 4.7

1. Connections are made as per the circuit diagram.
2. Give a sinusoidal input of 2 V_{pp}.
3. Switch on the dual power supply.
4. Increase the frequency until the output voltage reduces to 0.7 times the input voltage.
5. Note down the frequency at this point and this gives the bandwidth of the op-amp at unity gain.

Input bias current:

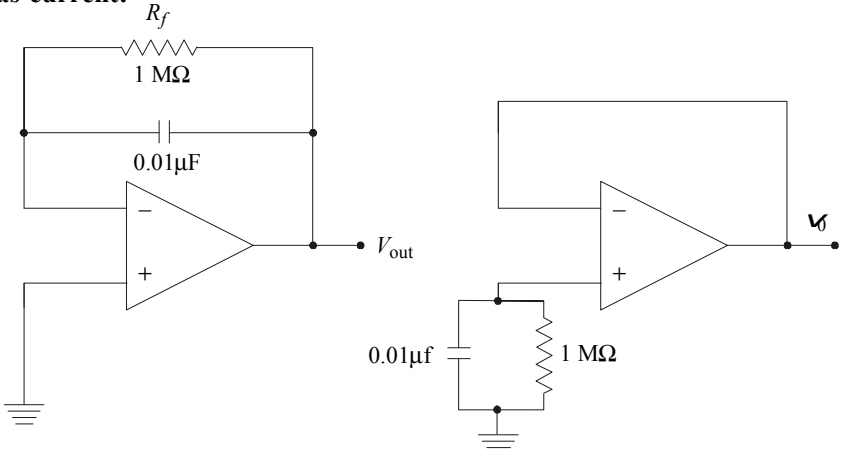


Fig. 4.8

1. Connections are made as per the circuit diagram.
2. Switch on the dual power supply.
3. Note down the output voltage from the CRO.
4. Calculate the input bias current in the inverting mode from the following formula,

$$I_0^- = \frac{V_0}{R}$$

5. Repeat the above procedure in the non-inverting mode and calculate the current from the following formula,

$$I_0^+ = -\frac{V_0}{R}$$

Result:

The characteristics of the op-amp were studied and the results are tabulated below.

Parameters Readings	
Input off-set voltage	
slew rate	
CMRR	
Bandwidth	
Input bias current – Inverting	
– Non-inverting	

Exercises:

1. Discuss any two methods of measuring the input offset voltage.
2. How is frequency compensation done in an op-amp?
3. Define CMRR, PSRR and the maximum output voltage swing of an op-amp.

Op-Amp Applications:

1. Signal Conditioners
   (a) Linear, e.g., adder, subtractor, differentiator, integrator, *V–I* converter, etc.
   (b) Non-linear, e.g., log amp, anti-log amp, multiplier, divider, etc.
2. Singal Processors
   (a) Linear, e.g., voltage follower, Instrumentation amplifier, etc.
   (b) Non-linear, e.g., comparator, peak detector, sample and hold circuit, etc.

Basic Rules:

Rule 1 The input terminals of op-amp draw no current because of the large differential input impedance of the op-amp.

Rule 2 The potential difference across the input terminals of an op-amp is zero because of the large open loop gain of the op-amp.

4.3 OP-AMP LINEAR APPLICATIONS

4.3.1 Inverting Amplifier

It is a closed loop mode application of op-amp and employs negative feedback. R_f and R_1 are feedback and input resistance of the circuit respectively.

The input terminals of op-amp draw no current because of the large differential input impedance. The potential difference across the input terminals of an op-amp is zero because of the large open loop gain of the op-amp. Due to these two conditions, no current enters op-amp circuit and the inverting terminal is at ground potential. The inverting terminal is now called *virtual ground*.

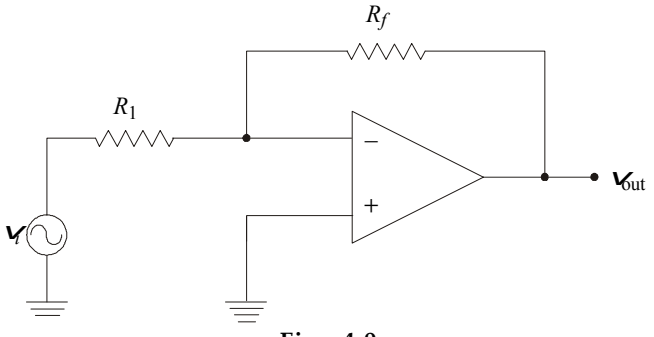


Fig. 4.9

By adding KCL to virtual ground we get,

$$I_i = I_f$$

$$\frac{(V_i - V_N)}{R_1} = \frac{(V_N - V_0)}{R_f}$$

V_N = virtual potential = 0 V.

Therefore, $$\frac{V_0}{V_i} = -\frac{R_F}{R_1} = A_v$$

Thus, the closed loop voltage gain A_v of the inverting amplifier is independent of the large open loop gain of the op-amp.

Disadvatanges of Inverting Amplifier

1. There exists a phase (180°) between input signal and output signal.
2. The input impedance, Z_i of the inverting amplifier is R_1. Thus input impedance is limited to a very low practical value. Hence the current requirement of the circuit is high. The circuit may load the source, V_i.
3. Smaller bandwidth when compared with non-inverting amplifier.

4.3.2 Auxillary Circuit using Inverting Amplifier

Sign Changer

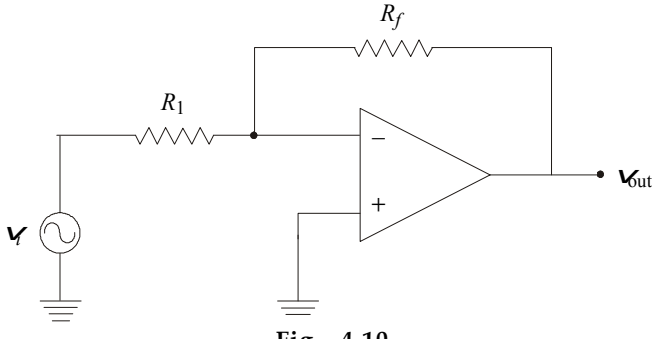


Fig. 4.10

If $R_f = R_1$, then $V_0 = - V_i$

A sign changer is a purely resistive network. It is an inverting amplifier with unity gain.

Scale Changer

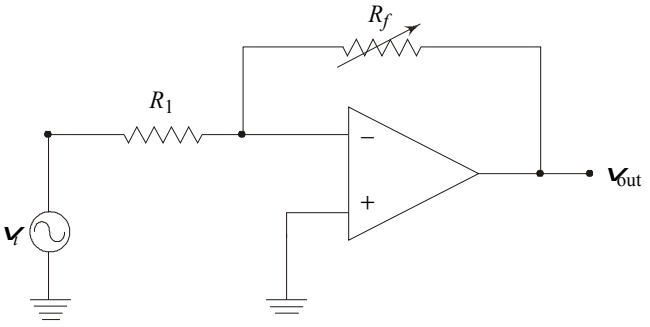


Fig. 4.11

A scale changer is a purely resistive network and it is an inverting amplifier with a gain other than unity.

Phase Shifter A phase shifter is an impedance (resistance + reactance) network and it introduces a phase angle of $(\theta - \phi)$ into the input signal V_i.

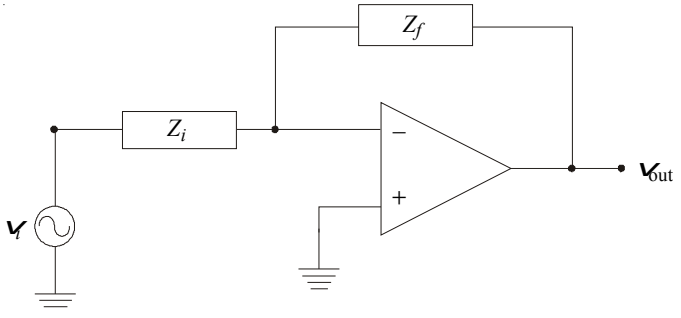


Fig. 4.12

$$\frac{V_0}{V_i} = \frac{- Z_f \angle \phi}{Z_i \angle \theta}$$

If, $|Z_f| = |Z_i|$, then

$$V_0 = - [\angle \phi - \theta] V_i$$

Adder

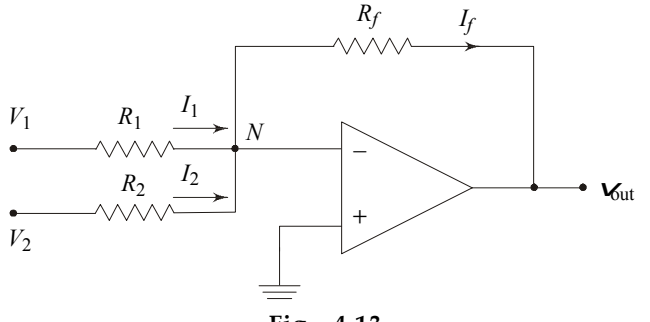


Fig. 4.13

Apply KCL to the node N, we get

$$I_1 + I_2 = I_f = \frac{(V_1 - V_N)}{R_1} + \frac{(V_2 - V_N)}{R_2} + \cdots\cdots = \frac{(V_N - V_0)}{R_f}$$

Virtual ground voltage, $V_N = 0$. Therefore,

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \cdots\cdots = -\frac{V_0}{R_f}$$

$$If,\ R_1 + R_2 + \cdots\cdots = R_f\ ,\ \text{then}$$

$$V_0 = -[V_1 + V_2 + \cdots\cdots + V_N]$$

Hence the addition operation.

Averagers For the adder circuit, if we make following assumption, we get averager, i.e.,

If, $R_1 = R_2 = 2R_f$, then

$$V_0 = -\frac{(V_1 + V_2)}{2}$$

For n inputs $R_1 = R_2 = \cdots = nR_f$, then

$$V_0 = -\frac{(V_1 + V_2 + V_3 + \cdots\cdots + V_N)}{N}$$

4.3.3 Non-Inverting Amplifier

It is a linear closed loop mode application of op-amp. There will be no phase shift between the output and input. Hence the name, *non-inverting amplifier.*

Advantages of a Non-Inverting Amplifier

1. There is no phase shift between output and input.
2. The input impedance of the non-inverting amplifier is approximately equal to $R_i + R_f \simeq R_i$, where R_i is the large differential input impedance of the op-amp and its value is ideally infinity. Therefore, the non-inverting amplifier will not load any source connected to it.
3. Larger bandwidth when compared with the inverting amplifier.
4. Circuit employs negative feedback.

Applying KCL at node N, we get

$$I_1 + I_f = 0$$

$$\frac{V_i}{R_1} + \frac{V_i - V_0}{R_f} = 0$$

$$\frac{V_i}{R_1} + \frac{V_i}{R_f} = \frac{V_0}{R_f}$$

On simplifying we get,

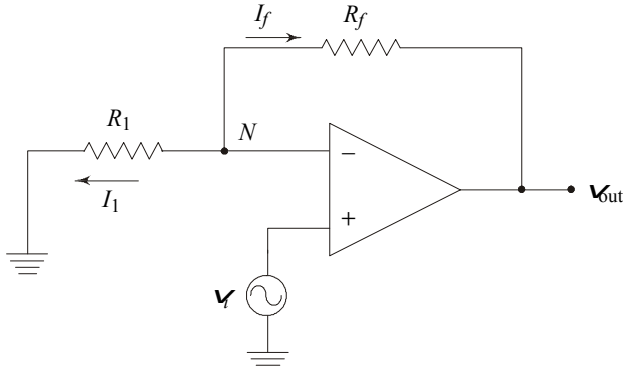


Fig. 4.14

$$\frac{V_0}{V_i} = \left[1 + \frac{R_f}{R_1}\right] A_v$$

The closed loop gain, A_v does not depend on the open loop gain, A, of the op-amp. A_v is usually greater than unity.

One of the applications of a non-inverting amplifier is emitter follower (explained earlier), wherein $R_f = 0$; hence $A_v = 1$.

4.3.4 Voltage Follower

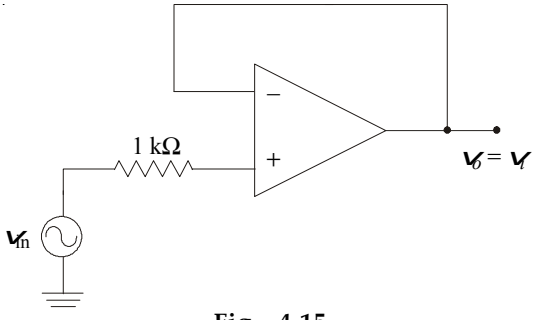


Fig. 4.15

It is a closed loop mode application of op-amp and it employs negative feedback. Since the two input terminals are virtually tied together, we get $V_0 = V_i$, i.e., output follows input. Closed loop voltage gain of the op-amp voltage follower circuit, $A_v = 1$.

The circuit is closed as a buffer in between the source and the load, to avoid loading effect (i.e., voltage follower is a current amplifier; it draws no current from the source because input sequence of the voltage follower, R_i = differential input impedance of op-amp).

4.3.5 Integrator

It is a linear signal conditioner. It is closed loop mode application of op-amp with negative feedback.

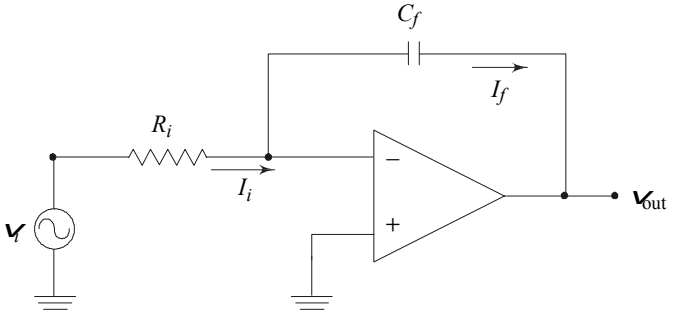


Fig. 4.16

If we give DC as input to the integrator circuit, the output will be a ramp increasing with time and output will saturate the op-amp when it reaches the biasing limits of the op-amp. Hence we do not apply DC normally to the integrator circuit.

The average value of the output AC of the integrator is the same as the average value of the input signal.

On applying the basic rules of an ideal op-amp, we get

1. $I_f = I_i$
2. The inverting terminal acts as virtual ground, $V_N = 0$.

From Rule (1),

$$\frac{(V_i - V_N)}{R_i} = C_f \frac{\mathrm{d}(V_N - V_0)}{\mathrm{d}t}$$

From Rule (2),

$$V_N = 0 \text{ (virtual ground)}$$

Therefore, $$V_0 = \frac{-1}{C_f R_i} \int v_i \, \mathrm{d}t$$

The negative sign indicates a phase shift of 180°.

The input to the circuit is AC and therefore, the circuit can be written in impedance or reactance.

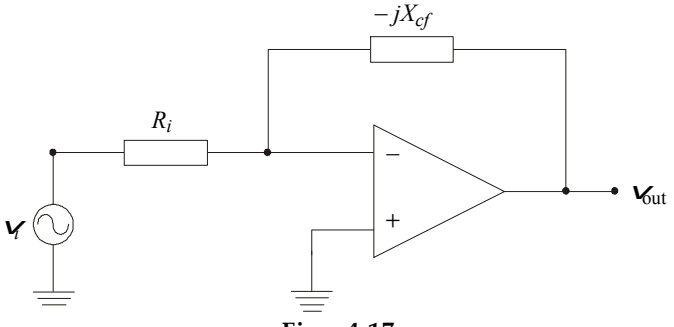


Fig. 4.17

As frequency increases, the capacitive reactance decreases. Hence output signal reduces and vice versa. The circuit allows only low frequency components to pass through the output and hence it is a *low pass filter.*

Since the integrator blocks high frequency components, it does not allow high frequency noise to pass through the output. And hence the integrator is insensitive to noise. That is why integrators are preferred to differentiator when we build electronic differential analyzer.

At very low frequencies, the capacitor (C_f) acts as open circuit thus making feedback impedance (X_{cf}) infinity.

Therefore, $$V_0 = -\left(\frac{\infty}{R_1}\right) V_i \quad (1)$$

$$V_0 = -A_v V_i \quad (2)$$

On simplifying Equation (1) and (2), we get

$$V_0 = -\infty = -V_{EE}$$

i.e., output saturates at very low frequencies. In order to avoid this problem, we should limit the low frequency gain to a safe practical value. Therefore, we connect a resistance (R_f) across C_f.

At f_c, $R_f = X_{cf}$

Therefore, $$R_f = \frac{1}{2\pi f_C C_f}$$

To minimize the effect due to input offset current, we introduce a resistor (R_{comp}) to the non-inverting terminal.

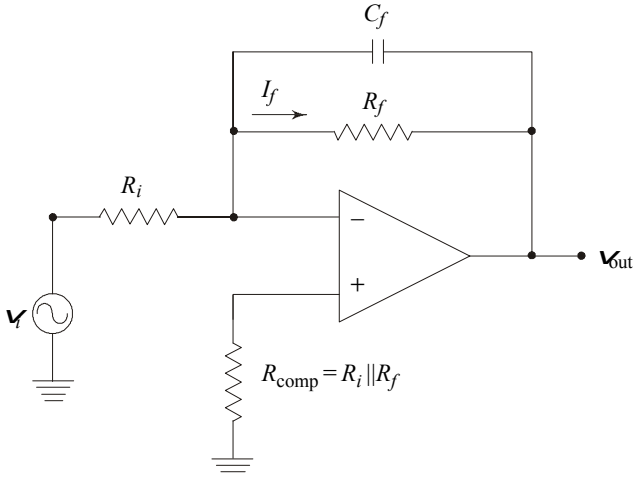


Fig. 4.18

4.3.6 Differentiator

A differentiator is a linear signal conditioner.

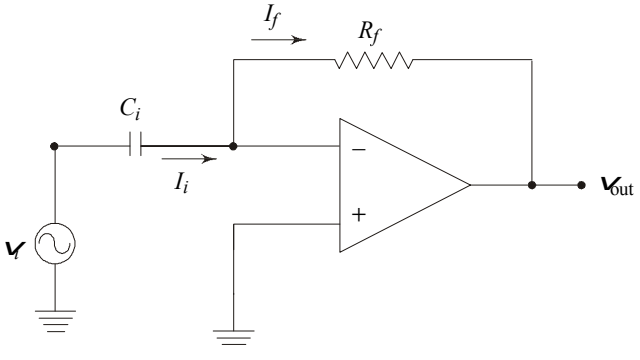


Fig. 4.19

We know that a capacitor blocks DC and hence we do not apply DC as input to the above circuit. The circuit as the name itself indicates, performs differentiation over the input variable. If the input is DC, then a constant K should represent it.

Mathematically, when differentiation is performed over the constant K, we get zero, i.e., $\frac{dK}{dt} = 0$.

Irrespective of the average value of the input AC to the differentiator, the output of the differentiator will be an AC signal with zero average value.

Applying the 2 basic rules of an op-amp, i.e.,

Therefore, $$C_i = \frac{d(V_i - V_N)}{dt} = \frac{V_N - V_0}{R_f}$$

$$V_N = 0 \text{ (virtual ground at zero potential)}$$

Therefore, $$V_0 = - R_f C_i \frac{d(V_i)}{dt}$$

Thus, $V_0 \alpha \frac{d(V_i)}{dt}$ and hence the name differetiator. Negative sign in the expression for V_0 indicates a phase shift of 180°.

$$\text{Gain,} = \frac{V_0}{V_1} = \frac{- R_f}{- j X_{Ci}}$$

$$A_v = \frac{R_f}{j X_{Ci}}$$

As the frequency increases, capacitive reactance decreases. Hence output voltage increases and vice versa. That means, this circuit allows high frequency components to pass through to the output and it blocks low frequency components. Hence it is a *high pass filter.*

At very high frequencies, $X_{ci} \simeq 0$. Then output voltage becomes infinite (saturation). To avoid this saturation, we should add a resistance in series with the input capacitor.

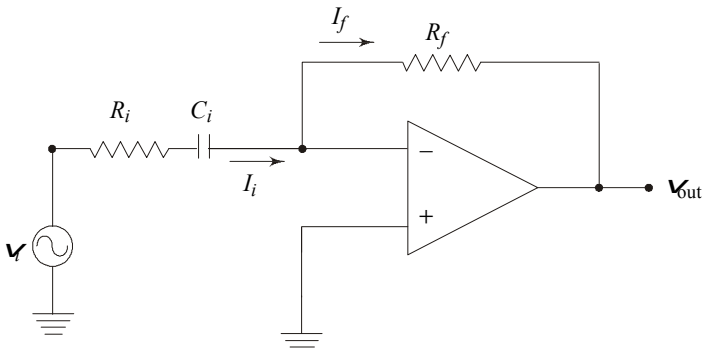


Fig. 4.20

R_i should be selected to be in the range of 50 Ω to 200 Ω so that a major portion of V_i should appear across C_i as it was in the basic circuit for differentiator.

$$f_c = \frac{1}{2\pi R_i C_i}$$

Even after the introduction of R_i into the network, the expression for output does not change if the circuit is operated in the differentiation range because the voltage across C_I is almost equal to V_i.

Disadvantages of a Differentiator

1. A differentiator is sensitive to high frequency noise.
2. Noise can be assumed as a superimposition of several sinewaves of different frequencies. If noise is defined as $V_i = V_m \sin \omega t$, where V_m is the magnitude of the noise and ω is its frequency (radians).

Noise being a high frequency noise, ω is large. Then output noise is given by,

$$V_{0n} = - R_f C_i \frac{d(V_i)}{dt}$$

$$V_{0n} = - R_f C_i [V_m \omega \cos \omega t]$$

Magnitude of the output noise = $+ R_f C_i V_m \omega$. Since at high frequencies, ω is large, the differentiator is highly susceptible to high frequency noise.

The above two disadvantages are overcome by having a capacitor across R_f.

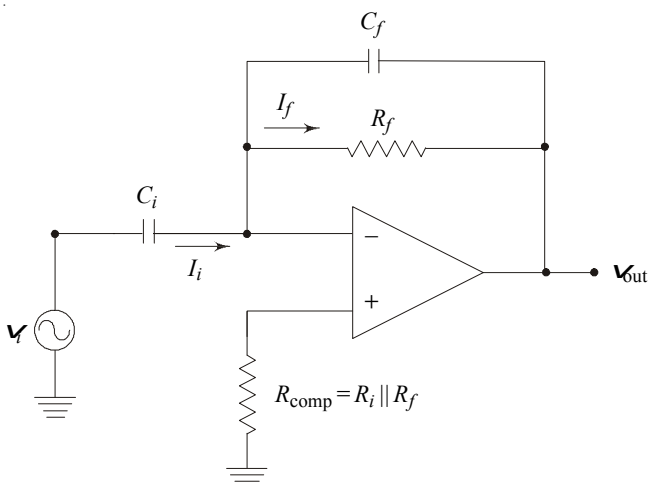


Fig. 4.21

The capacitor C_f should act as open circuit in the lower frequency range and at very high frequencies, the capacitor C_f should short circuit R_f. This is possible if and only if C_f is very small compared to C_i.

To minimize the effect due to the input offset current, we introduce a resistor (R_{comp}) to the non-inverting terminal.

Experiment (Linear Application of Op-Amp)

Aim: ***To Study the Following Applications of Op-Amp Using IC 741***

1. Voltage follower.
2. Inverting amplifier.
3. Non-inverting amplifier.
4. Variable voltage gain amplifier.
5. Adder.
6. Subtractor.

7. Differential amplifier.
8. Integrator.
9. Differentiator.

Equipments Required:

Equipments	Range	Quantity
Dual power supply	(15-0-15) V	1
Signal generator	(1 Hz-1MHz)	1
Regulated power supply	(0-30) V	2
CRO	100 kHz	1

Voltage Follower

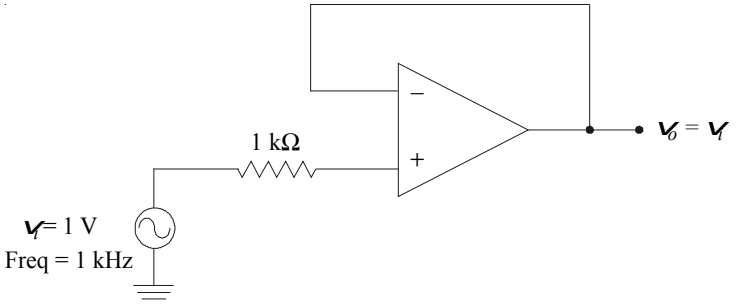


Fig. 4.22

Inverting Amplifier

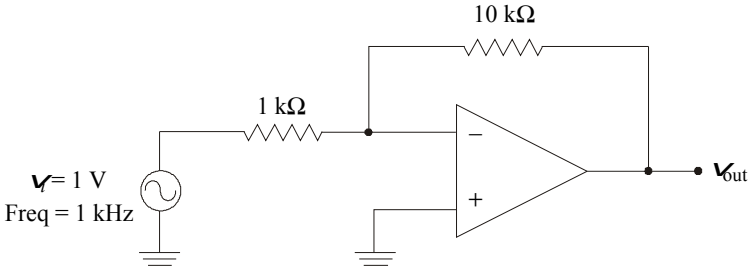


Fig. 4.23

Non-Inverting Mode

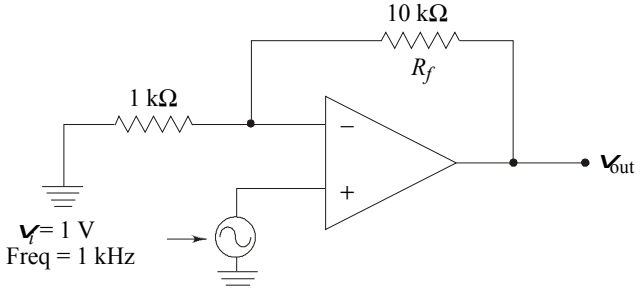


Fig. 4.24

Adder

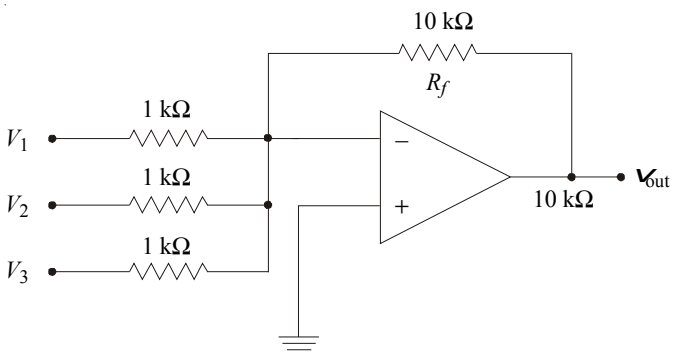


Fig. 4.25

Subtractor

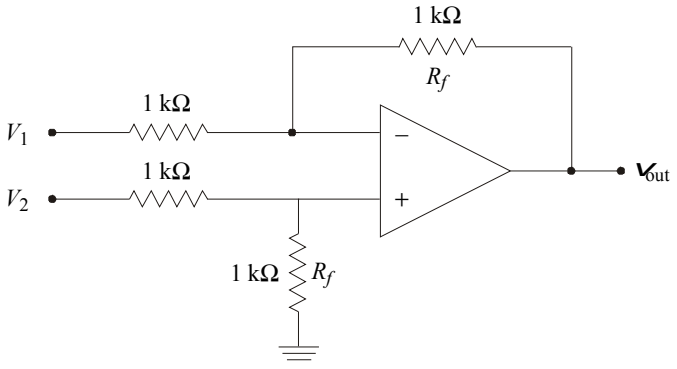


Fig. 4.26

Integrator

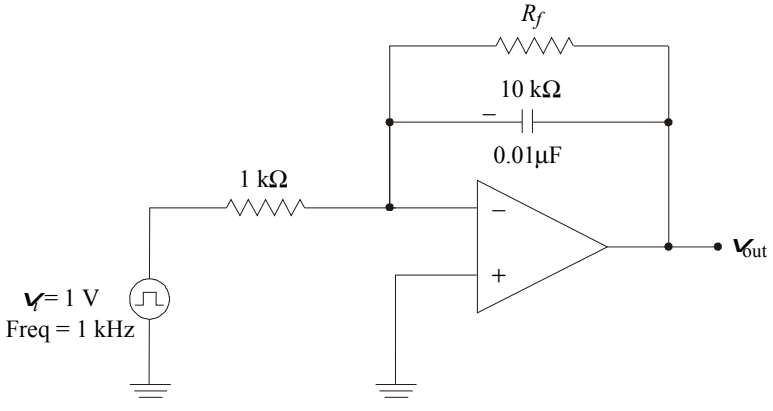


Fig. 4.27

Differentiator

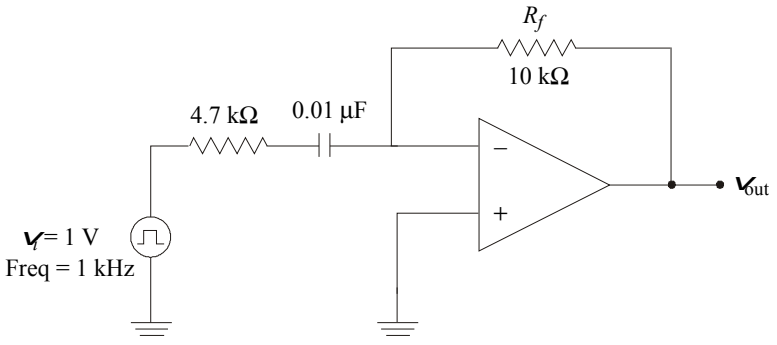


Fig. 4.28

Differential Amplifier $V_1 \neq V_2 ; f_1 = f_2$

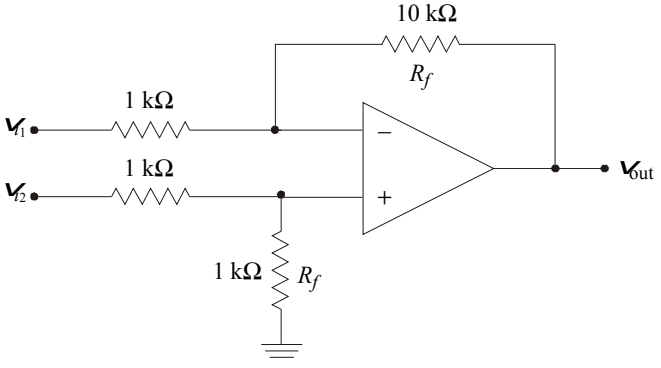


Fig. 4.29

Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Give the input signal as specified.
3. Switch on the dual power supply.
4. Note down the outputs from the CRO.
5. Draw the necessary waveforms on the graph sheet.
6. Repeat the procedure for all the circuits.

Result:

The applications of the IC 741 were studied.

Exercise:

1. Explain the difference between differentiators and integrators and give one application for each.
2. Explain why integrators are preferred over differentiators in an analog computer.
3. Draw a practical differentiator circuit that overcomes the drawbacks of an ordinary differentiator circuit.

4. Design an adder circuit to get the following output

$$V_0 = -[0.1\ V_1 + V_2 + 10\ V_3]$$

4.3.7 Instrumentation Amplifier

The instrumentation amplifier is one of the most useful and versatile amplifiers widely used in data acquisition units. The op-amps at the input provide high Z_{in} and the third op-amp along with four equal resistors, R, forms a differential amplifier with a gain of unity. To determine the output of the circuit E_3, E_4 should be known. The instrumentation amplifier is used in a situation where the input is small and noise level is high. The important features of an instrumentation amplifier are as follows:

1. High gain accuracy
2. High CMRR
3. Low DC offset
4. High gain stability
5. Low Z_0.
6. High Z_{in}

Instrumentation amplifier is basically a difference amplifier, which amplifies the difference between two signals and that the inputs are direct-coupled. Instrumentation amplifier has two stages:

1. Buffer stage.
2. Amplifier stage.

The first stage is the buffer stage whose input impedance is very high. This results in the perfect isolation between the input signal and output signal. This will avoid an overloading condition. A buffer is basically a voltage follower (unity gain amplifier) which is capable of giving the required drive to the second stage, amplifier stage.

The second stage is nothing but a difference amplifier, which amplifies the signal difference coming at the inverting and non-inverting terminals. This offers a very good CMR capability.

Some important areas of application of an instrumentation amplifier are measurement and control of temperature, humidity, light intensity, biological signals, etc.

The gain of the instrumentation amplifier is given by;

$$\frac{V_{out}}{(E_1 - E_2)} = A = \left(1 + \frac{2R_2}{R_1}\right)\left(-\frac{R_4}{R_3}\right) \qquad \text{when } E_1 > E_2$$

Experiment (Instrumentation Amplifier)

Aim: ***To Study the Performance of and Insturmentation Amplifier.***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1
Dual power supply	(12-0-12) V	1

Circuit Diagram:

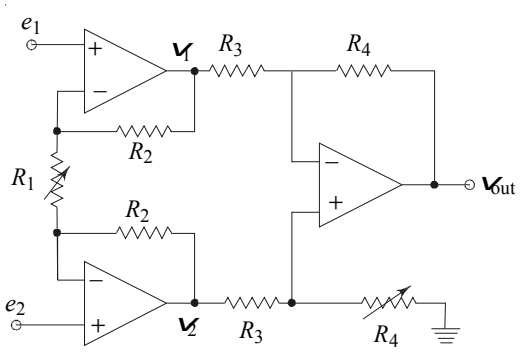


Fig. 4.30

If $e_1 > e_2;\ f_1 = f_2$

$$(e_1 - e_2) = (e_1 - e_2)\left(1 + \frac{2R_2}{R_1}\right)$$

$$e_{out} = (e_1 - e_2)\left(-\frac{R_4}{R_3}\right)$$

Therefore, $$A = \frac{V_{out}}{(e_1 - e_2)} = \left(\frac{-R_4}{R_3}\right)\left(1 + \frac{2R_2}{R_1}\right)$$

If $R_1 = R_2 = R_3 = R_4 = 10\ \text{k}\Omega$

then, $\boxed{\text{A} = -3}$

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Set the inputs E_1 and E_2 at different values but at the same frequency.
3. Adjust R_1 to a particular value.
4. Switch on the dual power supply.
5. Calculate the theoretical gain from the given formula and verify with the practical values.
6. Repeat the above procedure for different values of R_1.

4.4 OP-AMP NON-LINEAR APPLICATION

4.4.1 Comparator

A comparator is a non-linear signal processor. It is an open loop mode application of op-amp operated in saturation mode. Comparator compares a signal voltage at one input with a reference voltage at the other input. Here the op-amp is operated in the open loop mode and hence the input is $\pm V_{sat}$. It is basically classified as inverting comparator and non-inverting comparator. In a non-inverting comparator, V_{in} is given to the +ve terminal and V_{ref} to the –ve terminal. When $V_{in} < V_{ref}$, the output is $-V_{sat}$ and when $V_{in} > V_{ref}$, the output is $+V_{sat}$. In an inverting comparator, input is given to the inverting terminal and reference is given to the non-inverting terminal.

The comparator can be used as a:

1. Zero crossing detector
2. Window detector
3. Time marker
4. Phase meter

Non-Inverting Comparator

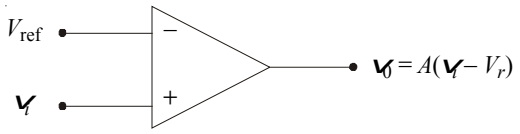


Fig. 4.31

When V_R is positive, $t_{ON} \neq t_{OFF}$ and $t_{ON} < t_{OFF}$

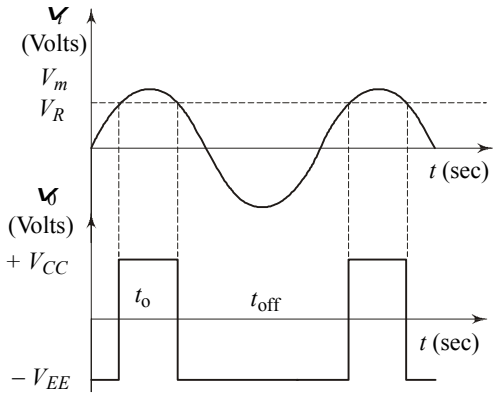


Fig. 4.32

Note: Average value of the output is not zeroing in the case of comparator.

When V_R is negative, $t_{ON} \neq t_{OFF}$ and $t_{ON} > t_{OFF}$

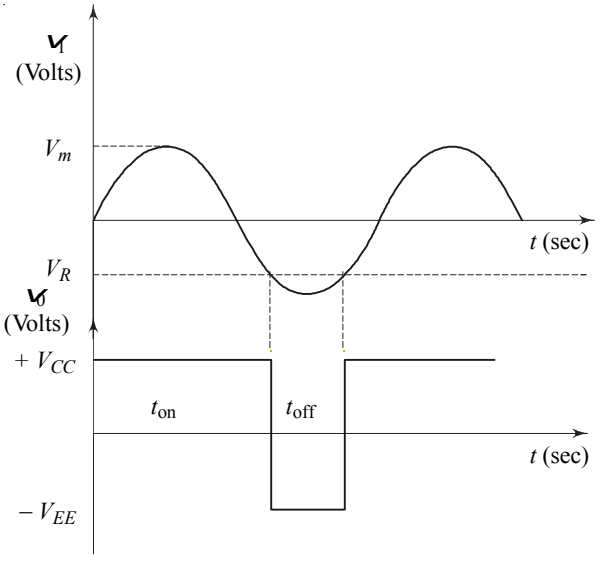


Fig. 4.33

If V_R is beyond the swing of the input, (V_R is positive) there will not be any comparison.

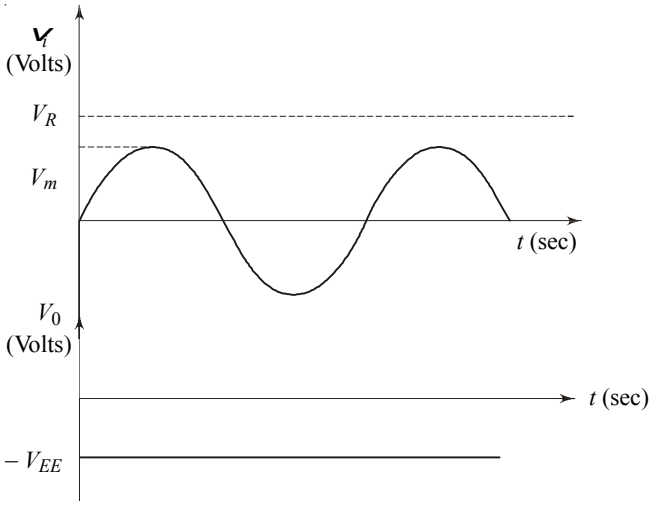


Fig. 4.34

When V_R is negative:

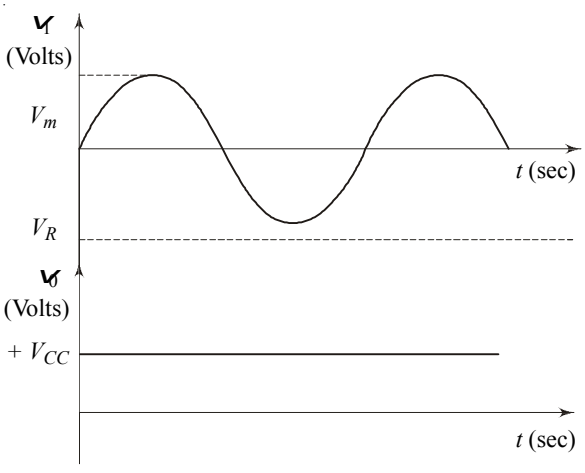


Fig. 4.35

Exercise:

Analyze the inverting comparator for the above said conditions.

Window Comparator It is obtained by connecting an inverting type comparator and a non-inverting type comparator as shown in the figure. The comparators in the window circuit have different reference.

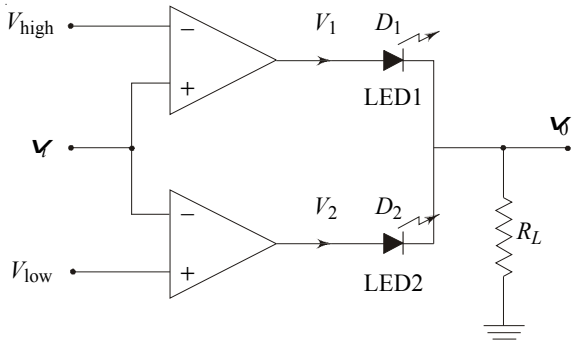


Fig. 4.36

Tabulation:

V_i (Volts)	V_1	D_1	V_2	D_2	V_0
$>V_{high}$ $>V_{low}$	$+V_{CC}$	ON	$-V_{EE}$	OFF	$+V_{CC}$
$<V_{high}$ $>V_{low}$	$-V_{EE}$	OFF	$-V_{EE}$	OFF	0
$<V_{high}$ $<V_{low}$	$-V_{EE}$	OFF	$+V_{CC}$	ON	$+V_{CC}$

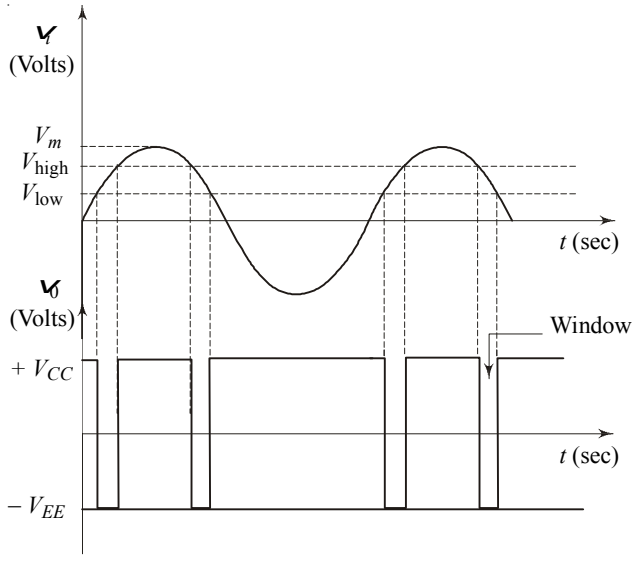


Fig. 4.37

The output V_0 is zero when V_i lies between V_{high} and V_{low}, and the output is $+ V_{cc}$. Otherwise, the circuit checks if the input V_i lies between V_{high} and V_{low} or not, and hence, the name *Sense amplifier*.

Zero Crossing Detector It is a non-inverting signal processor. It is an open loop/saturation mode operation of op-amp. It is basically a comparator with zero reference voltage.

Types:

1. Inverting type.
2. Non-inverting type.

Inverting Type Zero Crossing Detector

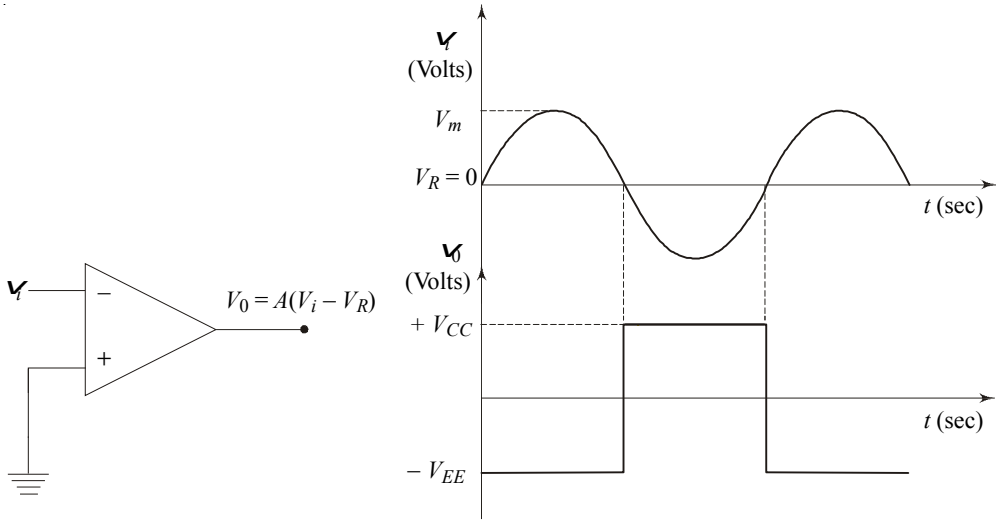


Fig. 4.38

Whenever the input crosses zero voltage axis, the output changes abruptly and hence the name *zero crossing detector*. Since the input is given to the inverting terminal, the output signal is out of phase (180°) with respect to the input signal. Hence the name.

Non-Inverting Type Zero Crossing Detector

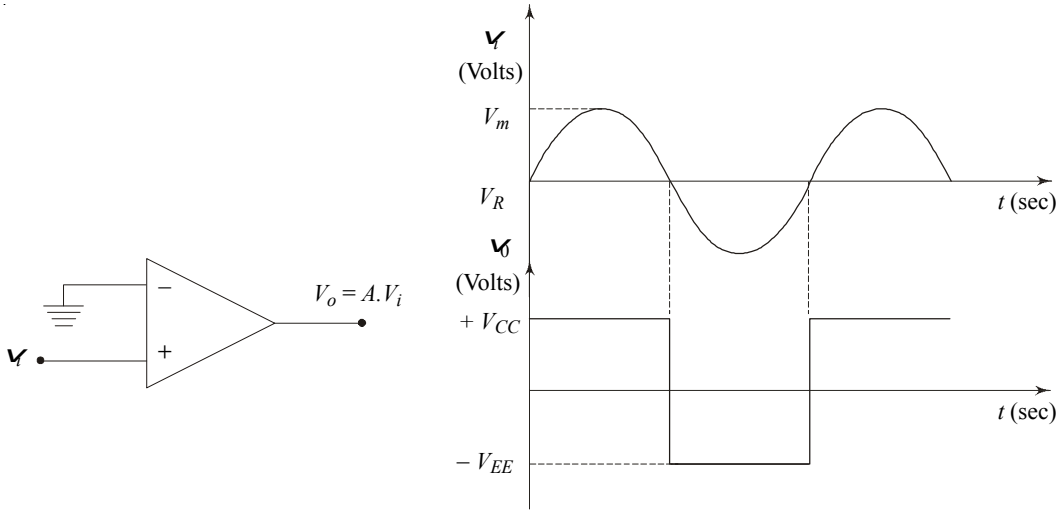


Fig. 4.39

Here the input signal is given to the non-inverting terminal. So the output signal is maintains the same phase (0°) as that of the input signal.

4.4.2 Square Wave Generator

This is operated in the astable mode. The op-amp is operated in the saturation region and the output swings between ± V_{sat}. A +ve feedback of $\beta = \dfrac{R_2}{R_1 + R_2}$ is provided to the non-inverting terminal. The output is fed back to the inverting terminal after integration through a RC network. When the input and the –ve terminal fall above or below the voltage at the +ve terminal, the output switches resulting in a square wave output. The frequency of oscillation of the output waveform is given by;

$$f_0 = \frac{1}{2RC}$$

Astable Multivibrator It is a free running square wave generator. It is a modified version of schmitt trigger. The circuit employs both positive and negative feedback.

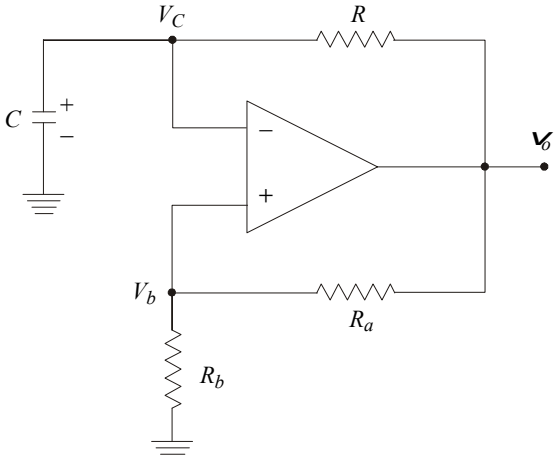


Fig. 4.40

The circuit is in the open loop mode or saturation mode, i.e., V_0 is either $+V_{CC}$ or $-V_{EE}$. Therefore, we can define two tripping points at the non-inverting terminal as given below.

$$V_{b_1} = \text{UTP} = R_b \left(\frac{+V_{CC} - 0}{R_a + R_b} \right)$$

$$V_{b_2} = \text{LTP} = R_b \left(\frac{-V_{EE} - 0}{R_a + R_b} \right)$$

Tabulation:

Present state			Next state		
V_C	V_b	$V_0 = A_0 (V_b - V_C)$	V_C	V_b	$V_0 = A_V (V_b - V_C)$
0	V_{b_1}	$+V_{CC}$	$V_C < V_{b_1}$	V_{b_1}	$+V_{CC}$
$V_C > V_{b_1}$	V_{b_2}	$-V_{EE}$	$V_C > V_{b_2}$	V_{b_2}	$-V_{EE}$
$V_C < V_{b_2}$	V_{b_1}	$+V_{CC}$	$V_C < V_{b1}$	V_{b_1}	$+V_{CC}$

In the beginning, the capacitor voltage is zero as it is uncharged. Let us assume that a small +ve input offset voltage appears across input terminals with respect to the circuit operated in saturation mode. Therefore, the +ve input offset voltage drives the op-amp output to the +ve saturation, $+V_{CC}$. This output voltage charges the capacitor C, as a result of which the voltage across the capacitor increases. This increases the input to the inverting terminal. As long as this voltage is less than the voltage at the non-inverting terminal, the output V_0 remains at $+V_{CC}$. When voltage across the capacitor exceeds input to the non-inverting terminal, the output changes to $-V_{EE}$. This, in turn, make non-inverting terminal much more –ve than inverting terminal and the output remains at $-V_{EE}$. When the output is $-V_{EE}$, capacitor starts discharging and recharging in the –ve direction. When the capacitor voltage falls below the non-inverting terminal potential, the output abruptly changes from $-V_{EE}$ to $+V_{CC}$. Thus the cycle repeats.

Sinewave Generator To generate a sinusoidal waveform an oscillator is used. The oscillator employs +ve feedback and it generates sustained oscillation when the Barkhause criteria is $A\beta = 1$ and angle = 360° is satisfied. The oscillations may be either in the high frequency range or low frequency range. LC oscillators are used to generate high frequency and RC oscillators are used for low frequency. Here we use a wein-bridge oscillator to generate a sinusoidal output in the audio frequency range. In the wien-bridge oscillator, both +ve and –ve feedbacks are used. From the circuit, it is clear that the feedback signal in this circuit is connected to the +ve input terminal so that the op-amp works as a non-inverting amplifier. To obtain sustained oscillation, when the gain is greater than 3, a –ve feedback is used so that the gain is brought to the required value, i.e., $A_v = 3$. The frequency of oscillation is given by;

$$f_0 = \frac{1}{2\pi RC}$$

Triangular Waveform Generator A triangular wave is obtained by integrating a square wave. Though the amplifier of the square wave is constant at $\pm V_{sat}$. The amplifier of the triangular wave will decrease as the frequency increase. This is because the reactance of the capacitor C_2 in the feedback circuit decrease at high frequency. The frequency of oscillation is given by;

$$f_0 = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2}$$

Experinent (Non-Linear Application of Op-Amps)

Aim: ***To Design a Suitable Circuit to Study the Following Non-Linear Applications of Op-Amp***

1. Comparator.
2. Sine wave generator.
3. Square wave generator.
4. Triangular wave generator.

Equipments Required:

Equipments	Range	Quantity
Dual power supply	(15-0-15) V	1
Signal generator	(0-1) MHz	1
Regulated power supply	(0-30) V	1
CRO	(0-20) MHz	1

Circuit Diagram:

Comparator: Zero crossing detector:

$V_0 = + V_{SAT}$ when $V_i < 0$

$V_0 = - V_{SAT}$ when $V_i > 0$

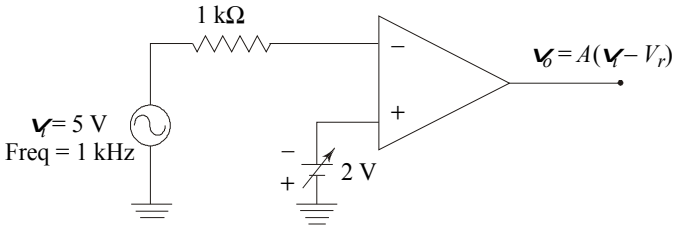


Fig. 4.41

Positive Comparator:

$V_0 = + V_{SAT}$ when $V_i < V_{REF}$

$V_0 = - V_{SAT}$ when $V_i > V_{REF}$

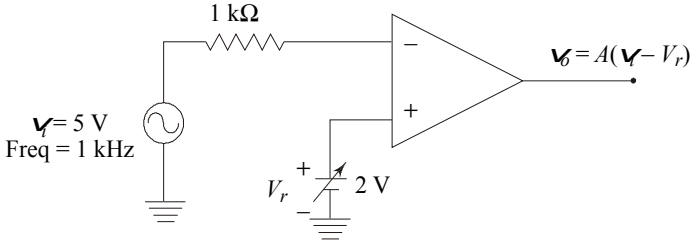


Fig. 4.42

Negative Comparator:

$V_0 = - V_{SAT}$ when $V_i < V_{REF}$

$V_0 = + V_{SAT}$ when $V_i > V_{REF}$

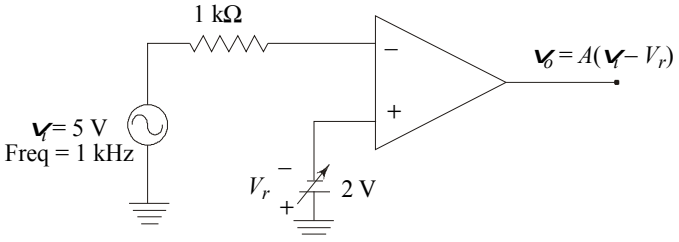


Fig. 4.43

Sinewave Generator:

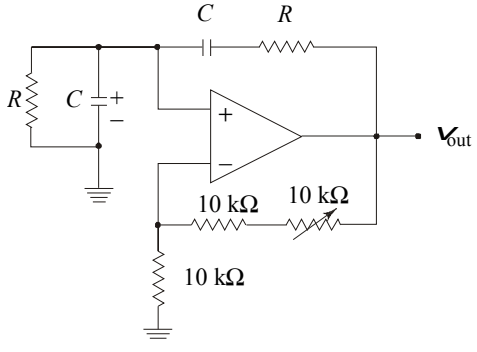


Fig. 4.44

To produce sustained osicllation, gain should be equal to 3, i.e., if $1 + \frac{R_f}{R_i} = 3$, then $R_f = 2\ R_i$.

Square Wave Generator:

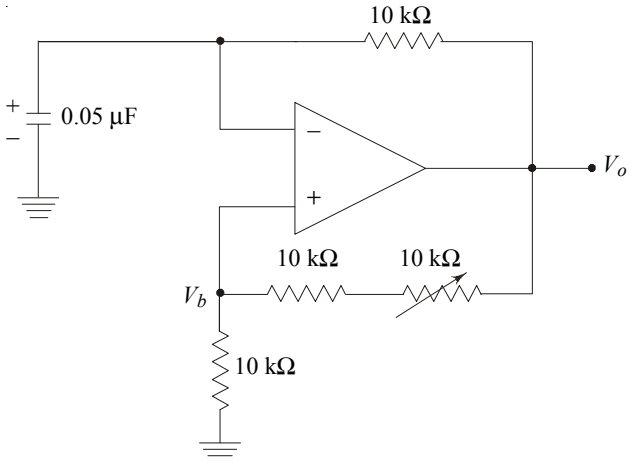


Fig. 4.45

Triangular Wave Generator:

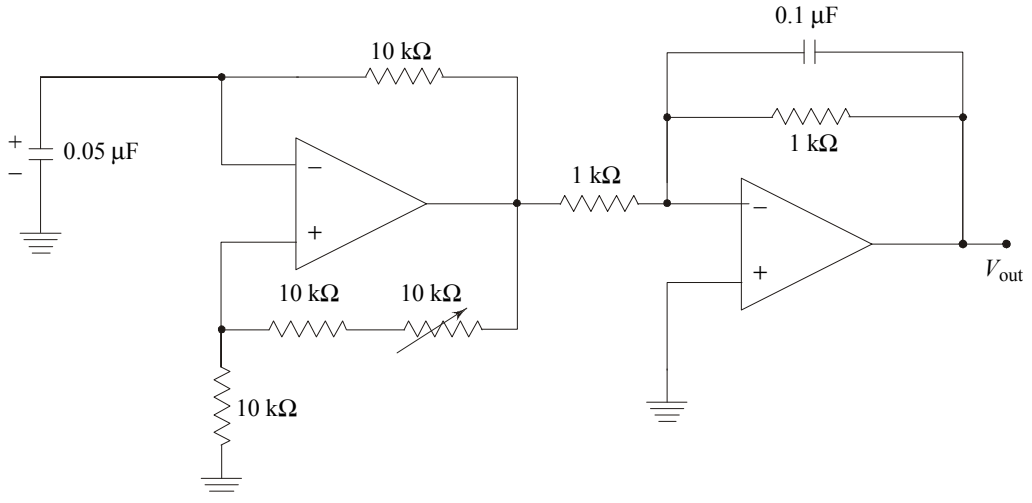


Fig. 4.46

Procedure:

Comparator:

1. Connect the circuit as shown in the circuit diagram.
2. Give a sinusoidal input of 4 V_{pp} to the inverting terminal.
3. For a zero crossing detector, connect the non-inverting terminal to ground.
4. Switch on the dual power supply.
5. Observe the output waveform on a CRO.
6. For a positive and negative comparator give a reference voltage of ± 1V DC respectively to the non-inverting input.

7. Observe the output waveform on a CRO.
8. Draw the output and input waveforms for all the three circuits on a graph sheet.

Sine Wave Generator:

1. Connect the circuit as shown in the circuit diagram.
2. Switch on the dual power supply and observe the output waveform on a CRO.
3. Adjust the potentiometer to get an undistorted waveform.
4. Calculate the time period and determine the frequency.
5. Verify it with the theoretical frequency. Calculate by using the formula,

$$f = 1/2\pi RC$$

6. Repeat the above procedure for different values of R and C.

Square Wave Generator:

1. Connect the circuit as shown in the circuit diagram.
2. Switch on the dual power supply and observe the output on a CRO.
3. Adjust the potentiometer to obtain an undistorted output.
4. Calculate the output frequency and verify it with the theoretical frequency obtained from the formula,

$$f = \frac{1}{2RC}$$

Triangular Wave Generator:

1. Connect the output of the square wave generator to an integrator circuit.
2. Observe the output waveform on a CRO and determine the frequency.

Design:

Sine Wave Generator:

We know, $f = 1/2\pi RC$

Let, $f = 1$ kHz

$$R = \frac{1}{2\pi fC}$$

Choose, $C = 0.01$ μF

$$R = 1/2\pi \times 10^3 \times 0.01 \times 10^{-6}$$

$$= ?$$

Square Wave Generator:

We know, $f_0 = \frac{1}{2RC}$

Let, $f_0 = 1$ kHz

Choose, $C = 0.05$ μF

$$R = 1/2 \times 10^3 \times 0.05 \times 10^{-6}$$

$$R = 10\ \text{k}\Omega$$

Choose, $R_1 = 1.16\ R_2$

If, $R_2 = 10$ kΩ

Then, $R_1 = 11.6$ kΩ

Choose 10 kΩ in series with a 10 kΩ potentiometer.

Triangular Wave Generator:

Design for the square wave generator is given above. Design for the integrator circuit is as follows:

Let, $R_4 = 10\ R_3$

If, $R_3 = 100\ \text{k}\Omega$

Then, $R_4 = 1\ \text{M}\Omega$

$$f_0 = \frac{1}{2\pi R_3 C_2}$$

Given, $R_3 = 100\ \text{k}\Omega$

Choose, $C_2 = 0.01\ \mu\text{F}$

Then, $f_0 = 1/2\pi \times 100 \times 10^3 \times 0.01 \times 10^{-6}$

$= ?$

Result:

The non-linear applications of the op-amp were studied.

Exercises:

1. Design a circuit to convert a square wave into a series of positive pulses.
2. What is a window detector?
3. What is the difference between a sawtooth wave and a triangular wave?
4. How do you recognize that positive feedback is being using in an op-amp oscillator circuit?

4.4.3 Schmitt Trigger

It is a regenerative comparator or it is comparator with hysteresis. The circuit is a closed loop mode application of op-amp employing only +ve feedback and hence it is equivalent to an open loop mode application operated in saturation.

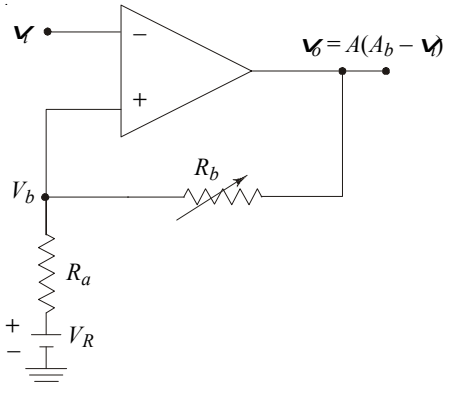


Fig. 4.47

The output V_0 takes two values, either + V_{CC} or – V_{EE}. Let the voltage at the non-inverting terminal be V_b with respect to V_i , the time varying signal. V_R is the fixed reference voltage source. Corresponding to the two values at the output, we can define two values for V_b and they are known as threshold voltages or trip points. One is known as UTP (upper trip point) and the other is known as LTP (lower trip point).

$$V_{b_1} = \text{UTP} = V_R + R_b \left(\frac{|+V_{CC}| - V_R}{R_a + R_b} \right)$$

$$V_{b_2} = \text{LTP} = V_R - R_b \left(\frac{|-V_{EE}| + V_R}{R_a + R_b} \right)$$

Tabulation:

Present state			Next state		
V_i	V_b	$V_0 = A_0(V_b - V_i)$	V_i	V_b	$V_0 = A_V(V_b - V_i)$
$V_i > V_{b_1}$	V_{b_1}	$+V_{CC}$	$V_i > V_{b_1}$	V_{b_2}	$-V_{EE}$
$V_i > V_{b_2}$	V_{b_2}	$-V_{EE}$	$V_i < V_{b_2}$	V_{b_1}	$+V_{CC}$
$V_i < V_{b_1}$	V_{b_1}	$+V_{CC}$	$V_i > V_{b1}$	V_{b_2}	$-V_{EE}$

Hysteresis Curve

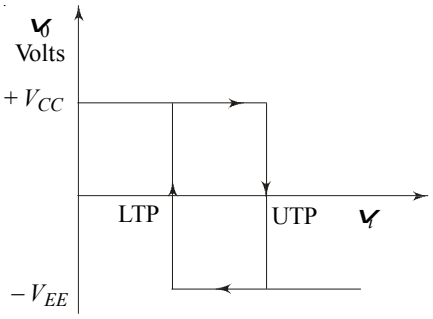


Fig. 4.48

The difference between V_{b_1} and V_{b_2} is known as hysteresis. This hysteresis is due to +ve feedback. The hysteresis avoids false triggering of the circuit by noise. If the peak to peak noise voltage is less than the hysteresis, then there is no way the noise can provide false triggering.

Example: $V_{b_1} = 2$ V and $V_{b_2} = 3$ V then, $(V_{b_1} - V_{b_2}) = 1.7$ V.

If the peak to peak voltage of the noise is less than 1.7 V, then false triggering is impossible by the noise.

When the input times varying signal V_i crosses V_{b_1} in the +ve direction (increasing), then the output makes transition from $+V_{CC}$ to $-V_{EE}$. Similarly, when the input V_i crosses V_{b_2} in the –ve direction (decreasing), then the output makes transition from $-V_{EE}$ to $+V_{CC}$. This is sketched in the hysteresis curve as shown in the figure.

The UTP and LTP are nothing but the potentials available at non-inverting terminal of the op-amp when the output is $+V_{sat}$ and $-V_{sat}$ respectively.

Experiment (Schmitt Trigger)

Aim: ***Design and Test the Schmitt Trigger for the given UTP and LTP***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1
Dual power supply	(12-0-12) V	1

Circuit Diagram:

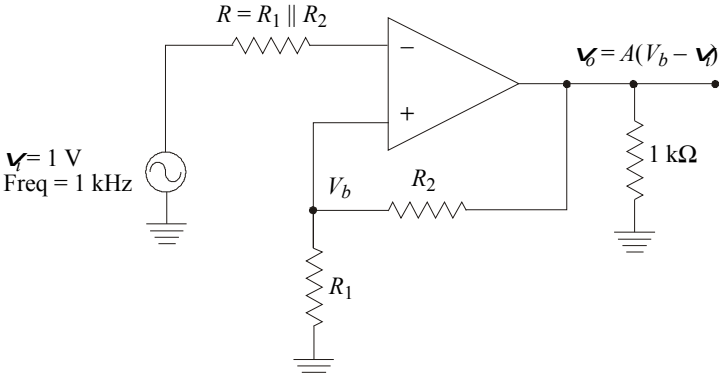


Fig. 4.49

Design:

Given, $V_R = 0$ and $\pm V_{sat} = \pm 12$ V.

Assume, $V_{b_1} = V_{b_2}$

$$V_{b_1} = \text{UTP} = R_1 \left(\frac{+V_{sat}}{R_1 + R_2} \right)$$

$$V_{b_2} = \text{LTP} = R_1 \left(\frac{-V_{sat}}{R_1 + R_2} \right)$$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Set input signal say 1 V, 1 KHz using signal generator.
3. Observe the input and output waveform on the CRO.
4. Plot the graphs: V_i vs time
   V_0 vs time

Model Waveform:

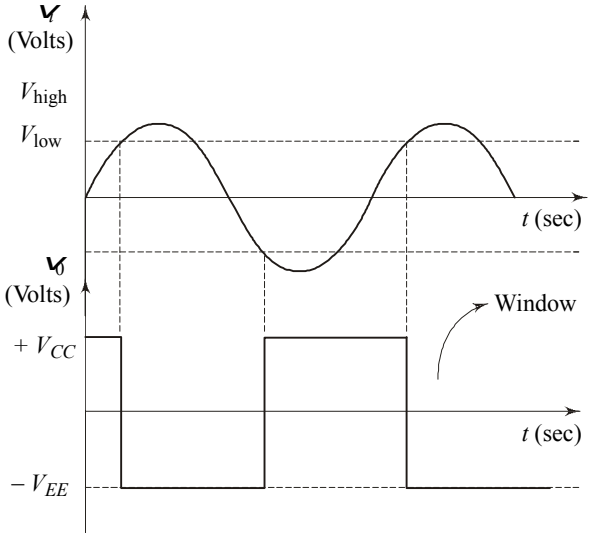


Fig. 4.50

Result:

Parameter	Theoretical	Practical
UTP	$R_1\left(\frac{+V_{sat}}{R_1+R_2}\right)$	
LTP	$R_1\left(\frac{-V_{sat}}{R_1+R_2}\right)$	

4.4.4 Precision Rectifier

A rectifier is a DC voltage source. It will have finite output impedance in series with a DC voltage. Therefore a rectifier can be modeled as a constant voltage source in series with a resistance.

The rectification becomes a crucial problem when we have to rectify millivolt signal at high frequencies. This is because of the following two drawbacks of conventional diodes.

1. The conventional diodes require at least 0.2 V (*Ge*) [0.7 V (*Si*)] across them for a forward bias and hence a millivolt signal cannot forward bias a conventional diode.
2. Switching speed of conventional diode will be very low.

If we use a diode in the forward path of op-amp, cut-in voltage of the diode will be divided by the large open loop gain, thus making the diode an ideal one (i.e., a diode with zero cut-in voltage).

When we use a conventional diode in the feedback path of an op-amp, we can rectify millivolt signals at high frequencies. This set up is then called *precision rectifier* (for obvious reason!).

3. In case of a conventional rectifier, output peak will be less than the input peak. This is due to loss of voltage across the diode due to finite cut-in voltage. But in the case of precision rectifier diodes, it will have zero cut-in voltage and hence output peak will be same as input peak.

   A precision diode can be made to operate as
   1. Half-wave rectifier
   2. Full-wave rectifier
   3. Peak detector
   4. Clipper
   5. Clamper

Half-Wave Rectifier The circuit employs –ve feedback. The circuit is in the active mode operation.

During the beginning of the +ve half-cycle, the diode D will not be conducting, V_0^1 attains a value $+V_{CC}$, inturn forward biasing the diode D, i.e.

At $t = 0$, diode is off, therefore, op-amp is open circuited.

$$V_0 = A\,(V_{in} - V_0)$$

$$V_0 = A\,(V_{in} - 0)$$

$$V_0 = \infty$$

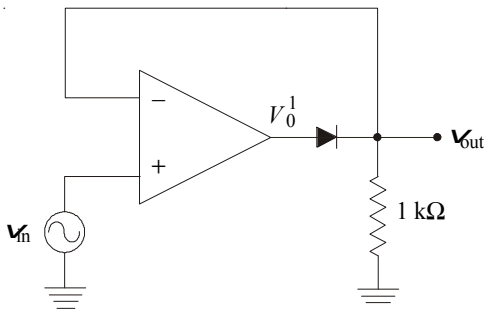


Fig. 4.51

$V_0 \approx +V_{CC}$ (saturation voltage)

Now the configuration is of the circuit will be that of a voltage follower and thus we get the +ve half-cycle at the output same as the +ve half-cycle of the input.

During the –ve half-cycle of the input, V_0^1 changes to $-V_{EE}$ and it reverse biases the diode D and hence V_0^1 will be disconnected from V_0. V_0 is now measured across the load resistance, R_L and it is zero because no current flows through R_L.

Note: For –ve rectification, reverse the polarity of the diode.

Full-Wave Rectification A full-wave rectification is achieved by employing the following logic.

Full wave rectified output = Input AC + 2 × Half-wave rectified output.

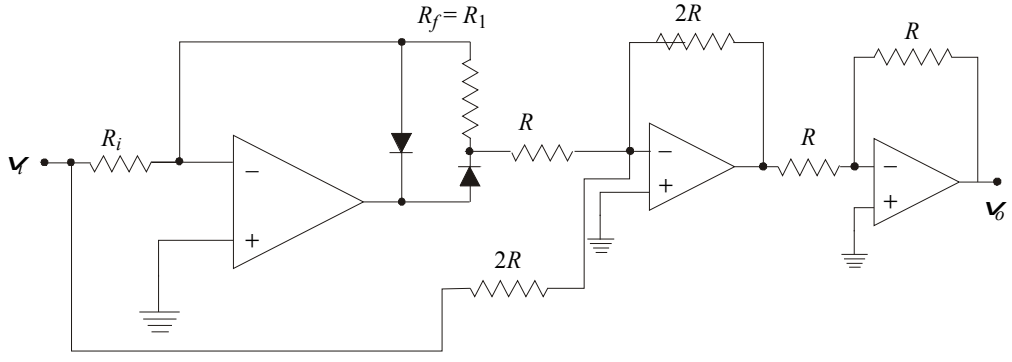


Fig. 4.52

Experiment (Precision Rectifier)

Aim: ***To Design a Precision Rectifier and Study its Operation using IC 741***

Equipment Required:

Equipment	Range	Quantity
Dual Power supply	(15-0-15) V	1
Signal generator	1 MHz	1
CRO	15 MHz	1

Circuit Diagram:

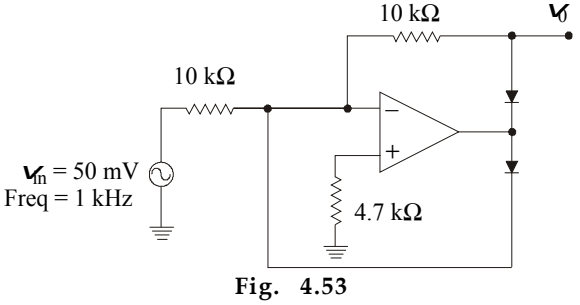


Fig. 4.53

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Give a sinusoidal input of 100 mVpp, 1 kHz from a signal generator.
3. Switch on the dual power supply and note down the output from the CRO.
4. Repeat the above procedure by reversing the diodes.

Model Waveform:

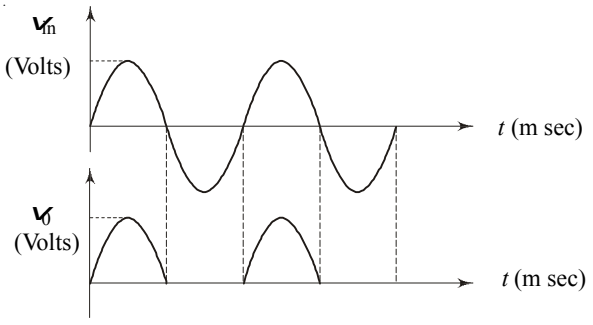


Fig. 4.53 A

Result:

The operation of the precision rectifier is studied using IC 741.

Exercises:

1. What is virtual ground?
2. What is the significance of a precision rectifier?
3. Explain the operation of a precision full wave rectifier.

4.4.5 V-I Converter

It is an inverting amplifier. It is a linear closed loop mode application of op-amp employing –ve feedback. It is used whenever current is required as input. There are two types of V-I converters:

1. V-I converter with floating load
2. V-I converter with grounded load

In the first case, the load is floating and the output current is given by $i_L = {}_{i} / R_1$. In this circuit, the current through the source and load are the same.

In the second type, the load is grounded. Here the op-amp operates in the non-inverting mode with a gain of 2. Here also $i_L = \frac{V_i}{R}$. The Z_{in} of this circuit is very high and it draws very little current from the source. This circuit finds applications in an AC voltmeter, DC voltmeter, LED tester, Zener diode tester, etc.

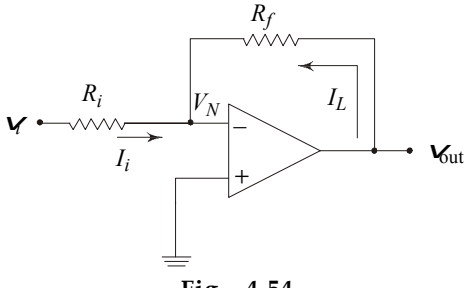


Fig. 4.54

We shall assume that a load R_L is connected as feedback resistor, R_f. We shall consider current through R_f, i.e., i_L as the output.

$$i_L = -\frac{V_i - V_N}{R_i} = -\frac{V_i}{R_i}$$

$V_N = 0.$

Negative sign indicates that there is 180° phase shift between input and output. The current through the load is independent of the value of the load R_L or the voltage across the load $\pm V_0$ and hence the name constant current sources. The input applied is voltage and output considered is current and hence the name *voltage to current converter* or *trans-conductance amplifier*.

None of the terminal of the load (R_L) is connected to the actual ground in the circuit and hence the load is said to be a floating type load.

Exercises:

Draw the circuit for a V-I converter with a grounded load. What condition will be the load current be proportional to source voltage? Prove the same.

4.4.6 I-V Converter

A small amount of current is produced by the photocell, photo diode and photo voltaic cell, which is proportional to the incident energy. This is converted to voltage by using an I-V converter and the amount of light or radiant energy incident on the photo device is measured. When an op-amp is used in such a circuit, even a very low value of I can be measured. Thus a op-amp is used in a photo detector application.

Experiment (Study of V-I and I-V Converter Using Op-Amp)

Aim: ***To Design a Voltage to Current (V-I) and Current to Voltage Converter and Study their Operation Using IC 741***

Equipments Required:

Equipment	Range	Quantity
Dual power supply	(15-0-15) V	1
Regulated power supply	(0-30) V	1
Signal generator	(0-1) MHz	1
CRO	(0-15) MHz	1
Ammeter	(0-30) μA	1

Circuit Diagram:

Voltage to Current Converter:

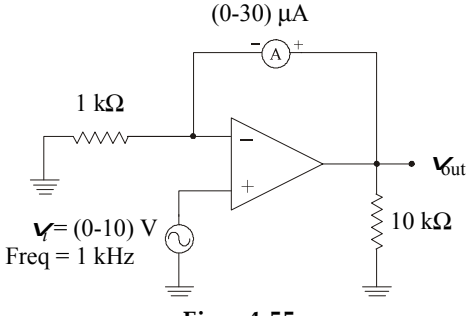


Fig. 4.55

Current to Voltage Converter:

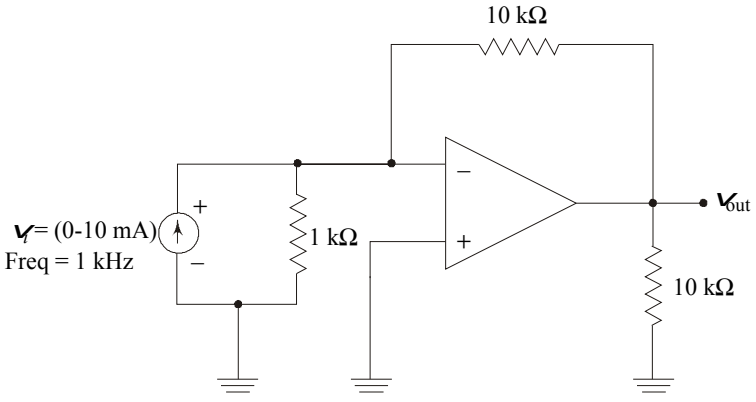


Fig. 4.56

Procedure:

Voltage to Current Converter:

1. Connect the circuit as per the circuit diagram.
2. Set the AC input to any desired value.
3. Switch on the dual power supply and note down the reading from an ammeter.
4. Repeat the above procedure for variation input voltages.
5. Tabulate the readings in the given tabular column.

Current to Voltage Converter:

1. Connect the circuit as per the circuit diagram.
2. Connect the DC bulb to a regulated power supply and give a DC voltage less than 6 V to it.
3. Focus the DC bulb on the photo-diode, which is connected to the non-inverting terminal of an op-amp.
4. Switch on the dual power supply and note down the voltage at the output.
5. Vary the regulated power supply voltage that would vary the intensity of the bulb.
6. Measure the diode current and the corresponding output voltage.
7. Tabulate the readings in the given tabular column.

Tabulation:

Voltage to Current Converter:

Voltage (Volts)	Current (μ A)

Current to Voltage Converter:

Current (μ A)	Voltage (Volts)

Result:

The operation of the current to voltage and voltage to current are thus studied.

Exercises:

1. Discuss the different types of V-I converter.
2. Explain the operation of a I-V converter. When we use IC 741, what is the maximum value of current that can be measured?

4.4.7 Active Filters Using Op-Amp

A frequency selective electric circuit that passes electric signals of specified band of frequencies and attenuates the signal of frequencies outside the band is called an electric filter. At low frequencies, passive filters have certain problems due to the inductors. This is overcome in an active filter where an op-amp and a RC network are used. Since an op-amp is used, the circuit offers high Z_{in} and low Z_{out}. Due to high Z_{in} of op-amp, large value resistors can be used, thereby reducing the value of the capacitors. The operation of the active filters is limited in the high frequency by the gain bandwidth product and slew rate of the op-amp.

The filters are classified as given below. Depending on the number of capacitors, we have first order, second order and higher order filters. Depending on the characteristics exhibited, we have low pass filter (LPF), high pass filter (HPF), band pass filter (BPF) and band elimination filter (BEF). Depending on the type of the circuit used, we have VCVS filters, infinite gain multiple feedback filters and infinite gain-state variable feedback filter. Depending on the method of design, we have Butterworth filter, Chebyshev filter, Bessel filter, etc.

Characteristics of an Ideal Filter

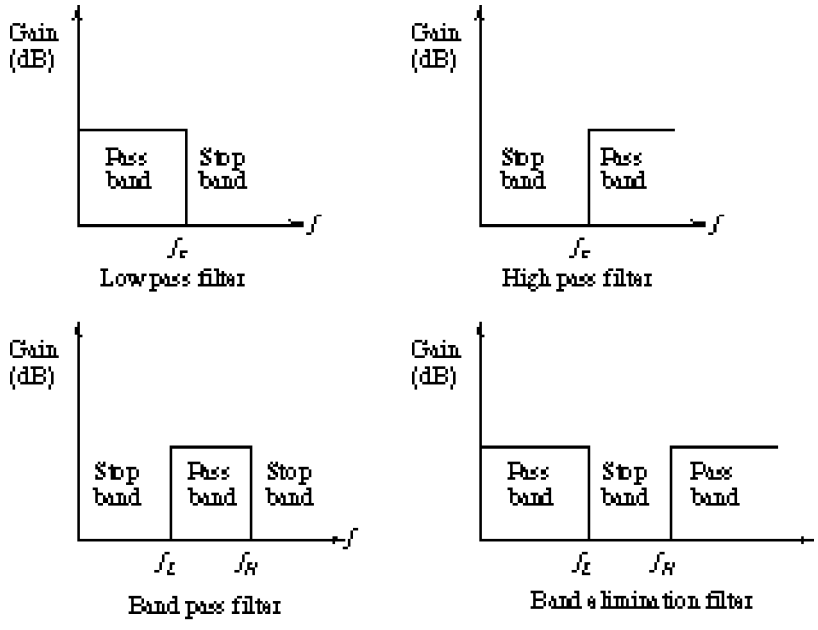


Fig. 4.57

The Cut-Off Characteristics for Different Orders (Butterworth LPF)

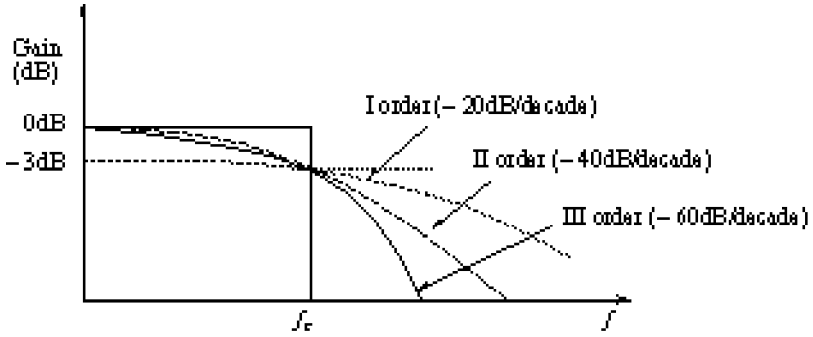


Fig. 4.58

The cut-off characteristic of a filter is improved as the order of the filter increases.

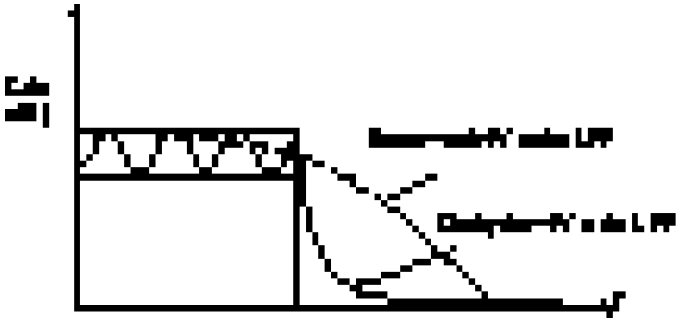


Fig. 4.59

From the figure, it is evident that a cut-off characteristic of a Chebyshev filter is better than that of a Butterworth filter. Butterworth filters are known as *maximally flat type* filter, as its pass band response is almost flat. The Chebyshev filters are known as *equal ripple filter* and they exhibit gain maxima and minima in the pass band. This gain ripple is a disadvantage of Chebyshev filter. Both these filters have got another disadvantage, i.e., they exhibit maximum phase shift at the cut-off frequency. Another filter called *Bessel filter* exhibits minimum phase shift at the cut-off frequency and is known as minimal phase shift filter. But its cut-off characteristic is not sharp.

Experiment (Study of Active Filters Using Op-Amp)

Aim: ***To Design and Test a 2nd Order Low Pass Filter and High Pass Filter Using IC 741***

Equipment Required:

Equipment	Range	Quantity
Dual power supply	(15-0-15) V	1
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1

Circuit Diagram:

Low Pass Filter:

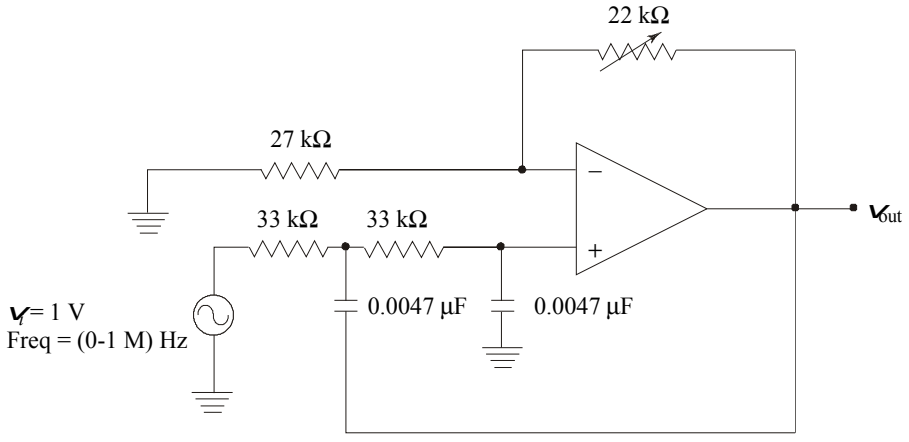


Fig. 4.60

High Pass Filter:

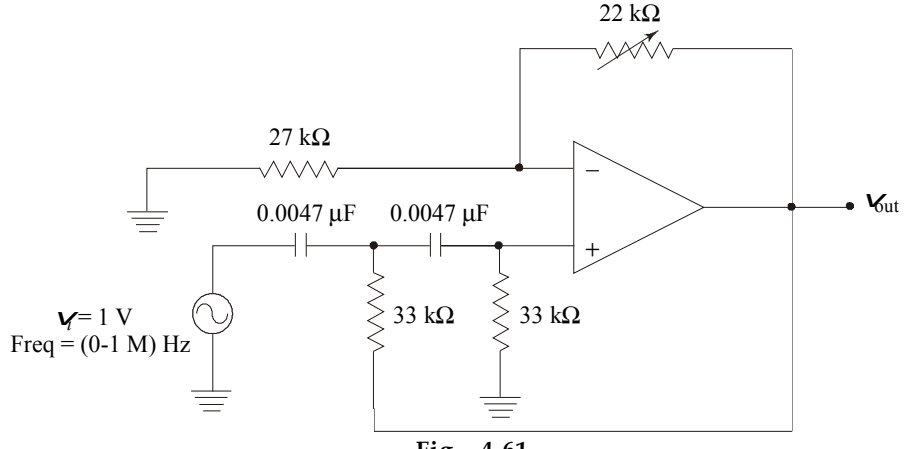


Fig. 4.61

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Give a sinusoidal input of say 2 V_{pp}.
3. Adjust the potentiometer such that R_f = 15.8 kW.
4. Switch on the dual power supply.
5. Vary the input frequency at regular intervals and note down the output response from the CRO.
6. Verify the practical and the calculated theoretical cut-off frequency.
7. Plot the frequency response on a semilog sheet.
8. Repeat the above procedure for the high-pass filter.

Design:

Low Pass Filter:

Given f_H = 1 kHz.

We know that, $f_H = \dfrac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$

Let, $R_1 = R_2 = R$

$C_1 = C_2 = C$

Therefore, $f_H = \dfrac{1}{2\pi\sqrt{RC}}$

Choose, $C = 0.0047\ \mu\text{F}$

Therefore, $R = \dfrac{1}{2\pi f_H C} = 1/2\ \pi \times 10^3 \times 0.0047 \times 10^{-6} = 33.86\ \text{k}\Omega$

Choose a standard value of 33 kΩ.

Let the pass band voltage gain be 1.586.

$$1 + \frac{R_f}{R_1} = 1.586$$

Therefore, $R_f = 0.586\ R_1$

Choose, $R_1 = 27\ \text{k}\Omega$

$R_f = 0.586 \times 27\ \text{k}\Omega = 15.82\ \text{k}\Omega$

Use a standard value of 22 kΩ

High Pass Filter:

Given, $f_l = 1$ kHz

Proceeding in the same way $R = 33$ kΩ and $R_f = 15.82$ kΩ.

Use the standard value of 22 kΩ as a potentiometer.

Model Graphs:

Low Pass Filter:

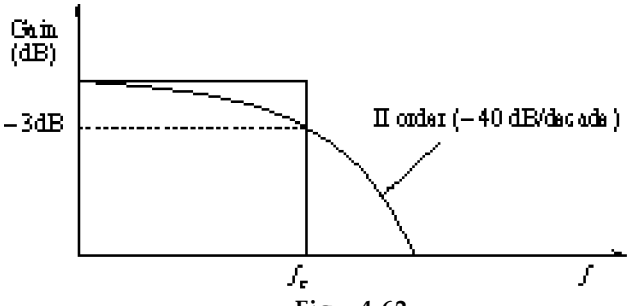


Fig. 4.62

High Pass Filter:

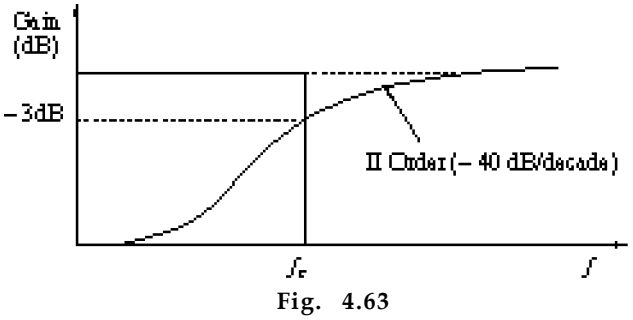


Fig. 4.63

Result:

The frequency response of the ACTIVE LPF AND HPF are studied and the cut-off frequencies are calculated and verified.

Exercises:

1. Why are Active filters preferred over passive filter?
2. Define the 3-dB cut-off frequency of a filter.
3. What is a notch filter? Explain its response.

4.4.8 Digital to Analog Converter

Analog signal is a smooth, but continuous time varying signal. It is not possible to study such a change in signals. In order to study the signal, we require discrete samples of the signal at different instances of time, i.e., we require a digitized signal or digital signal. Digital signal is therefore a discrete signal. Discrete signal obtained for the purpose of analysis must be converted back again into the original analog signal after the analysis of the signal. Thus, we require *Analog to Digital Converter (ADC)* and *Digital to Analog Converter (DAC)*.

The input to a DAC is a digital signal. A digital signal is a sequence of 1's and 0's. Each bit is positionaly weighed in a digital port or signal. A digital port in electronics can be of *N* bit length.

Consider a digital code of 4-bit length. It can be represented by a sequence of *b*'s as given below. When we convert the code into decimal, we follow the following rule,

$$\underset{\text{MSB}}{b_3,} \quad b_2, \quad b_1, \quad \underset{\text{LSB}}{b_0}$$

Decimal equivalent of binary code,

$$b_3 \times 2^3 + b_2 \times 2^2 + b_1 \times 2^1 + b_0 \times 2^0$$

The expression tells us that the positional weight of b_3 is 8 and that of the b_2 is 4 and that of the b_1 is 2 and that of b_0 is 1. By applying the positional weighing principle, we can convert a bit into a corresponding analog voltage [DAC is based on positional weighing principle].

'1' means presence of a particular condition (+ 5 V) and '0' means absence of a particular condition (V). Using the positional weighing principle explained above, two types of DACs are constructed.

1. Binary weighed resistor DAC.
2. *R*-2*R* ladder network type DAC.

4.4.8.1 Binary Weighed Resistor DAC It makes use of a summing amplifier using op-amp. Let us construct a DAC for 4-bit as shown in the figure.

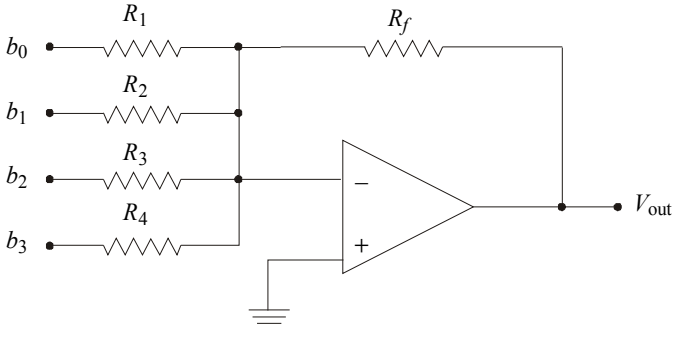


Fig. 4.64

$$V_0 = -\frac{R_f}{R_1} b_0 - \frac{R_f}{R_2} b_1 - \frac{R_f}{R_3} b_2 - \frac{R_f}{R_4} b_3$$

$$V_0 = -\frac{R_f}{R} b_0 - \frac{R_f}{R/2} b_1 - \frac{R_f}{R/4} b_2 - \frac{R_f}{R/8} b_3$$

If, $R_f = 1\ \text{k}\Omega$ and $R = 10\ \text{k}\Omega$, then

$$V_0 = -\frac{1}{16} [b_0 + 2b_1 + 4b_2 + 8b_3]$$

Disadvantage When there are N bits in the digital codes, there is a requirement of N number of binary weighed resistors from R to $\frac{R}{2^{n-1}}$

4.4.8.2 R-2R Ladder Network DAC

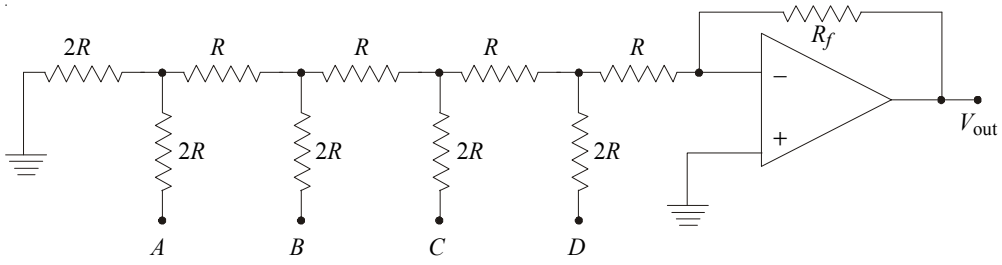


Fig. 4.65

It uses op-amp in the inverting mode. Let us assume that the op-amp is ideal. From the figure, it is evident that the DAC requires a large number of resistors. Although it is a disadvantage, *R-2R ladder network* is preferred to *Binary-weighed DAC*. the inverting terminal is at the virtual ground potential.

Experiment (Digital to Analog Converter)

Aim: ***To Study the Operation of DAC using IC 741***

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1
Dual power supply	(12-0-12) V	1

Circuit Diagram:

4-Bit Binary Weighed Resistor DAC:

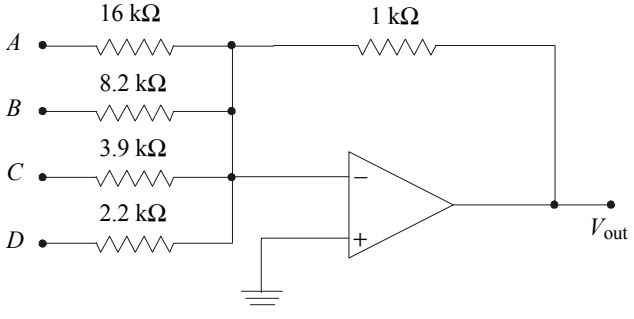


Fig. 4.66

R-2*R* Ladder Network DAC:

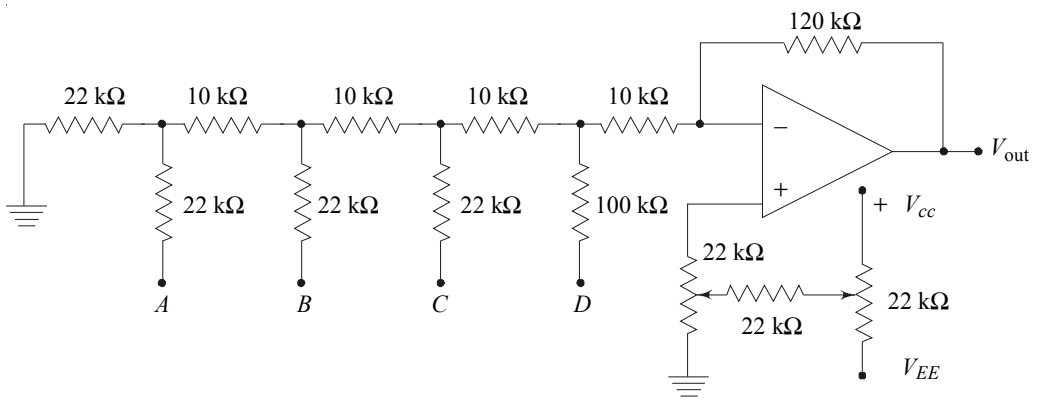


Fig. 4.67

Procedure:

1. Connect the circuit as per the circuit diagram.
2. With all input shorted to ground, adjust the 22 kΩ potentiometer till the output is zero. This nullifies the offset voltage at the input of the op-amp.
3. Give the binary from (0000–1111) and measure the output using a multimeter.
4. Repeat the above procedure for the 4-bit weighed-resistor DAC circuit, leaving step 2.

Model graph:

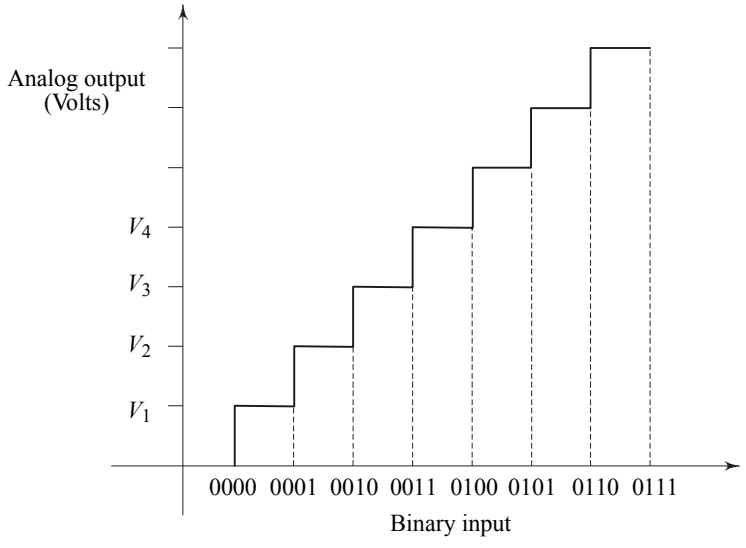


Fig. 4.67(a)

Exercises:

1. Classify DACs on the basis of their output.
2. Why is an inverted *R*-2*R* ladder network DAC better than *R*-2*R* ladder DAC?
3. Describe the various types of electronic switches used in DAC.
4. Study DAC using IC 1408.

Experiment (Study of Digital to Analog Converter)

Aim: ***To Study the Working of a DAC Using IC 0808***

Experiment Required:

Equipment	Quantity
Digital IC trainer kit	1
Digital multimeter	1
CRO	1

Circuit Diagram:

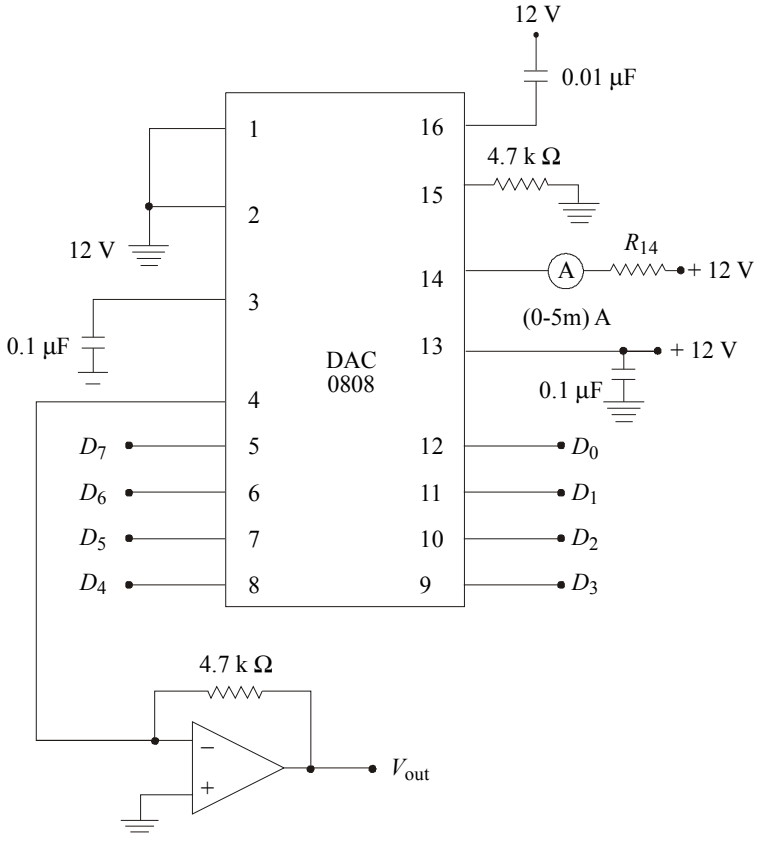


Fig. 4.67(b)

Design:

$$I_0 = (D_{n-1} + 2^{-1} D_{n-2} + \cdots 2^{n-1} D_0) \times \frac{I_{REF}}{2};\ V_0 = I_0 R_{14} \qquad \text{(where, } R_{14} = 4.7 \text{ k}\Omega\text{)}$$

Procedure:

1. Connections are made as per the circuit diagram and pin configuration of the ICs.
2. The digital inputs are given.
3. The resistor R_{14} is adjusted to get a reference current of 2 mA.
4. Measure the output using a multimeter for all the combinations of the digital inputs.

Tabulation:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	V_0 (Volts)	Theoretical value of V_0 (Volts)
1	1	1	1	1	1	1	1		
1	1	1	1	1	1	1	0		
1	1	1	1	1	1	0	0		
1	1	1	1	1	0	0	0		
1	1	1	1	0	0	0	0		
1	1	1	0	0	0	0	0		
1	1	0	0	0	0	0	0		
1	0	0	0	0	0	0	0		
0	1	0	0	0	0	0	0		
0	0	1	0	0	0	0	0		
0	0	0	1	0	0	0	0		
0	0	0	0	1	0	0	0		
0	0	0	0	0	1	0	0		
0	0	0	0	0	0	1	0		
0	0	0	0	0	0	0	1		
0	0	0	0	0	0	0	0		

Result:

The working of a DAC using IC 0808 was studied.

Exercises:

1. Discuss the factors involved in designing a good DAC.
2. Compare the merits and demerits of the different types of DAC.

4.4.9 Analog to Digital Converter

There are many methods of analog to digital conversion. They are:

1. Ramp conversion.
2. Dual slope integration.
3. Successive approximation.
4. Parallel conversion.
5. Parallel/serial conversion.

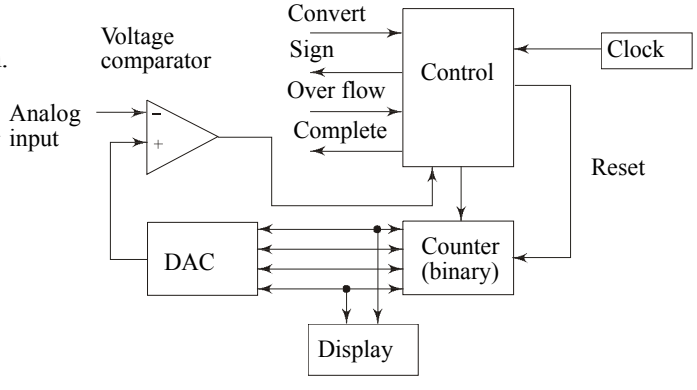


Fig. 4.68

Ramp Conversion

It is the least expensive and simplest of all ADC. But it is the slowest and highly susceptible to noise.

When the control unit receives CONVERT signal, it starts converting analog signal to digital. First of all, it resets the counter to 000···0 and then it supplies clock pulses to the counter. At every clock pulse, the counter counts increase by 1. The output of the counter, which is a binary number, is converted into equivalent analog voltage by a DAC and the DAC output feeds a voltage comparator. The voltage comparator waits till the analog input equal DAC output. When the analog input equals DAC output, the comparator signals the control

unit. The control unit stops supplying clock pulses to the counter and it indicates the completion of the operation through *Complete* channel. The counter output is displayed as the digital equivalent of analog input. The sign of the output is indicated through a channel called *Sign*. If the value of the analog input is beyond the maximum permissible voltage range of the DAC, then it is indicated by the control unit to the operator through a channel called *Overflow*.

This is most suited for application like Digital voltmeter, Digital multimeter, etc., as conversion rate require/unit time is minimal.

Dual-Slope Integrated ADC

It overcomes the disadvantages of counter ramp ADC.

1. It is a low cost device.
2. Conversion rate is high.
3. Good noise immunity.

The heart of the circuit is an op-amp integrator. The operations are controlled by a control unit (dual slope ADC is assumed to be an open loop system where as counter ramp ADC is a closed loop system).

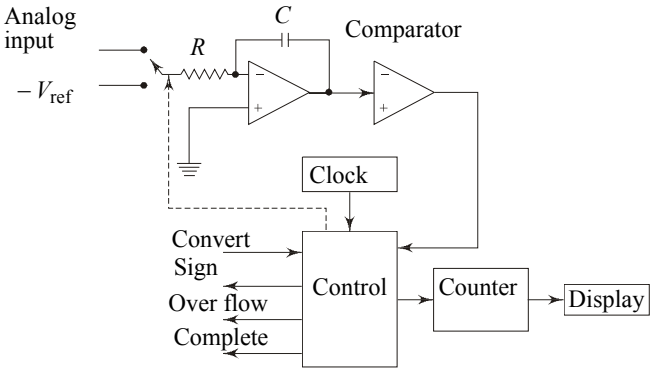


Fig. 4.69

Upon receipt of convert signal, the control unit switches analog input as the input to the integrator. At the same time, it resets the control and the integrator starts integrating analog input. The integration is done for a specific period of time as decided by the control unit. During the integration period, no clock pulse is applied to the counter and at the end of the integration period, the control unit supplies clock to the counter and the counter counts. At the end of the integration period, control changes the switch position from analog input to $-V_{ref}$ (reference voltage). Now $-V_{ref}$ is integrated giving –ve going ramp, ultimately crossing zero voltage line. When the zero crossing is detected by the zero crossing detector, the control stops supplying particular instant of time which is displayed as the digital equivalent of the analog input.

Successive Approximation ADC: (Serial)

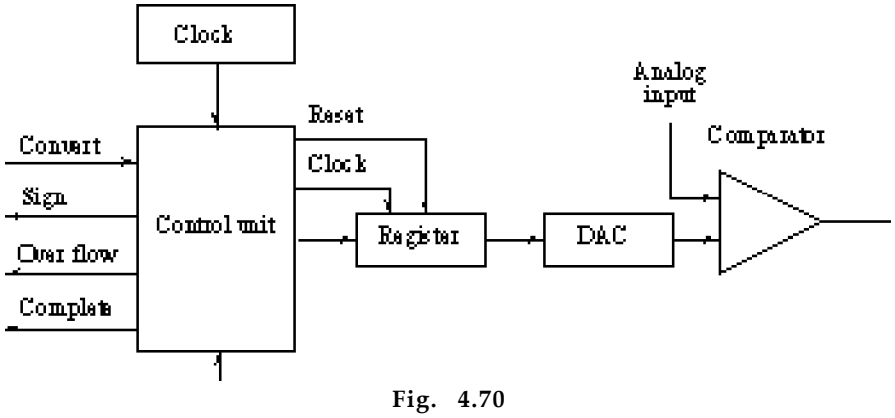


Fig. 4.70

It is very fast and less expensive when compared with parallel converter. It consists of a programmer, which sets a '1' in MSB position and resets all other bits. The digital number so

obtained is converted to analog and is compared with the actual analog signal input. If the DAC output is larger than the actual analog input, then '1' is removed from MSB and it is tried in next MSB. If the DAC output becomes less than the analog signal input, then '1' is tried in the remaining bit positions also. In this way, '1' is tried in each and every bit position of the code until digital equivalent of the actual analog input signal is obtained.

It requires N clock periods to give the right answer under the worst case, whereas a counter ramp ADC requires 2^N number of clock periods to give the correct answer under the worst case.

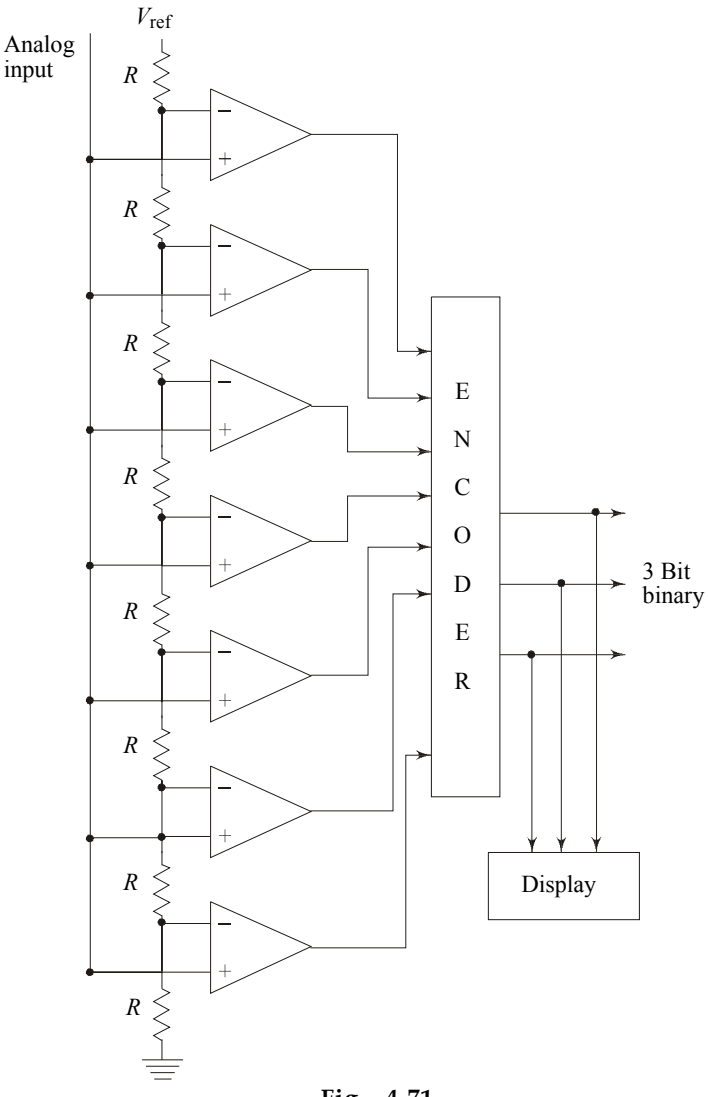


Fig. 4.71

Parallel Conversion It is best suited for high-speed conversion. It is the fastest of all ADCs. But it is very expensive. For N-bit digital signal, the converter requires 2^N–1 number of comparators.

It makes use of 2^3–1 = 7 comparators. The encoder provides 3-bit binary output equivalent of analog input.

Parallel / Serial ADC Combining the advantages of parallel and successive approximation ADC, we have the parallel/serial converter. It is used in high-speed applications. It is less expensive than parallel converter. The circuit given above is for 3-bit digital signal. Therefore, it makes use of 7 comparator. The encoder provides binary output. The control unit switches either V_{ref} or the DAC output to the resistive divider string and current control.

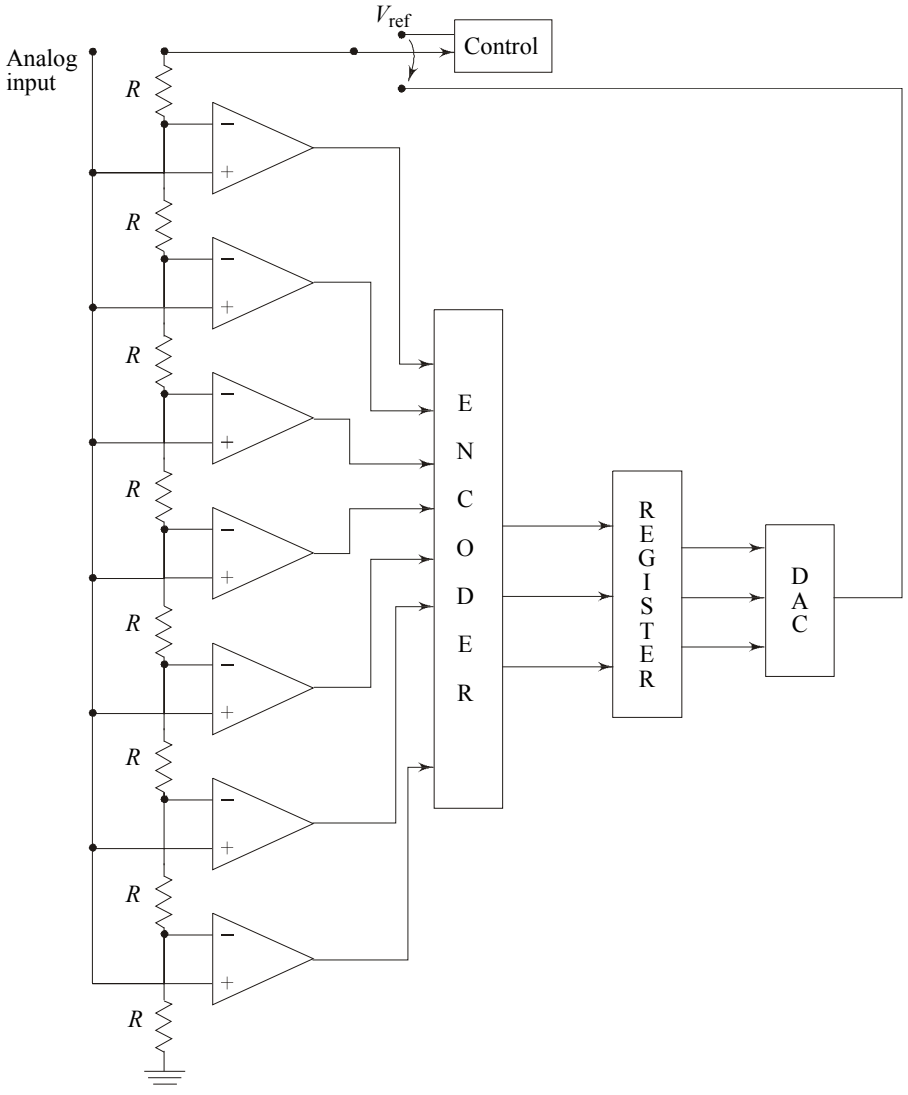


Fig. 4.72

Experiment (Study of Analog to Digital Converter)

Aim: ***To Study the Working of ADC.***

1. Counter type ADC.
2. Single slop ADC.

Equipment Required:

Equipment	Quantity
Digital IC trainer kit	1
Digital multimeter	1
CRO	1

Circuit Diagram:

Counter type ADC:

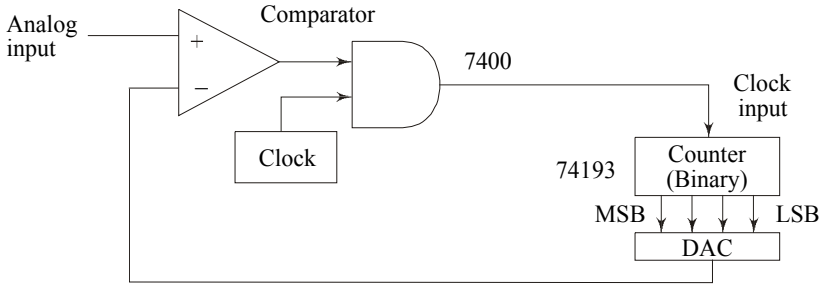


Fig. 4.73

Single Slope ADC:

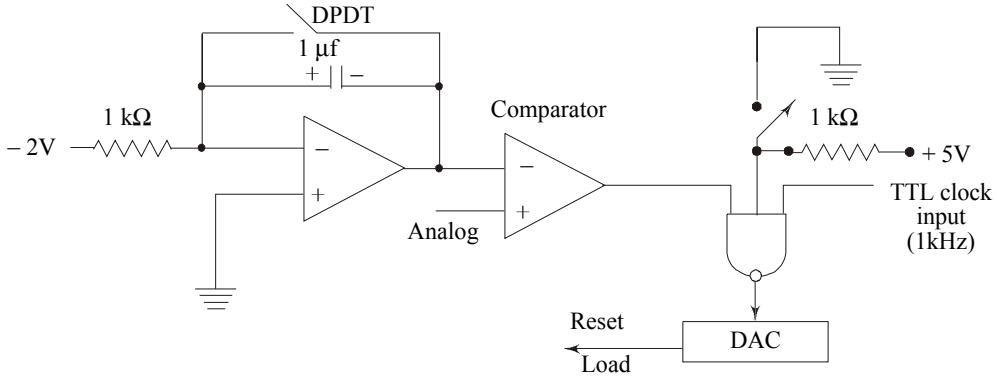


Fig. 4.74

Procedure:

1. Connections are made as per the circuit diagram and pin configuration of the *ICs*.
2. The analog input is given.
3. Note down the reading from the counter.

Tabular Column:

Analog Input	D	C	B	A

Experiment (Study of Analog to Digital Converter)

Aim: ***To Study the Working of Flash ADC.***

Equipment Required:

Equipment required	Range	Quantity
DC power supply	(12–0–12) V	1
Signal generator	(0–1 M) Hz	1
DC power supply	(0–30) V	1

Circuit Diagram:

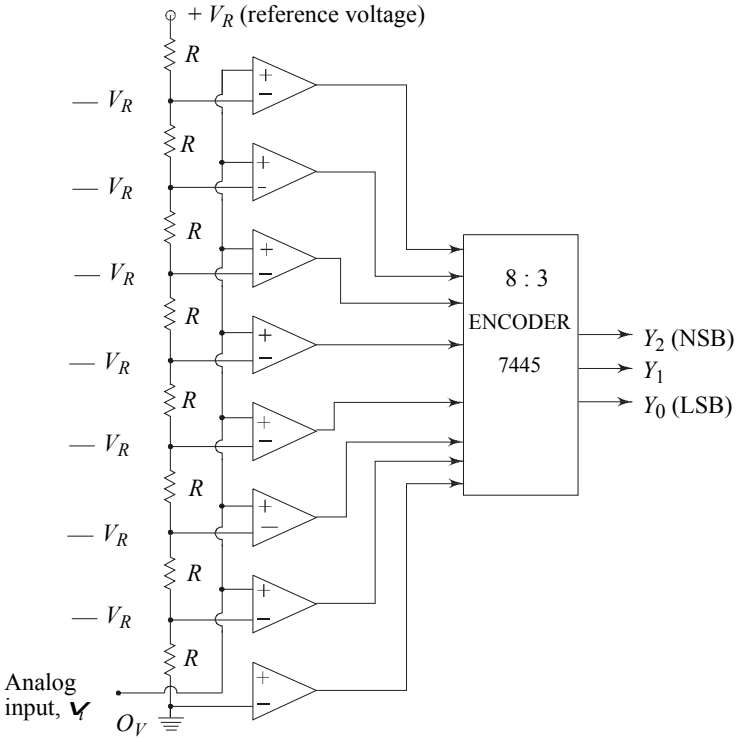


Fig. 4.74 (a)

Procedure

1. Connect the circuit as per the circuit diagram.
2. Set the reference voltage (V_R) to the required maximum voltage.
3. Increase the analog input (dc power supply) slowly, note down the corresponding digital equivalent.

Logical Table:

Input Voltage (V_i)	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
$0 - \frac{1}{8} V_R$	0	0	0	0	0	0	0	1	0	0	0
$\frac{1}{8} V_R - \frac{2}{8} V_R$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2}{8} V_R - \frac{3}{8} V_R$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3}{8} V_R - \frac{4}{8} V_R$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4}{8} V_R - \frac{5}{8} V_R$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5}{8} V_R - \frac{6}{8} V_R$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6}{8} V_R - \frac{7}{8} V_R$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7}{8} V_R - V_R$	1	1	1	1	1	1	1	1	1	1	1

4.5 555 TIMER APPLICATIONS

555 Timer as Astable Multivibrator

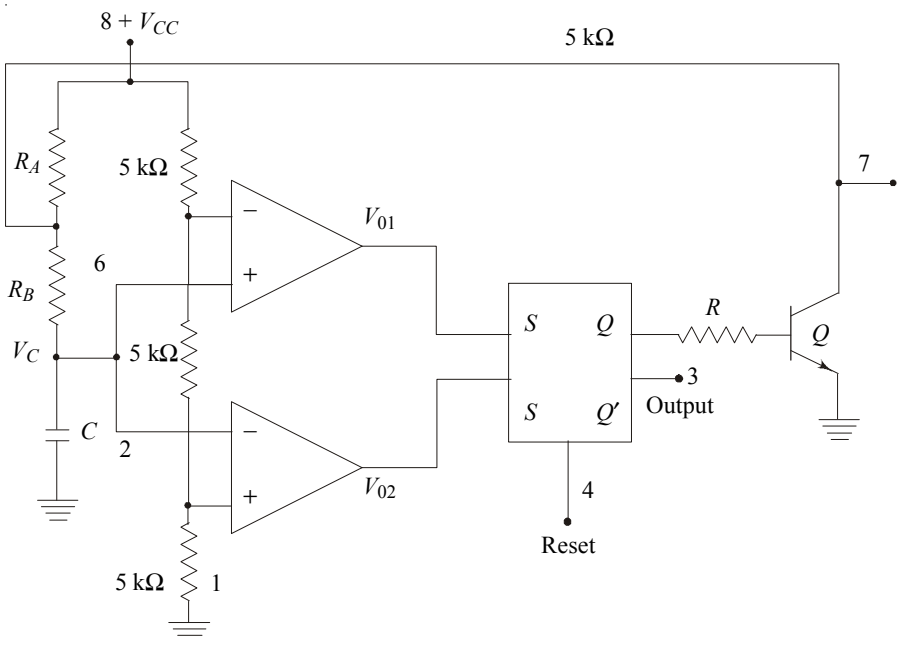


Fig. 4.75

When $V_C = 0$, V_{01} = '0' and V_{02} = '1' i.e., $S = 0$ and $R = 1$. Therefore Q is reset to '0' and output is therefore '1'. (Output is $\overline{Q}$). Therefore, the transistor is cut-off and hence capacitor, C is charged by V_{CC} through $(R_A + R_B)$. When V_i becomes slightly greater than $V_{CC}/3$, V_{01} = '0' and V_{02} = '1' i.e., $S = 0$ and $R = 0$. This does not change the condition and hence charging of capacitor, C continues. When V_C becomes slighter than $2V_{CC}/3$, V_{01} = '1' and V_{02} = '0' i.e., $S = 1$ and $R = 0$. This sets the Q output to 1 and $\overline{Q} = 0$. Now transistor enters saturation and capacitor, C discharges to ground through the transistor via R_B. [This charging time constant is $(R_A + R_B)C$ and discharging time constant is R_BC]. Now V_C discharges or decreases, when it becomes less than $2V_{CC}/3$ (but greater than $V_{CC}/3$). V_{01} = '0' and V_{02} = '1' i.e., $S = 0$ and $R = 0$. Then there is no charge at the output and capacitor, C continues to discharge.

When the V_C falls below $V_{CC}/3$, V_{01} = '0' and V_{02} = '1' i.e., $S = 0$ and $R = 1$. This resets Q and the transistor is now turned off. Hence capacitor is again charged. Thus cycle repeats. Output toggles every time when $V_C > 2V_{CC}/3$ or when $V_C < 2V_{CC}/3$.

Capacitor voltage,

$$V_C(t) = V_f - (V_f - V_{\text{in}})\, e^{-\frac{t}{T}}$$

where, V_f = final voltage

V_{in} = initial voltage

T = time constant

During charging, the capacitor voltage is given by,

$$V_C(t) = V_{CC} - (V_{CC} - V_{CC}/3)\, e^{-\frac{t}{(R_a + R_B)C}}$$

At $t = t_{ON}$, when $V_C(t) = 2V_{CC}/3$, above equation reduce to

$$T_{ON} = 0.693(R_A + R_B)C$$

During discharging, the capacitor voltage is given by,

$$V_C(t) = 0 - (0 - 2V_{CC}/3)\, e^{-\frac{t}{(R_B)C}}$$

At $t = t_{OFF}$, when $V_C(t) = V_{CC}/3$, above equation reduce to

$$T_{OFF} = 0.693(R_B)C$$

Total time, $T = t_{ON} + t_{OFF}$

$$T = 0.693(R_A + 2R_B)C$$

Therefore, frequency, $f = 1/T = \dfrac{1{\cdot}44}{(R_A + R_B)C}$

Duty cycle, $T_D = (t_{ON}/T)100\%$

$$T_D = \frac{R_A + R_B}{(R_A + 2R_B)} \times 100\%$$

555 Timer as Monostable Multivibrator

Operation

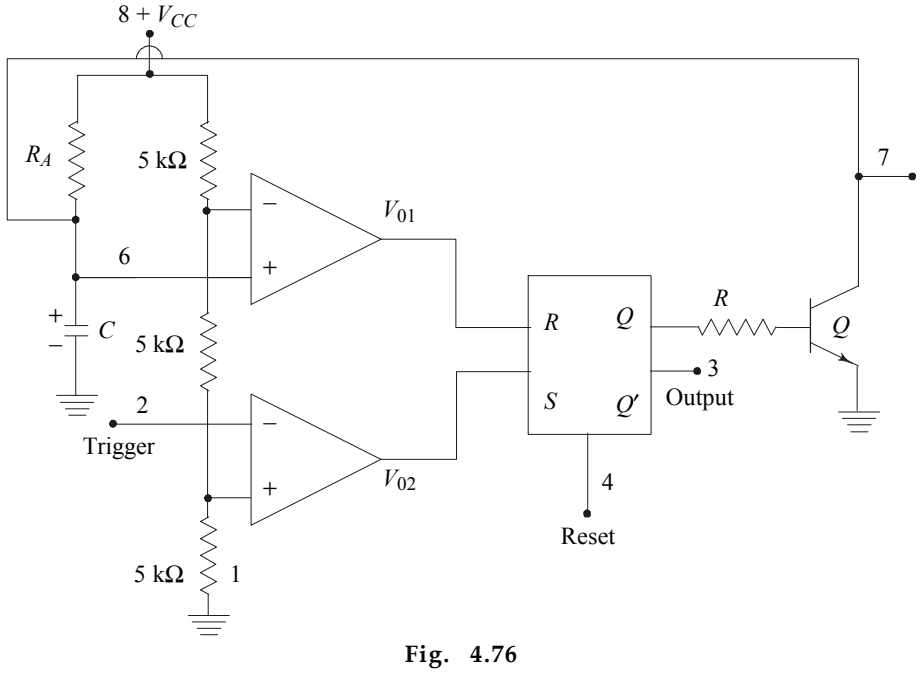


Fig. 4.76

Trigger is a negative going pulse (it is a narrow pulse with a quiescent value $+V_{CC}$). Initially, the capacitor is uncharged. When the trigger voltage falls below $V_{CC}/3$, the output of comparator 2 is '1' and the output of comparator 2 is '0'. This causes $S = 0$, $R = 1$, input condition for the flip-flop. Its output, $Q = 0$, $\overline{Q} = 1$. Now, the transistor is cut-off and hence there is no path for the capacitor to discharge and the supply voltage ($+ V_{CC}$) now charge capacitor. The negative trigger pulse now goes 'high' and hence output of comparator 2 is '0'. As long as comparator 2 is less than $2\frac{V_{CC}}{3}$, the output of comparator 1 is '0'. This condition ($S = 0$; $R = 0$) does not change the output. Hence $Q = 0$, $\overline{Q} = 1$ and transistor is cut-off.

When the capacitor voltage exceeds $2V_{CC}/3$, then the output of comparator 1 is '1'. The output of comparator 2 is anyway '0'. And hence $S = 1$; $R = 0$. This sets the $Q = 0$ and $\overline{Q} = 0$. Now transistor enters saturation and capacitor starts discharging through the transistor. Thus capacitor voltage becomes less than $2V_{CC}/3$ and ultimately becomes '0'. This results in $S = 0$ and $R = 0$. This maintains $Q = 1$ and $\overline{Q} = 0$.

When the trigger goes low, $S = 0$ and $R = 1$, $Q = 0$ and $\overline{Q} = 1$, i.e., cycle repeats.

Capacitor voltage is given by,

$$V_C(t) = V_{CC} - (V_{CC} - 0)\, e^{-t/RC}$$

When $V_C(t) = 2\,\frac{V_{CC}}{3}$, $t = t_p$, the output pulse terminates.

Therefore, $t_p = 1.1$ RC

For noise filtering control (pin 5) is connected to ground via a capacitor 0.01μf.

Experiment (Study of Application 555 Timer)

Aim: ***To Design and Test the Following Circuit Using IC 555***

1. Astable multivibrator
2. Monostable multivibrator
3. Voltage to frequency converter (voltage controlled oscillator).
4. Schmitt trigger

Equipment Required:

Equipment	Range	Quantity
Regulated power supply	(0-5) V	1
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1

Circuit Diagram:

Astable Multivibrator:

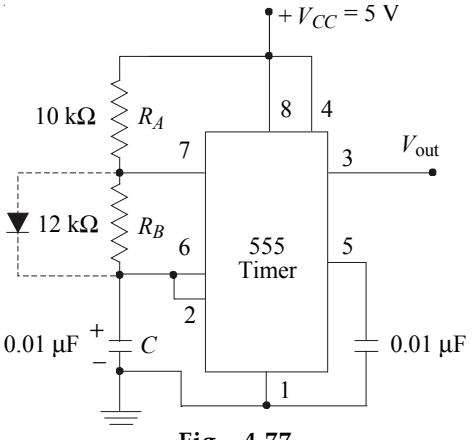


Fig. 4.77

Monostable Multivibrator:

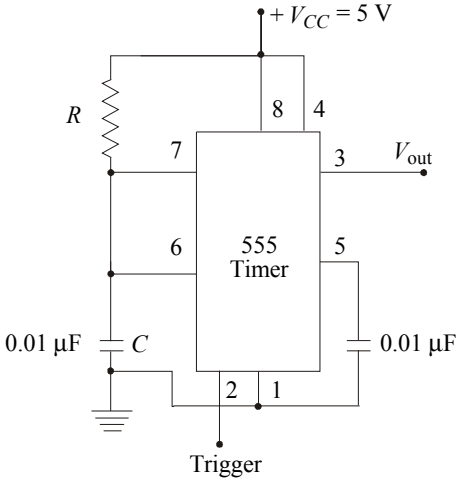


Fig. 4.78

Trigger should be either a square wave or a differentiated square wave. Differentiated square wave is preferred over square wave as it reduces the power consumption.

Voltage to Frequency Converter (VCO):

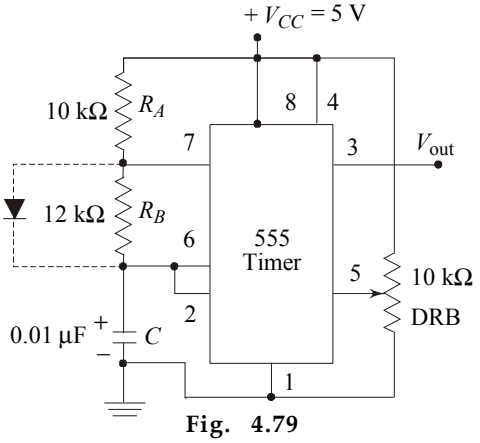


Fig. 4.79

Schmitt trigger:

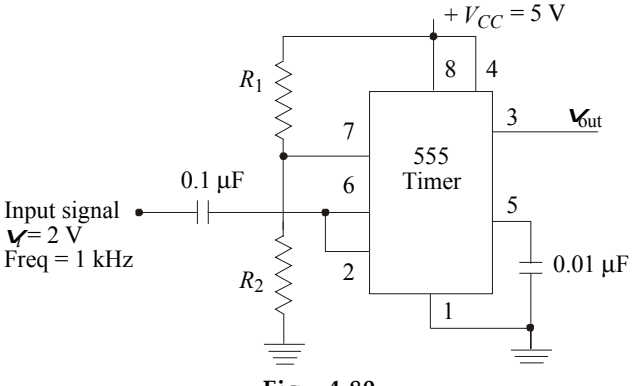


Fig. 4.80

Procedure:

Astable Multivibrator:

1. Connect the circuit as per the circuit diagram.
2. Switch on the supply and note down the output waveform at pin No 3 from the CRO.
3. Draw the output waveform on a graph sheet.
4. Verify the theoretical and practical time periods.
5. The theoretical time period is given by,

$$t_p = 0.693\ (\ R_A + R_B\ )\ C$$

Monostable Multivibrator:

1. Connect the circuit as per the circuit diagram.
2. Give a square wave input as a trigger to pin No. 2.
3. Switch on the power supply.
4. Note down the output waveform at pin No. 3.
5. Calculate the ON and OFF time periods and verify with the theoretical values.
6. 1.1 RC gives theoretical time period.
7. Repeat the above procedure for different values of R.

Voltage to Frequency Converter (Voltage Controlled Oscillator):

1. Connect the circuit as per the circuit diagram.
2. Set the input voltage at + 5 V.
3. Note down the output waveform at pin No. 3 for various voltages at pin No. 5.
4. Determine the frequency of the output waveform and verify with the theoretical value.
5. Repeat the above procedure for different voltages.

Schmitt Trigger:

1. Connect the circuit as per the circuit diagram.
2. Give a sine wave input as a trigger to pin No. 2.
3. Switch on the power supply.
4. Note down the output waveform at pin No. 3.
5. Calculate the ON and OFF time periods and verify with the theoretical values.

Design:

$$t_p = 1.1\ \text{RC}$$

Let C be chosen to be 0.01μ F

If the t_p is designed for a value of 0.11 msec, then

$$R = \frac{t_p}{1{\cdot}1C} = 0.11 \times 10^{-3}/1.1 \times 0.01 \times 10^{-6} = 10\ \text{k}\Omega$$

Therefore, the design values for t_p = 0.11 msec are C = 0.01 μF and R = 10 kΩ

Voltage to Frequency Converter:

Given, f = 4 kHz

Duty cycle = 65%

C = 0.01 μF

Total time period $= T_{\text{on}} + T_{\text{off}} = \dfrac{1}{f} = 2.5 \times 10^{-4}$ Second

$$\text{Duty cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} = 0.65$$

Therefore, $T_{on} = 0.65\ (T_{on} + T_{off})$

$= 0.65\ (2.5 \times 10^{-4}) = 1.625 \times 10^{-4}$ sec

$T_{off} = T - T_{on} = (2.5 - 1.635)\ 10^{-4}$ sec $= 0.875 \times 10^{-4}$ sec

We know that, $T_{off} = 0.693\ R_2C$

$$R_2 = \frac{T_{OFF}}{0.693C} = 0.875 \times 10^{-4} / (0.693 \times 0.01 \times 10^{-6}) = 12.63\ \text{k}\Omega$$

Choose $R_2 = 12\ \text{k}\Omega$; $R_1 = 10\ \text{k}\Omega$

Tabular Column:

Voltage at Pin 5 (Volts)	T_{on} (μ sec)	T_{off} (μ sec)	$T = T_{on} + T_{off}$ (μ sec)	Frequency $f = 1/T$ (kHz)

Exercises:

1. Draw the internal structure of a 555 timer and write a brief note on it.
2. Discuss some applications of timer in monostable mode.
3. What are the modes of operation of a timer?

4.6 PHASE LOCKED LOOP (PLL)

Principle of PLL

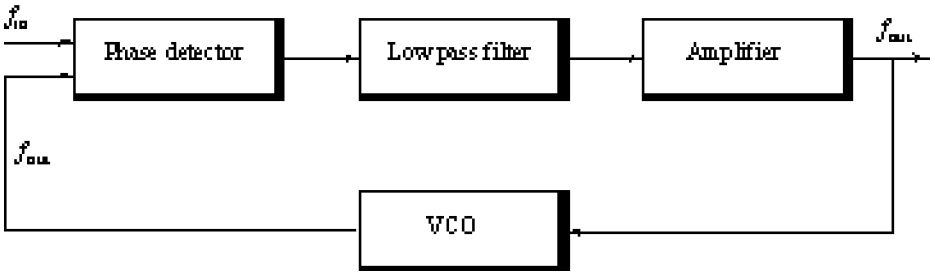


Fig. 4.80(a)

PLL has emerged as one of the fundamental building block in electronic technology. It is used for the frequency multiplication, FM stereo detector, FM demodulator, frequency shift keying decoders, local oscillator in TV and FM tuner.

The block diagram of a PLL is shown in the figure. It consists of a phase detector, a LPF, and a voltage controlled oscillator (VCO). The phase detector or comparator compares the input frequency, f_{in}, with feedback frequency, f_{out} (output frequency). The output of the phase

detector is proportional to the phase difference between, f_{in} and f_{out}. The output voltage of the phase detector is a DC voltage and therefore, is often refers to as error voltage. The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a DC level. The DC level, in-tern is the input to the VCO.

The output frequency of the VCO is directly proportional to the input DC level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequency. In short, PLL keeps its output frequency constant at the input frequency.

Thus, the PLL goes through 3 states,

1. Free running state.
2. Capture range/mode.
3. Phase lock state.

Before input is applied, the PLL is in the free running state. Once the input frequency is applied, the VCO frequency starts to change and the PLL is said to be the capture range/mode.

The VCO frequency continues to change (output frequency) until it equals the input frequency and the PLL is then in the phase locked state. When phase is locked, the loop tracks any change in the input frequency through its repetitive action.

IC Version of PLL Today, the PLL is even available as a single package, and examples are 560, 561, 562, 564, 565 and 567. These are all monolithic ICs. These differs mainly in operating frequency range, power supply requirements, etc.

Characteristics of 565 IC

1. Operating frequency: 0.001 Hz to 500 kHz.
2. Operating voltage: ± 6V to ± 12V.
3. Input level required for tracking: 10 mV (rms) to 3V(pp).
4. Input impedance: 10 kΩ (typical)
5. Output sink current: 1 mA (typical)
6. Output source current: 10 mA (typical).

Frequency Multiplication Using PLL

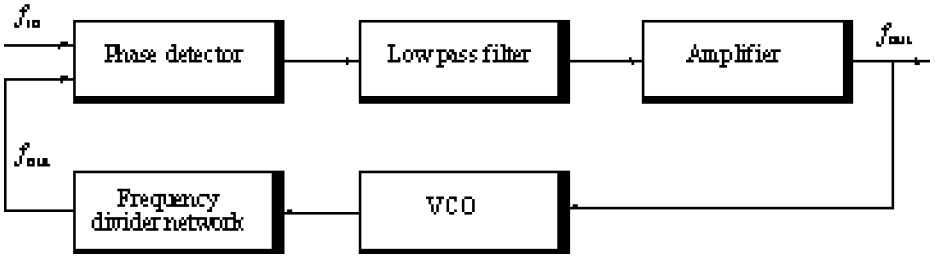


Fig. 4.81

The frequency divider is inserted between the VCO and the phase detector in the feedback path. Since the output of the divider is locked to the input frequency, f_{in}, the VCO is actually running at the multiple of the input frequency and hence the name multiplier. The divider-by-N network is a modulo-N (MOD-N) binary counter. A proper divide-by-N network can obtain the desired amount of multiplication. Where N is an integer.

Example: To obtain the output frequency, $f_{out} = 5\, f_{in}$, a divide-by-5 network is needed.

Relationship between F_{OUT}, F_L and F_C

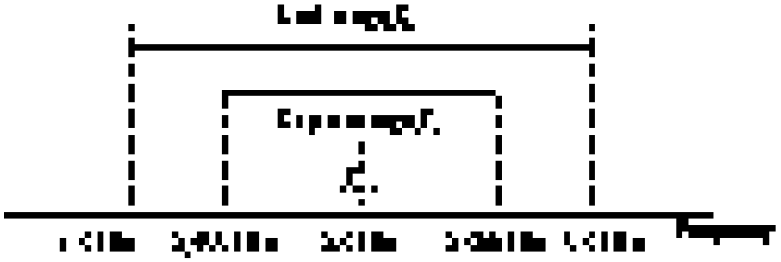


Fig. 4.82

Experiment (Phase Locked Loop)

Aim: ***Study of IC 565 PLL and Find the Following Paramenters***

1. Lock range
2. Capture range

Equipment Required:

Equipment	Range	Quantity
Signal generator	(0-1) MHz	1
CRO	(0-20) MHz	1
Dual Power supply	(12-0-12) V	1

Circuit Diagram:

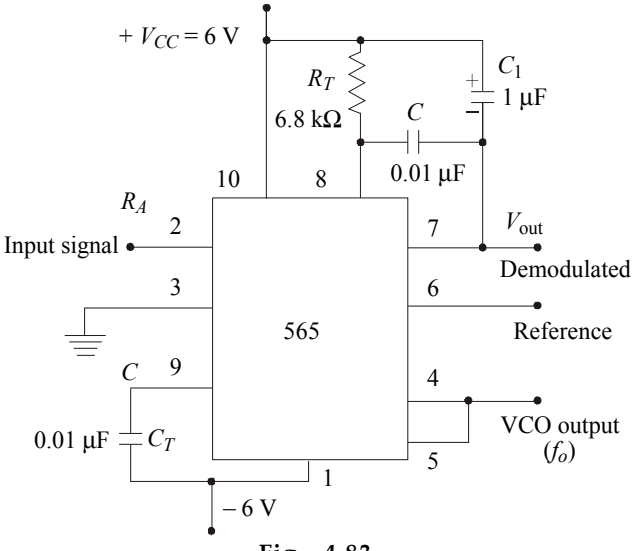


Fig. 4.83

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Measure the free running frequency of IC 565 at pin 4 using CRO with the input signal (say 0 V) from the signal generator OR shorting pin 2 to ground.
3. Set the input signal say 1 V, 1 kHz to pin 2 using signal generator and observe the waveform on the CRO.

4. The frequency varied till the output signal is 180° out of phase with input. This is the upper end of the lock range.
5. The frequency is reduced till the output is 90° output of phase with the input. This is the upper end of the capture range.
6. The frequency is varied till a 90° phase shift is obtained in the output with reference to the input once again. This is the lower end of locking range.
7. As the frequency is decreased further, output goes to 180° out of phase with the input once again. This is the lower end of the capture range.
8. The lock range, $\Delta f_L = (f_2 - f_4)$
   The capture range, $\Delta f_c = (f_3 - f_1)$
9. Compare these values with its theoretical value.

Result:

Parameter	Theoretical value	Practical value
Lock range	$\Delta f_L = \pm \frac{7.8\, f_0}{12}$	
Capture range	$\Delta f_C = \pm \sqrt{\frac{\Delta f_L}{2\pi \times 3.6 \times 10^3 \times C}}$	
Free running frequency	$f_0 = \frac{0.25}{R_T C_T}$	

OBJECTIVE QUESTIONS

1. What are the basic components of PLL?
2. List out the ideal characteristics of an op-amp.
3. List out the linear applications of an op-amp.
4. List out the non-linear applications of an op-amp.
5. Explain op-amp schmitt trigger.
6. Explain the following terms:
   (a) frequency compensation
   (b) slew-rate
   (c) off-set control
7. What are the limitations of monolithic IC technology?
8. What are the uses of PRBs generators?
9. Discuss about the various types of displays used in electronic industries.
10. What are the applications of VCO?
11. What are the four basic requirements of an instrumentation amplifier?
12. How is clipper circuit different from clamper?
13. What modification is required to convert triangular wave generator into a sawtooth one?
14. What is the resolution of an 8-bit DAC?
15. Draw a phasor comparator circuit using op-amp.
16. Explain the application of a comparator as a window detector.
17. How is multiplying of DC voltages done using op-amp?
18. Draw the schematic of a buffer amplifier using op-amp.
19. An integrator is _____ filter and differentiator is _____ filter.

20. How do you improve the fall-off rate of any filter?
21. What are the advantages of integrating types of ADC?
22. Draw the circuit of an op-amp based sample and hold circuit.
23. What are the applications of a schmitt trigger?
24. What is the main advantage of mono-stable multivibrator?
25. What is the main application of bi-stable multivibrator?
26. What is the main application of PLL?
27. What is the off-set voltage for μA 741 IC?
28. How do you compensate for the off-set in μA 741 IC?
29. Inductors cannot be integrated. Why?
30. What are the advantages of precision rectifiers?
31. What are the advantages of active filters over passive filters?
32. How do you design band pass filter and band elimination filter using low pass filter and high pass filter?
33. What is the main advantage in having sample and hold circuit along with ADC?
34. What are the parameters to be considered while selecting an ADC chip?
35. What are the advantages in instrumentation amplifier?
36. What is the main application of a buffer?
37. What is the main advantage in having a non-inverting amplifier over an inverting amplifier?

5 DIGITAL ELECTRONICS

Digital signal consists of only 2 values, '0' and '1'. These two values are logical, i.e., '1' represents the existence of a particular condition and '0' represents the absence of the condition.

5.1 BOOLEAN ALGEBRA

It is a technique of mathematical manipulation, using the 2 binary numbers, '0' and '1'. There are several laws in Boolean algebra and they are used in digital circuits.

Boolean Postulates

If $X = 0$, then

$\overline{X} = 1$

$0 \times 0 = 0$

$1 \times 1 = 1$

$1 + 1 = 1$

$1 \times 0 = 0 \times 1 = 0$

$1 + 0 = 0 + 1 = 1$

$\overline{1} = 0$ & $\overline{0} = 1$

Theorems of Boolean Algebra

Boolean algebra deals with logical relation between Boolean variables. A fundamental rule relating Boolean variables is called a *Boolean theorem*. The following are some of the Boolean theorems,

1. Commutative law:

$$X + Y = Y + X$$

Its dual, $X \times Y = Y \times X$

2. Associative law:

$(X + Y) + Z = X + (Y + Z)$

Its dual, $(X \times Y) \times Z = X \times (Y \times Z)$

3. Distributive law:

$X \times (Y + Z) = X \times Y + X \times Z$

Its dual, $X + (Y \times Z) = (X + Y) \times (X + Z)$

4. Negative law:
   Complement of $X = \overline{X}$
   $\overline{\overline{X}} = X$
5. Identity law:
   $X + X = X$
   Its dual, $X \times X = X$
6. Redundance law:
   $X + X \times Y = X$
   Its dual, $X \times (X + Y) = X$
7. $0 + X = X$
   Its dual, $1 \times X = X$
8. $1 + X = 1$
   Its dual, $0 \times X = 0$
9. $\overline{X} + X = 1$
   Its dual, $X \times \overline{X} = 0$
10. $X + \overline{X} \times Y = X + Y$
    Its dual, $X \times \overline{X} + Y = X \times Y$

D'morgan's Theorem

Statement: *The complement of a product is equal to sum of the complements and the complement of a sum is equal to product of the complements.*

$$\overline{X \times Y} = \overline{X} + \overline{Y}$$

$$\overline{X + Y} = \overline{X} \times \overline{Y}$$

They are duals of each other.

5.2 LOGICAL IC FAMILIES

Emitter Coupled Logic (ECL) IC

Operational Characteristic

1. Propagation delay: 4 ns
2. Fan out: 25
3. Power dissipation: 40 mW
4. Power delay product: 160 pJ
5. Z_{out} (1): 15 Ω
6. Z_{out}(0): 15 Ω
7. V_{out}(1): – 0.75 V
8. V_{out}(0): – 0.6 V
9. V_{EE}: – 5.2 V ±10%

Advantages

1. Highest operating speed.
2. Low Z_{out}.
3. High fan out.
4. Logically flexible:

(a) Have complementary outputs
(b) Wired output capability facility is flexible

5. High CMRR:
   (a) Improves noise immunity
   (b) Decreases performance degradation
6. Internal reference voltage is available. Hence a power supply of single polarity is sufficient.
7. No noise generation.
8. Data transmission over long distance using balanced twisted pair 50 Ω lines is possible.

Disadvantages

1. High power dissipation.
2. Requires interfacing circuit to operate with other logic families.
3. When capacitive loads used fans out, speeds decrease.
4. Larger fan in is avoided as the speed decreases.
5. Due to the large frequency response shielding should be good.

Metal Oxide Semiconductor (MOS) IC

Operational Characteristic

1. Propagation delay: 100 ns
2. Fan out: 20
3. Power dissipation: <1 mW
4. Power delay product: 100 pJ
5. $Z_{out}(1)$: 2 kΩ
6. $Z_{out}(0)$: 100 kΩ
7. V_{dd}: +5 V
8. V_{gg}: +10 V

5.3 LOGIC GATES

A logic gate is an electronic circuit, which takes in one or more inputs and produces a single output. The possible combinations of the inputs and the corresponding outputs are tabulated in a truth table. The AND, OR, NOT gates are basic gates while NAND, NOR gates are universal gates. The NAND, NOR gates are so called as by using them the basic gates can be built.

5.3.1 Gate Realization Using Diodes and Transistors

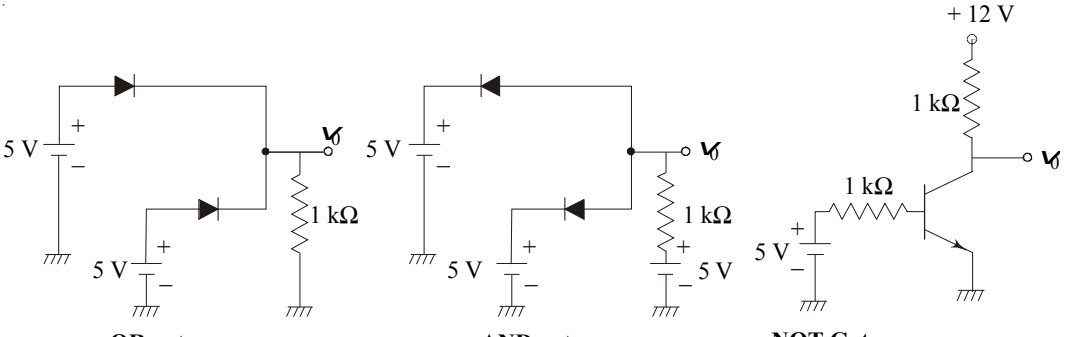


Fig. 5.1

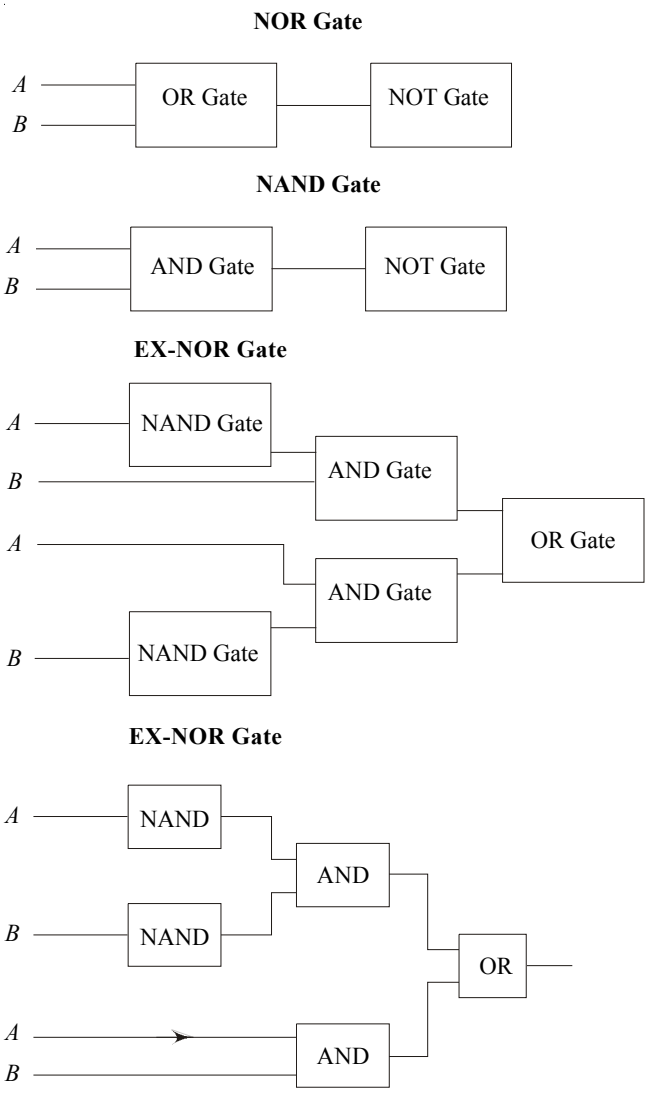


Fig. 5.2

5.3.2 Verification of Logic Gates Using ICS

OR Gate The logic of an OR gate is that it takes in one or more inputs and produces a single output which will be high if one or all its inputs are high. It produces a low output if all its inputs are low. The OR gate can be realized by the Boolean expression $Y = A + B$ and can be implemented using diodes as shown in Fig. 5.3.

Truth Table:

Input A	Input B	Output Y
Low	Low	Low
High	Low	High
Low	High	High
High	High	High

Fig. 5.3

AND Gate The logic of an AND gate is that it produces a high output only if all its inputs are high and produces a low output if any of its inputs are low. The AND gate can be realized by the Boolean expression $Y = A + B$ and can be implemented using diodes as shown in Fig. 5.4.

Truth Table:

Input A	Input B	Output Y
Low	Low	Low
High	Low	Low
Low	High	Low
High	High	High

Fig. 5.4

NOT Gate The logic of the NOT gate is that it produces the complement of the input. It has a single input and a single output. The Boolean equation for the NOT gate is $A = \overline{A}$ and it is implemented using a transistor as shown in Fig. 5.5.

Truth Table:

Input A	Output Y
Low	High
High	Low

Fig. 5.5

NAND and NOR Gates These gates produce the complementary outputs of AND and OR gates respectively.

These gates are implemented using diodes and transistors.

Truth Table:

NOR Gate:

Input A	Input B	Output Y
Low	Low	High
High	Low	Low
Low	High	Low
High	High	Low

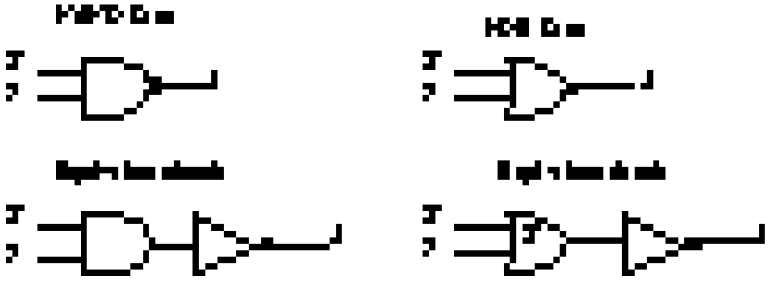


Fig. 5.6

NAND Gate:

Input A	Input B	Output Y
Low	Low	High
High	Low	High
Low	High	High
High	High	Low

EX-OR Gate:

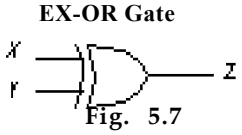


Fig. 5.7

EX-NOR Gate:

Fig. 5.8

5.3.3 Realization of Basic Gates Using Universal Gates

NAND equivalent of NOT gate:

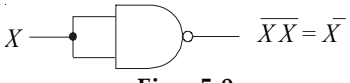


Fig. 5.9

NAND equivalent of AND gate:

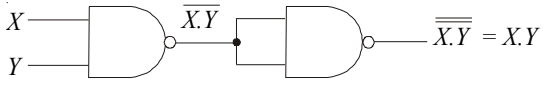


Fig. 5.10

NAND equivalent of OR gate:

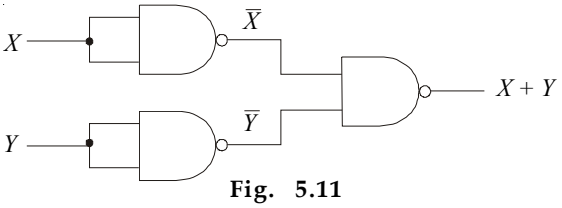


Fig. 5.11

NAND equivalent of NOR gate:

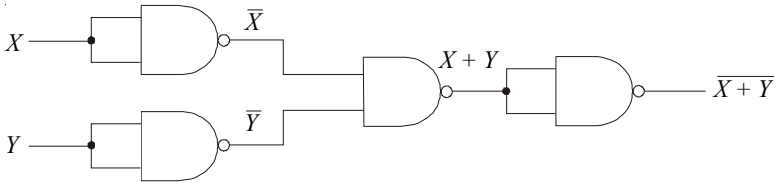


Fig. 5.12

NAND equivalent of EX-OR gate:

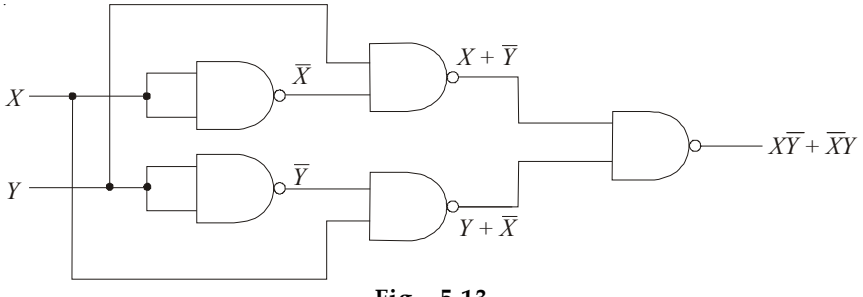


Fig. 5.13

NAND equivalent of EX-NOR gate:

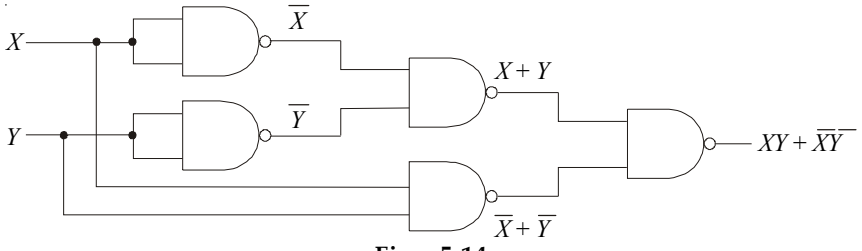


Fig. 5.14

NOR equivalent of NOT gate:

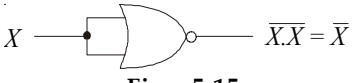


Fig. 5.15

NOR equivalent of AND gate:

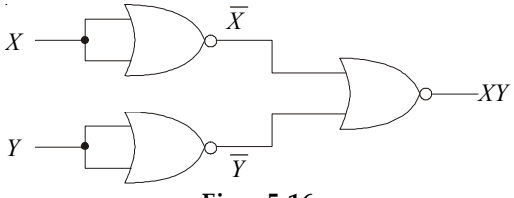


Fig. 5.16

NOR equivalent of OR gate:

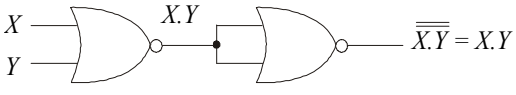


Fig. 5.17

NOR equivalent of NAND gate:

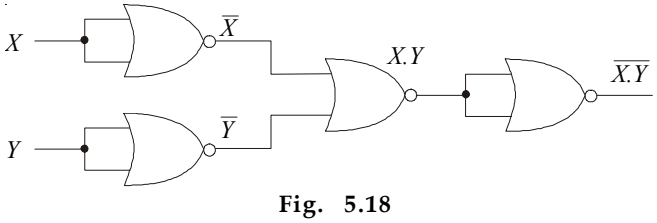


Fig. 5.18

NOR equivalent of EX-OR gate:

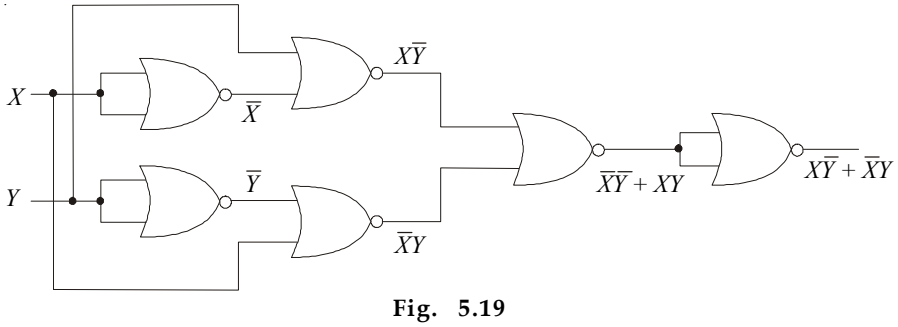


Fig. 5.19

NOR equivalent of EX-NOR gate:

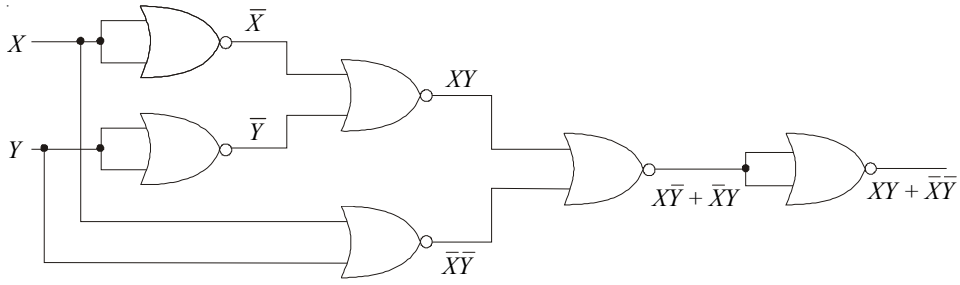
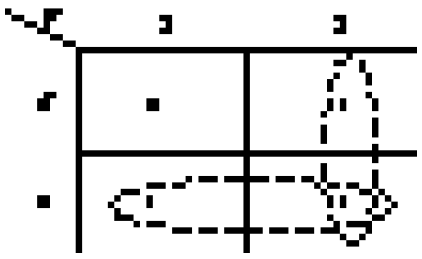


Fig. 5.20

Karnaugh Map (K-map) Karnaugh maps are effective in reducing a Boolean expression either to sum of product form or product of sum form.

Two Variable Form:



Eg., $F = \sum m(1, 2, 3) = \sum (m_1, m_2, m_3)$

$m_0 = 0\ 0 = \overline{A}\,\overline{B}$

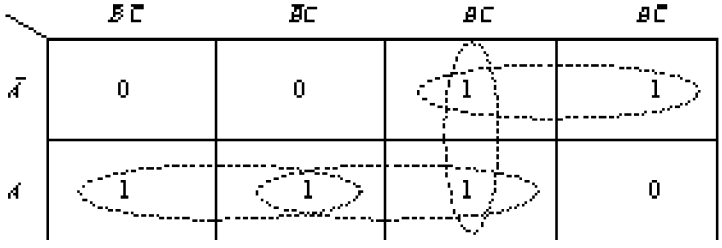
$m_1 = 0\ 1 = \overline{A}$ B

$m_2 = 1\ 0 = A\overline{B}$

$m_3 = 1\ 1 = A\ B$

Three Variable K-Map:

Eg., $F = \sum m(2, 3, 4, 5, 7) = \sum (m_2, m_3, m_4, m_5, m_7)$



$m_0 = 0\ 0\ 0 = \overline{A}\,\overline{B}\,\overline{C}$

$m_1 = 0\ 0\ 1 = \overline{A}\,\overline{B}\,C$

$m_2 = 0\ 1\ 0 = \overline{A}B\overline{C}$

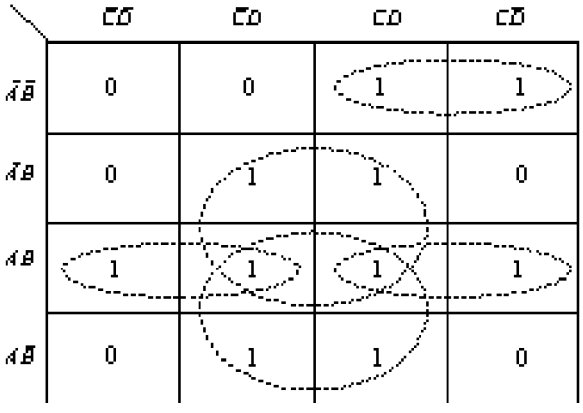
$m_3 = 0\ 1\ 1 = \overline{A}BC$

$m_4 = 1\ 0\ 0 = A\overline{B}\,\overline{C}$

$m_5 = 1\ 0\ 1 = A\overline{B}\,C$

$m_6 = 1\ 1\ 0 = AB\overline{C}$

$m_7 = 1\ 1\ 1 = ABC$



Four Variable K-Map:

$F = \sum m(2, 3, 5, 7, 9, 11, 13, 14, 15)$

5.3.4 Reduction Boolean Equation Using Karnaugh Map Method

Since every logic operator represents a corresponding element of hardware, we must reduce every Boolean expression to as simple as possible in order to reduce cost.

A Boolean expression can be written (direct/reduced) in two standard forms:

(a) sum of product (SOP)
(b) product of sum (POS)

Sum of Product

Example $F = ABC + A\overline{B}C + AB\overline{C}$

Each product term here consists of three variables A, B and C. Each such term is called a *Min term,* i.e., it is a product of all three variables in a SOP expression.

$$m_0 = 0\ 0\ 0 = \overline{A}\,\overline{B}\,\overline{C}$$

$$m_1 = 0\ 0\ 1 = \overline{A}\,\overline{B}\,C$$

$$m_2 = 0\ 1\ 0 = \overline{A}\,B\,\overline{C}$$

$$m_3 = 0\ 1\ 1 = \overline{A}\,BC$$

$$m_4 = 1\ 0\ 0 = A\,\overline{B}\,\overline{C}$$

$$m_5 = 1\ 0\ 1 = A\,\overline{B}\,C$$

$$m_6 = 1\ 1\ 0 = AB\,\overline{C}$$

$$m_7 = 1\ 1\ 1 = ABC$$

Therefore, $F = \sum\ (m_7, m_5, m_6)$

Product of Sum

Example $F = (A + B + C)\ (A + \overline{B} + C)\ (A + B + \overline{A})$

Each sum term here consists of three variables A, B and C. Each such term, is called a *Max term,* i.e., it is a sum of all three variables in a POS expression.

$$F = \pi\,(M_0, M_2, M_1)$$

In case of SOP, only 1's should be grouped evenly (2's, 4's, 8's).

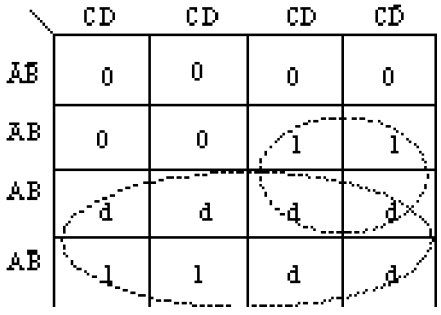
In case of POS, only 0's should be grouped evenly.

Incompletely Specified Functions Many designs require only certain min-terms to be defined, others could be either X's or O's?

Eg, in *bcd* code, only the states 0000 through 1001 are valid and states 1010 through 1111 which never appear are treated as *DON'T CARE*. *Don't cares* are represented by the symbols φ or d. They can be treated either as 1 or 0 depending on the design requirement.

Binary	Decimal	BCD	Excess-3
0000	0	0000	0011
0001	1	0001	0100
0010	2	0010	0101
0011	3	0011	0110
0100	4	0100	0111
0101	5	0101	1000
0110	6	0110	1001
0111	7	0111	1010
1000	8	1000	1011
1001	9	1001	ϕ
1010	10	ϕ	ϕ
1011	11	ϕ	ϕ
1100	12	ϕ	ϕ
1101	13	ϕ	ϕ
1110	14	ϕ	ϕ
1111	15	ϕ	ϕ

Example $Y = \sum m\,(6, 7, 8, 9) + \phi\,(10, 11, 12, 13, 14, 15)$



$Y = A + BC$

5.3.5 Gate Implementation of Boolean Expression

Experiment (Logic Gates)

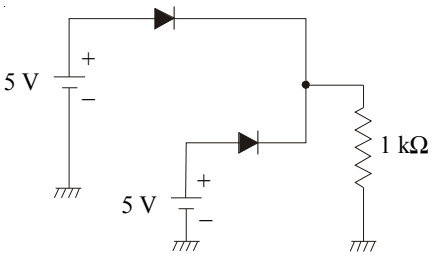
Aim: ***Realize the Logic Gates Using Diodes and Transistor***

Components Required:

Name of the component	Number	Quantity
Diode	IN4001	2
Resistor	1 kΩ	1
	68 kΩ	

Circuit Diagram:

OR Gate



AND Gate

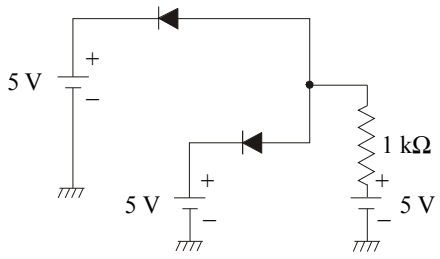
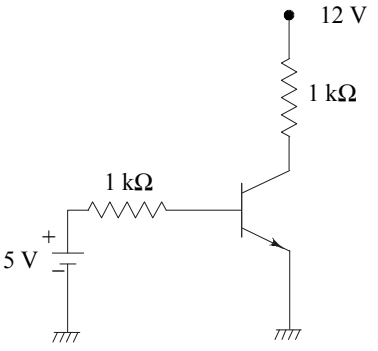


Fig. 5.21

NOT Gate



EX-OR Gate

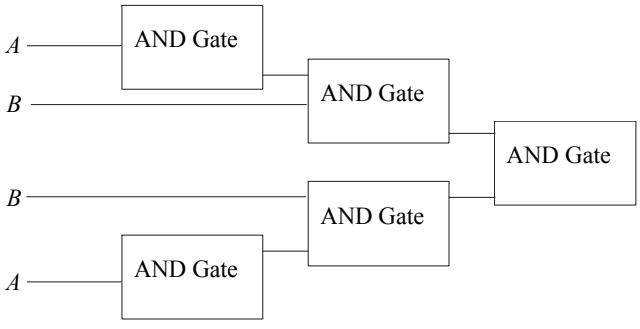
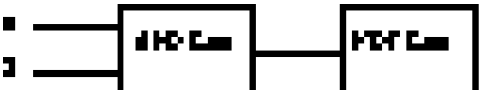


Fig. 5.22

NAND Gate



NOR Gate

Fig. 5.23

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Low level refers to 0 V; high level refers to + 5 V.
3. Switch on the input according to the truth table condition.
4. Verify the output and compare it with the truth table result.
5. Continue the above procedure for all other gates.

Truth Tables:

OR Gate:

Input A	Input B	Output Y
Low	Low	Low
High	Low	High
Low	High	High
High	High	High

AND Gate:

Input A	Input B	Output Y
Low	Low	Low
High	Low	Low
Low	High	Low
High	High	High

NOT Gate:

Input A	Output Y
Low	High
High	Low

NOR Gate:

Input A	Input B	Output Y
Low	Low	High
High	Low	Low
Low	High	Low
High	High	Low

NAND Gate:

Input A	Input B	Output Y
Low	Low	High
High	Low	High
Low	High	High
High	High	Low

EX-OR Gate:

Input A	Input B	Output Y
Low	Low	Low
Low	High	High
High	Low	High
High	High	Low

EX-NOR Gate:

Input A	Input B	Output Y
Low	Low	High
Low	High	Low
High	Low	Low
High	High	High

Experiment (Simplification of a Boolean Expression and its Realization Using Logic Gates)

Aim: ***To Simplify the given Boolean Expression and Realise the Resultant Expression Using***

(a) Basic gates

(b) Universal gates

Equipments Required:

Equipment	Quantity
Digital IC trainer kit	1
Patch cords	20

Components Required:

IC name	Quantity
IC 74LS00	1
IC 74LS02	1
IC 74LS04	1
IC 74LS08	1
IC 74LS32	1
IC 74LS21	1

Circuit Diagram:

Sum of products:

$$Y = \overline{A}\,B\,\overline{C} + \overline{A}\,\overline{B}\,C + ABC$$

Logic implementation using BASIC gates:

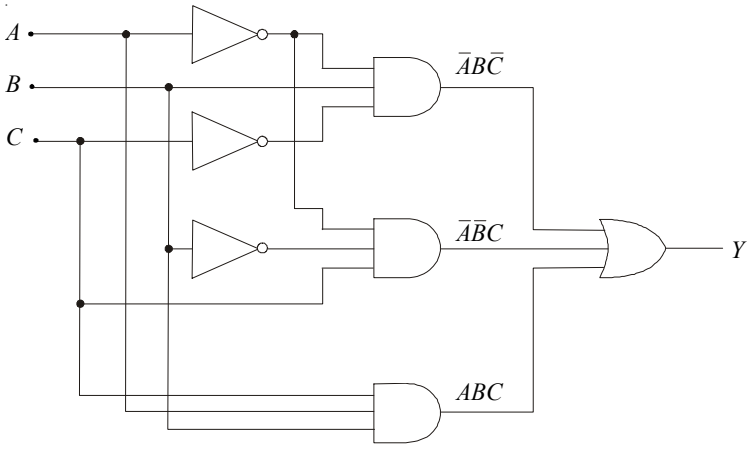


Fig. 5.24

Logic implementation using NAND gates:

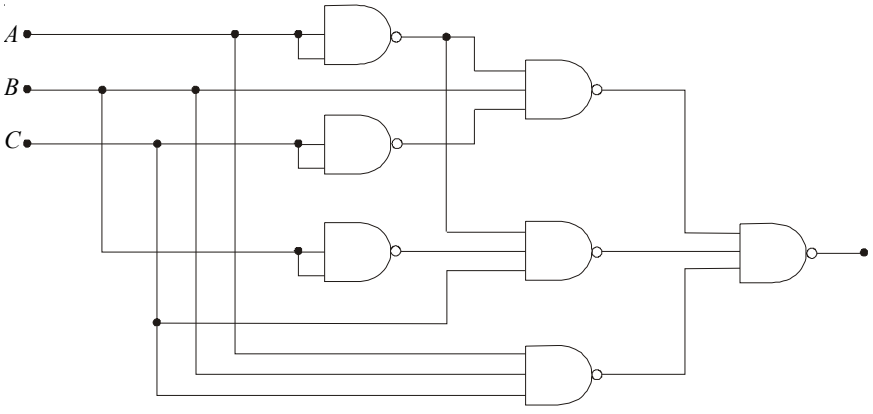


Fig. 5.25

Logic implementation using NOR gates:

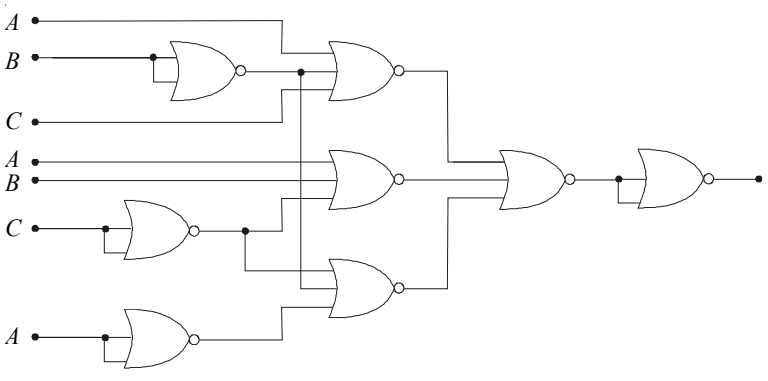


Fig. 5.26

Product of Sums:

$$Y = (A + B)\ (\overline{A} + \overline{C})\ (\overline{B} + C)$$

Logic implementation using BASIC gates:

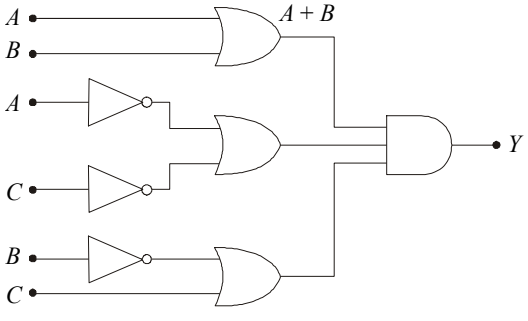


Fig. 5.27

Logic implementation using NOR gates:

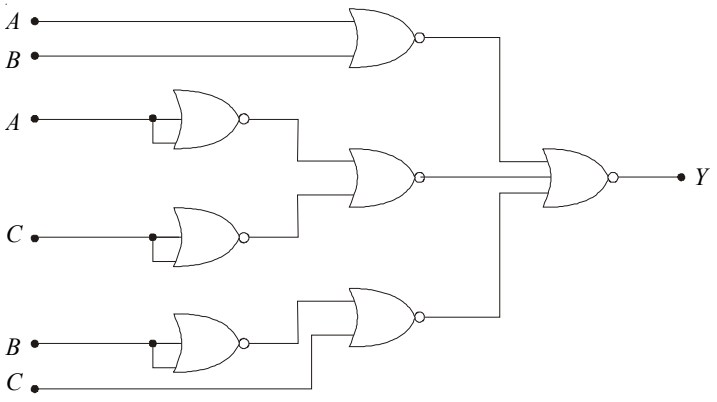


Fig. 5.28

Logic implementation using NAND gates:

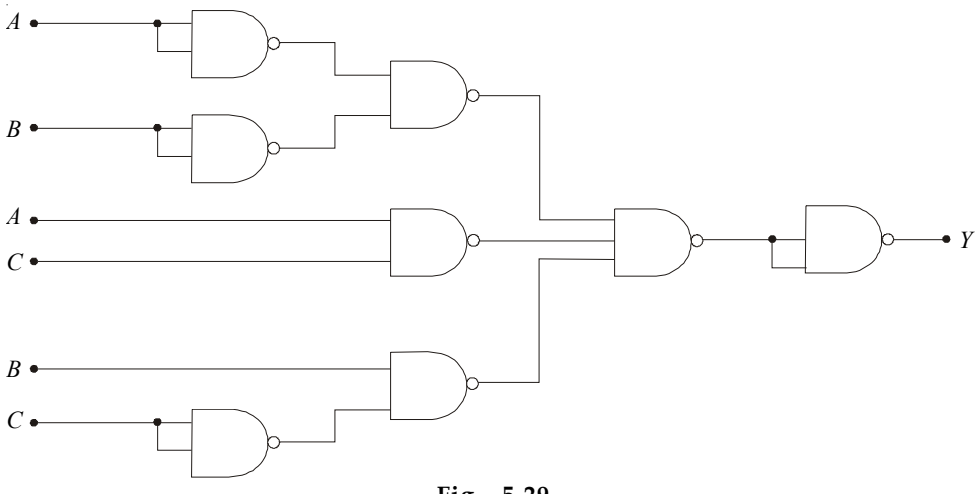


Fig. 5.29

Procedures:

1. Connect the circuit as per the circuit diagram and pin configurations of the IC.
2. Switch on the supply and note down the outputs for all the possible combinations of inputs.
3. Repeat the same using Universal gates.

Example:

$$XY + \overline{X}\overline{Y}\overline{Z} + \overline{X}Y\overline{Z}$$

$$XY + \overline{X}\overline{Z}\left[\overline{Y} + Y\right]$$

$$XY + \overline{X}\overline{Z}$$

This equation can be realized using NAND gates. On converting equation 1 into product of sum form, we get $(\overline{X} + \overline{Y})\ (X + Z)$. This equation can be realized using NOR gates.

Observation and Tabulations: $XY + \overline{X}\overline{Z}$

X	Y	Z	$\overline{X}$	$\overline{Z}$	XY	$\overline{X}\,\overline{Z}$	$XY + \overline{X}\,\overline{Z}$
0	0	0	1	1	0	1	1
0	0	1	1	0	0	0	0
0	1	0	1	1	0	1	1
0	1	1	1	0	0	0	0
1	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0
1	1	0	0	1	1	0	1
1	1	1	0	0	1	0	1

$$\left(\overline{X} + \overline{Y}\right)(X + Z)$$

X	Y	Z	$\overline{X}$	$\overline{Y}$	$\overline{Y} + \overline{Y}$	$\overline{X} + \overline{Z}$	$\left(\overline{X} + \overline{Y}\right)(X + Z)$
0	0	0	1	1	1	0	0
0	0	1	1	1	1	1	1
0	1	0	1	0	1	0	0
0	1	1	1	0	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	0	0	1	0
1	1	1	0	0	0	1	0

Result:

The given Boolean expression was simplified and realized using logic gates.

Exercises:

1. Write the logic, Boolean expression and truth table of an EX-OR gate.
2. Realize the EX-OR gate using NOR gates.
3. Justify the statement UNIVERSAL gates.

5.4 BINARY ADDERS

The basic operations in a digital computer are addition and subtraction, as multiplication is repeated addition and division is repeated subtraction. Hence the binary adder and subtractor are important building blocks in a digital computer. Half-adder performs the addition of two binary digits. The sum in a half-adder is provided by an EX-OR gate while the carry is provided by the AND gate. When the number of bits is more than 2, the addition is performed using a full-adder. The binary addition is done either serially or parallelly. In serial addition, the execution time is more and hardware is less. In a parallel adder, hardware is more, while the execution time is less.

The adders can be operated either in the serial or parallel mode. The serial addition has the advantage of less hardware, i.e., it requires only one adder circuit to perform addition for any number of bits. In parallel addition, for every bit an adder is required. The advantage of parallel addition is that the execution time is less as the addition of all bits is performed simultaneously, whereas the execution time of serial adders is very high. Depending on the number of bits to be

added the adders can be classified as *half-adder* or *full-adder*. The half-adder is used to add two bits and the full-adder is used to add three bits.

Half-Adder The half-adder is used to add two bits called the augend and addend and it produces two outputs sum and carry.

Serial Adder The serial addition is performed using a full-adder circuit. The LSBs are first added and the carry resulting from this addition is taken as the third bit during the addition of the next higher bits. A delay FF is used to delay the carry bit by one clock pulse so that it is available at the input during the addition of the next higher bits. Thus any number of bits can be added in a sequential manner using a single adder in serial addition.

Parallel Adder The parallel adder requires one full-adder for each bit except for the LSB. The LSB are added using a half-adder and the next higher bits are added using full-adders. The adders are connected in cascade and the carry from the previous stage is carried on to the next stage for addition. Consider the inputs $ABC + XYZ$. The half-adder adds the LSB C and Z and gives out the sum and carry. The next full-adder adds the carry and the bits B and Y resulting in a sum and carry. This carry is carried on to the next stage where a full-adder adds the MSB A and X along with the carry and gives out the sum and carry outputs. Thus the parallel adder adds all the bits simultaneously and gives the outputs of all the bits at the same time.

Experiment (Adders)

Aim: ***To Construct and Verify the Operation of Half-Adder and Full-Adder Using Logic Gates.***

Equipments Required:

Equipment	Quantity
Digital IC trainer	1
Kit	1
Patch cords	20

Components Required:

Component	Quantity
IC 74LS08	1
IC 74LS32	1
IC 74LS86	1

Circuit Diagram:

Using BASIC gates:

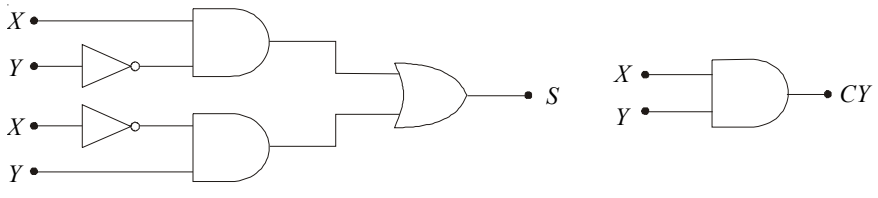


Fig. 5.30

Using NAND gates:

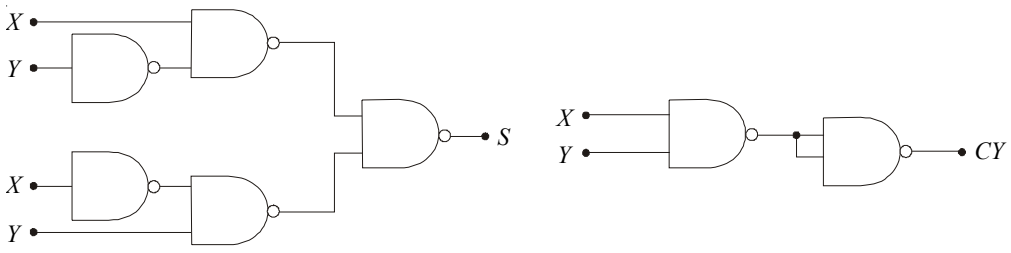


Fig. 5.31

Using NOR gates:

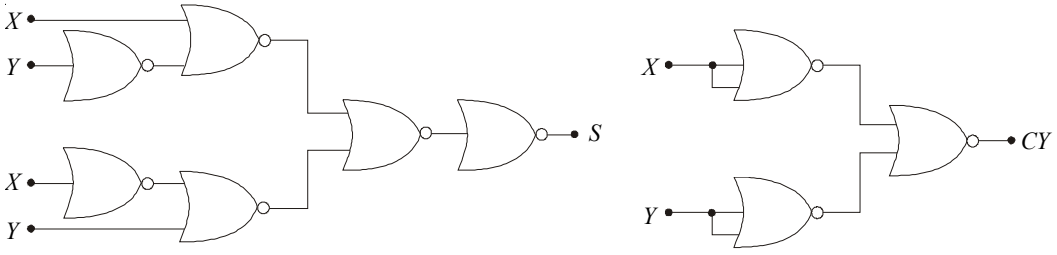


Fig. 5.32

Using EX-OR gates:

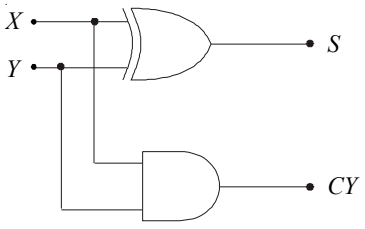


Fig. 5.33

Full adder:

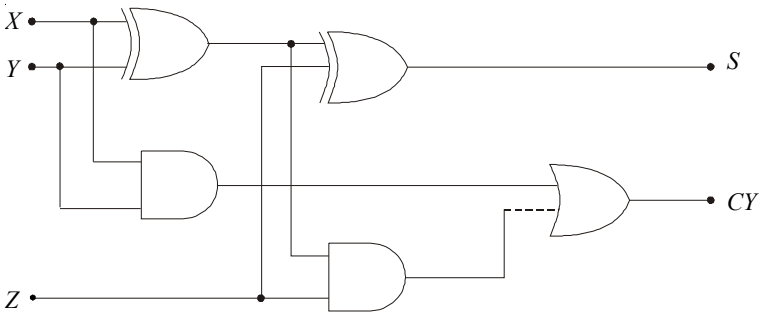


Fig. 5.34

Block diagram of full adder using two half-adders:

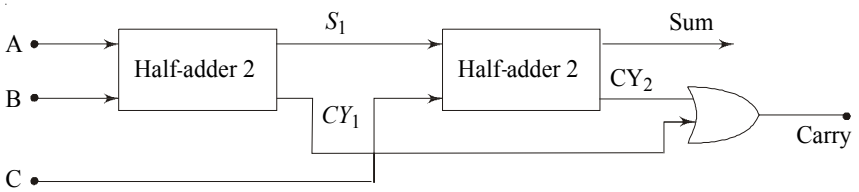


Fig. 5.35

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Give logical inputs as per the respective truth table.
3. Observe the logical output and verify with your truth table.

Truth Table:

Half-adders:

A	*B*	Sum (*S*)	Carry (*Cy*)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full-adder:

A	*B*	*C*	Sum (*S*)	Carry (*Cy*)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Result:

The operation of a half-adder and full-adder were studied.

5.5 BINARY (SUBTRACTION)

Experiment (Subtractor)

Aim: ***Design of Half-Subtractor and Full-Subtractor***

Half-Subtractor:

Truth Table:

X	Y	Borrow (B)	Output difference (D)
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

$$D = \overline{X}\,Y + X\overline{Y} = X \oplus Y$$

$$B = \overline{X}\,Y$$

Using BASIC gate:

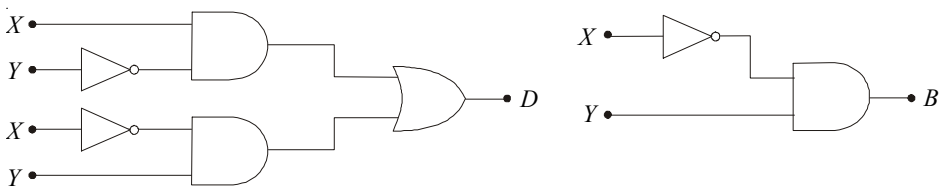


Fig. 5.36

Using NAND gate:

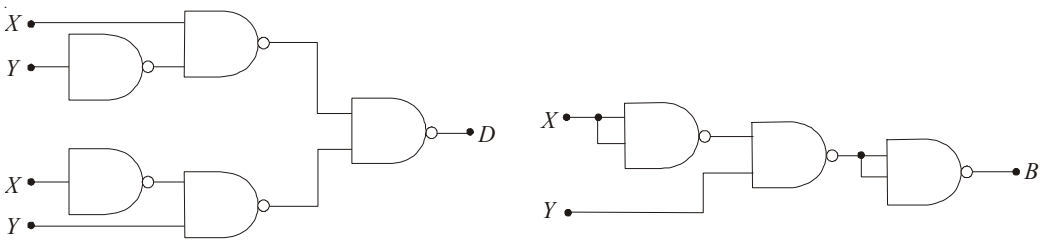


Fig. 5.37

Using NOR gate:

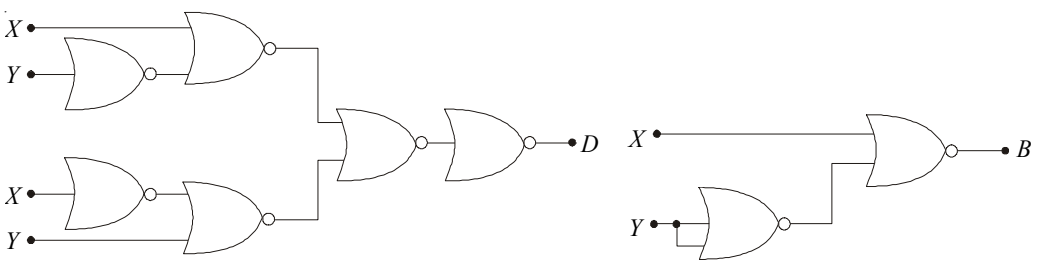


Fig. 5.38

*** Full-Subtractor:**

Truth-Table:

A	*B*	*C*	Borrow (B)	Output (D) Difference
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D = \overline{X}\overline{Y}Z + \overline{X}\overline{Z}Y + \overline{Y}\overline{Z}X + XYZ = X \oplus Y \oplus Z$$

$$B = \overline{X}Y + \overline{X}Z + YZ$$

** Note: Try your circuit and implement.*

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Give logical inputs as per the respective truth table.
3. Observe the logical output and verify with your truth table.

5.6 PARITY GENERATOR AND CHECK ER

EX-OR gates are very useful in systems requiring error detection and correction codes. A parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with the message to make the number of 1's either odd or even. The message including the parity bit is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the transmitted one. The circuit that generates the parity bit at the transmitter is the parity generator and the circuit that checks the parity at the receiver is the parity checker.

Consider a message to be transmitted with an even parity. Let the inputs X, Y and Z be fed to an EX-OR gate and the output of the gate is the parity bit generated. The EX-OR gate generates a 1 if the odd number of inputs is high and a 0 if even number of inputs is high. Hence the output of the EX-OR gate is as follows and the bit generated maintains the information to be of even parity.

Truth Table

X	*Y*	*Z*	Parity bit (*P*)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

The three-bit message along with the parity is transmitted to the destination and applied to the parity checker to check for possible errors in the transmission. Since the information was transmitted with even parity, the 4 bits must have an even number of 1's. An error is said to have occurred during the transmission if the four bits received have an odd number of 1's indicating that one bit has changed in value during transmission. The output of the parity checker denoted by *C* is 1 if an error occurs.

Parity is an extra bit added to the word being transmitted for the purpose of detecting the error in the data communication. Hence the name *Error detecting code* for parity. There are two types of parity bit.

1. Odd parity
2. Even parity

Odd Parity Odd parity is to see that the total number of 1's in the word is *ODD* including the parity bit.

Even Parity Even parity is to see that the total number of 1's in the word is *EVEN* including the parity bit.

Experiment (Parity Generation and Checking)

Aim: ***Design of Even Parity Generator and Checker***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-5) V	1

Components Required:

Components	Quantity
7486	3

Circuit Diagram:

Even parity generator:

Truth Table:

X	*Y*	*Z*	Parity bit (*P*)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$P = \overline{X}\overline{Y}Z + \overline{X}\overline{Z}Y + \overline{Y}\overline{Z}X + XYZ = X \oplus Y \oplus Z$$

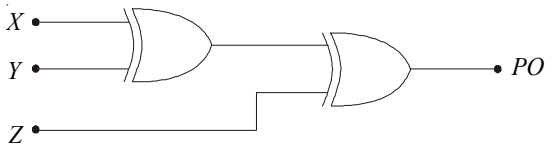


Fig. 5.39

Even parity checker:

X	*Y*	*Z*	Parity (P)	Parity Error Checker ©
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
0	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

$C = X \oplus Y \oplus Z \oplus P$

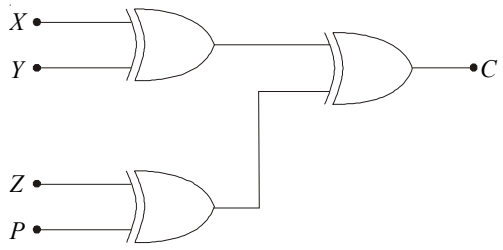


Fig. 5.40

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Give logical inputs as per the respective truth table.
3. Observe the logical output and verify with your truth table.

5.7 MULTIPLEXER

Multiplexing means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of the many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. There are 2 input lines and *n* selection lines whose combinations determine the input bit selected. A 4-1 line multiplexer is shown in the circuit. Each of the four input lines I_0 to I_3 is applied to one of the AND gates selected by the signals S_0 and S_1. For e.g., consider the case $S_0S_1 = 01$, then the AND gate 2

alone is enabled and the data I_2 is transmitted to the output. The outputs of all the AND gates are fed to an OR gate and the output of the OR gate will be the data I_2. *Enable* input can be used to control the operation of the circuit as one state of the input enables the circuit and the other state disables it.

Truth Table:

Inputs		Outputs
X	Y	
0	0	D_1
0	1	D_2
1	0	D_3
1	1	D_4

A multiplexer is also called a *Data Selector*. It selects one of the several inputs and then feeds it through to a single output. A multiplexer can be used for parallel to serial conversion.

Experiment (Multiplexer)

Aim: ***Design and Implement A* 4:1 *Multiplexer Using Logic Gates***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-5) V	1

Components Required:

Components	Quantity
7404	1
7411	4
LED	4

Circuit Diagram:

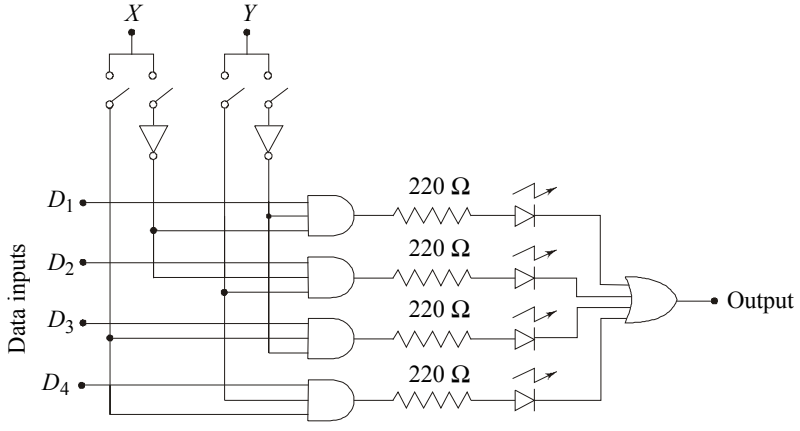


Fig. 5.41

Truth Table:

Inputs		Outputs
X	Y	
0	0	D_1
0	1	D_2
1	0	D_3
1	1	D_4

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Give logical inputs as per the respective truth table.
3. Observe the logical output and verify with your truth table.

Exercise:

Obtain EX-OR operation on a multiplexer.

5.8 DEMULTIPLEXER

A demultiplexer is a circuit that receives information on a single line and transmits this information on one of the possible output lines. The selection of the specific output line is controlled by the bit values of the 'n' selection lines. For e.g., if the selection inputs are $A = 0$, $B = 1$ then the AND gate 2 is enabled and the data available is passed on to the output through the output line Y_1.

Truth Table:

Inputs		Output			
A	B	Y_0	Y_1	Y_2	Y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

A demultiplexer is reverse of multiplexer. Input is connected through to the selected output line depending on the information on the control lines. It is used to convert serial data to parallel form.

Experiment (Demultiplexer)

Aim: ***Design and Implement A* 4:1 *Demultiplexer Using Logic Gates***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-5) V	1

Components Required:

Components	Quantity
7411	4
7404	1
LED	4

Circuit Diagram:

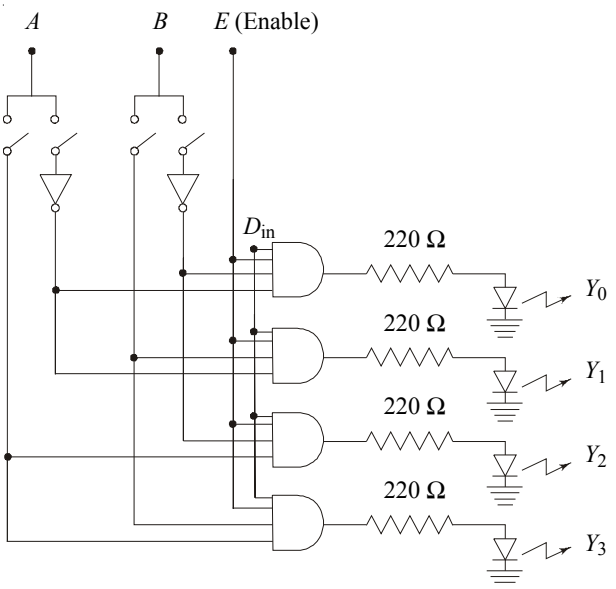


Fig. 5.42

Demultiplexer

Truth Table:

Enable	*Select Lines*		*Data input*	*Outputs*			
E	*A*	*B*	D_{in}	Y_0	Y_1	Y_2	Y_3
0	X	X	X	0	0	0	0
1	X	X	0	0	0	0	0
1	0	0	1	1	0	0	0
1	0	1	1	0	1	0	0
1	1	0	1	0	0	1	0
1	1	1	1	0	0	0	1

*X = '1' or '0'

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Give logical inputs as per the respective truth table.
3. Observe the logical output and verify with your truth table.

5.9 ENCODERS

An encoder is a digital circuit, which performs the inverse operation of a decoder. An encoder has 2^n input lines and *n* output lines. The output lines generate the binary code corresponding to the input value. The encoder can be implemented using OR gates. The OR gates are given the inputs in such a way that when any one of the input line is enabled, i.e., connected to high, the OR gates give out an o/p which will be the binary equivalent of the input given. For e.g., if the input line 5 is enabled then the outputs Y_0–Y_4 will be 0101, the binary equivalent of 5.

Priority Encoder

A priority encoder is an encoder circuit that includes the priority function. The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence. The input D_0 has the least priority while the input D_3 has the highest priority. The output V is high if any of the inputs is high. If the input D_0 is high the output is $XY = 00$. If the input D_1 is high the o/p $XY = 01$. If the input D_2 is high the output is 10 and if D_3 is high the output is 11. The output for D_3 appears regardless of the values of the other inputs as it has the highest priority. Similarly, the output for the input D_0 appears only if all the higher bits are 0 since it has the least priority. The Boolean expressions for the outputs of the priority encoder are:

$$X = D_2 + D_3$$
$$Y = D_3 + D_1 \overline{D_2}$$
$$V = D_0 + D_1 + D_2 + D_3$$

Circuit Diagram:

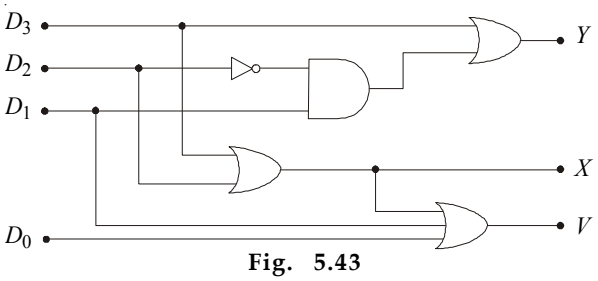


Fig. 5.43

Truth Table:

Inputs				Outputs		
D_0	D_1	D_3	D_4	X	Y	V
0	0	0	0	0	0	0
1	0	0	0	0	0	1
0	1	0	0	0	1	1
0	0	1	0	1	0	1
0	0	0	1	1	1	1

An encoder is a digital circuit that performs the inverse operation of a decoder. It has 2^n inputs and n outputs. The output is the binary code for the input value fed in. When an input line is energized, the output gives the corresponding binary code. When two input lines are active simultaneously, the output produces an undefined combination. To overcome this ambiguity a priority encoder is used in which priority is given to the largest number.

Experiment (Encoders)

Aim: ***Design and Implementation of Encoders Using Logic Gates***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-5)V	1

Components Required:

Components	Quantity
7402	2
7420	1
7408	1
7404	1
LED	4

Circuit Diagram:

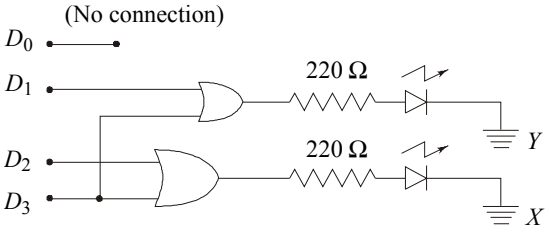


Fig. 5.44 Encoder

Functional Table:

Inputs				Outputs	
D_0	D_1	D_2	D_3	X	Y
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Above conditions can be expressed by the following output Boolean expression

$$X = D_2 + D_3$$

$$Y = D_1 + D_3$$

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Give logical inputs as per the respective truth table.
3. Observe the logical output and verify with your truth table.

Exercise:

1. Compare an encoder and multiplexer.
2. Explain the operation of a priority encoder.
3. Design a decimal to BCD encoder using universal gates.
4. Conduct the decimal to BCD encoder using IC 74147.

5.10 DECODERS

A binary code of n bits is capable of representing up to two distinct elements of the coded information. A decoder is a combinational circuit that converts binary information from n input lines into a maximum of two output lines. The decoders are also known as binary to decimal converters. Consider the given circuit in which A and B are the inputs. Depending on the combination of the inputs one of the output lines is high. For e.g., if $A = 0$, $B = 0$ then the AND gate 1 whose inputs are A' and B' alone will give a high output while all the other gates will have a low output. Thus Y_0 which is the decimal equivalent of 0 alone is high.

Truth Table:

Inputs		Outputs			
X	Y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

The decoder circuit can be extended to any number of inputs. The operation of the decoder circuit can be controlled by enable input. The decoder circuit functions only if this input opens the gates. For the above example the enable signal has to be high for the AND gates to respond to the input signals.

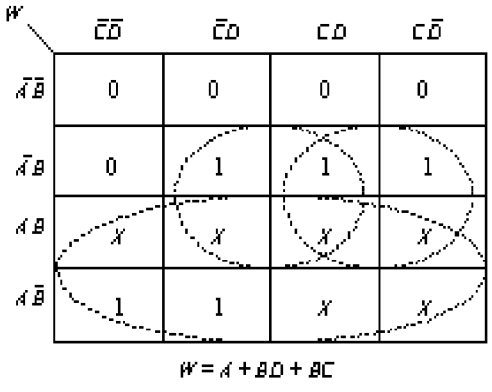
The decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^2 unique output lines. Traditional uses of the decoder include code converters or read only memories. The operation of the decoders is controlled using STROBE inputs. A strobed decoder gives an output only if the STROBE input is enabled or high.

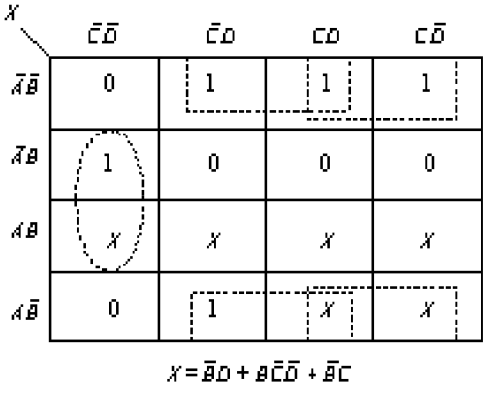
Design of BCD to Excess-3 Decoder

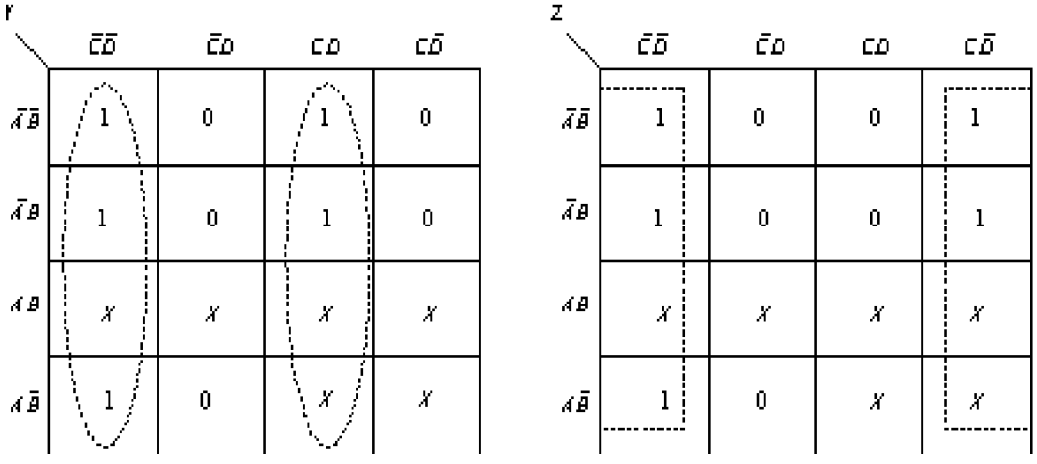
This design accepts BCD inputs and outputs an EXCESS-3 code equivalent.

Functional Table	
BCD Inputs	Excess-3 Output
0000	0011
0001	0100
0010	0101
0011	0110
0100	0111
0101	1000
0110	1001
0111	1010
1000	1011
1001	1100

Obtain the equation for W, X, Y and Z using K-maps with A, B, C and D as inputs.






Y
$\bar{C}\bar{D}$ $\bar{C}D$ CD $C\bar{D}$
$\bar{A}\bar{B}$ 1 0 1 0
$\bar{A}B$ 1 0 1 0
AB X X X X
$A\bar{B}$ 1 0 X X
Z
$\bar{C}\bar{D}$ $\bar{C}D$ CD $C\bar{D}$
$\bar{A}\bar{B}$ 1 0 0 1
$\bar{A}B$ 1 0 0 1
AB X X X X
$A\bar{B}$ 1 0 X X

$Y = \overline{C}\overline{D} + CD$ $Z = \overline{D}$

Experiment (Decoders)

Aim: ***Design and Implementation of Decoders Using Logic Gates***

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-5) V	1

Components Required:

Components	Quantity
7408	1
LED	4
7404	1

Truth Table:

Inputs		Outputs			
X	Y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Circuit Diagram:

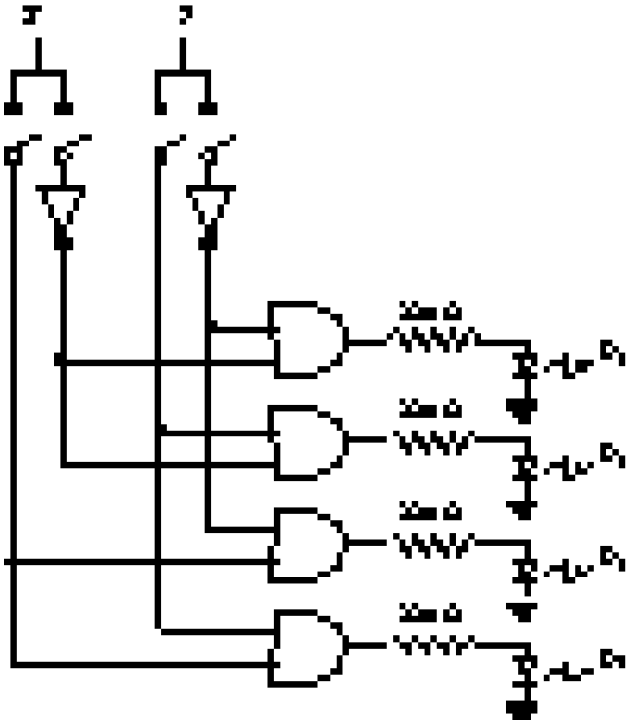


Fig. 5.45

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Give logical inputs as per the respective truth table.
3. Observe the logical output and verify with your truth table.

Truth Table:

Inputs		Outputs			
X	Y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Exercises:

1. Conduct the BCD to Decimal encoder using IC 7445.
2. Design a BCD to Excess-3 decoder using logic gates.
3. Compare a decoder and demultiplexer.
4. Discuss the operation of a BCD/7 segment decoder.
5. Discuss about a strobe signal.

Note: Decoders permit one of the 'n' outputs to be selected depending on the address on the select lines or control lines. Any of the demultiplexers can be used as a binary decoder

by providing a constant, continuous '1' (or removing permanently the input signal channel) on the signal input line.

BCD to 7 Segment Display Decoder This circuit facilitates the operation of seven segment devices such as incandescent lamps, LED, LCD. The output of the decoder is designed in such a way that segments of the corresponding decimal digit is enabled. For e.g., consider the segments of the display, i.e., $a - g$. The segments other than g should glow if the digit is 0. The inputs A, B, C, D will be 0 and the decoder outputs to the segments $a - f$ should be high and to the segment g should be low for the digit 0 to glow. Similar analysis can be done for the other digits also as given below.

Decimal	BCD Code				7-Segment Op-Code						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	1	0	0	1	1	1	1	1	1	1
9	1	1	0	1	1	1	1	0	0	1	1

5.11 DIGITAL LOGIC FAMILIES

Digital Integrated Circuits

In electronic digital circuits 0 and 1 are always represented by high and low. Many functions are being preferred with these two inputs and are realized by using logic gates. A logic gate is an electronic circuit, which can take in one or more inputs and give a single output. A logic circuit can be operated in two logics.

1. Positive logic.
2. Negative logic.

Positive Logic In positive logic convention, logic 1 is assigned the more positive value of the two voltage levels and logic 0 is assigned the less positive value.

Negative Logic In this logic, 0 is assigned the more positive value and logic 1 is assigned the less positive value.

Digital ICs are circuits, which perform logic functions using these inputs. It is basically classified as bipolar ICs and MOS ICs. The digital ICs are classified into different logic families depending on the components and logic used. RTL, DTL, TTL, ECL, HTL, etc., are a few logic families commonly used.

Characteristics of Digital ICs

1. Logic Flexibility.
2. Operating Speed.

3. Availability of complex functions.
4. Power dissipation.
5. Supply voltage.
6. Noise immunity.
7. Noise generation.
8. Fan-in /Fan-out.
9. Cost.
10. Operating temperature range.

Logic Flexibilty This is a measure of the utility of the IC in meeting the needs of the system.

1. Wired Logic Capability Connecting the gate output together or using them directly to perform additional logic functions without any external hardware.

2. Complementary Outputs If the IC has complementary output facility then the requirement of extra inverters can be avoided.

3. Driving Non-Standard Loads Non-standard loads like long lines electromagnetic relays have to be driven so that the need for the coupling elements can be avoided.

4. I/O Facilities The number of inputs of the gate, the input impedance and output impedance at both logic 0 and 1 determine the I/O capacity of the IC.

5. Ability to Drive Other Logic Forms This character avoids the necessity of external interfacing circuits and hence reduces the space and system cost.

6. Types of Gates The logic family should have many types so that when used in a system, interconnections and power supply requirements can be simplified.

Operating Speed The operating speed of an IC should be very high, as it reduces the operating and execution time. When high speed ICs are available, the system can be designed to operate in the serial mode rather than in a parallel mode, as this would reduce the system cost.

Speed of an IC is limited by the following factors:

Propagation Delay This is due to the finite operating speed of the active devices and RC time constants of the associated circuitry. Since the delay from logic 1 to logic 0 is different from the delay from logic 0 to logic 1 the average of both is taken as the propagation delay.

Pair Delay This is a measure of the propagation delay through two inverters.

Complex Functions Grouping of basic gates in a single package chip is termed as complexity of the IC. The chip size, number of pins per gate and the overall number of input/output pins per package are important factors of consideration. With increase in complexity the number of input/output terminals for the IC increases but at a decreased rate. With increase in the complexity the reliability and assembling cost of the IC are increased.

Power Dissipation This factor should be low as it reduces cooling, power supply and distribution cost. With decrease in power dissipation of a gate, f of the active device decreases and RC time constants increases. This increases the propagation delay. Hence a decrease in power dissipation is achieved at the cost of increase in propagation delay.

Supply Voltage A standard supply voltage is used for every logic family. A + 5V is usually used for standard TTL.

Noise Immunity An IC should have high noise immunity. This is a characteristic term of noise voltage and pulse width, that can be tolerated by the circuit or total noise energy required causing a false output of the logic gate. This noise immunity depends on the following.

Parameters of a gate:

1. Supply voltage
2. Fan-in
3. Fan-out
4. Stray inductance
5. Stray capacitance
6. Source of noise
7. Shape of the noise source

To specify the noise immunity of an IC the following definitions are considered:

A. DC Noise Immunity This is specified in terms of the noise margin. The DC noise margin is defined as the difference between the guaranteed logic state voltage limits of a driving gate and the voltage requirements of a driven gate.

B. AC Noise Immunity This considers the amplitude and pulse width of the noise signal. If the pulse width is more noise immunity is less. But if it is less than the propagation delay the noise immunity is high.

Noise Generation

1. External Noise Noise radiated into the system due to the make and break contacts, which are present near the IC.

2. Power Line Noise Due to AC or DC power distribution system this noise is generated.

3. Cross Talk This is due to interference from adjacent signal lines.

4. Signal Current Noise Noise from unterminated or mismatched transmission lines.

Icc Current Spikes There are many causes for this type of noise.

1. Unequal currents drawn from the supply under logic 0 and 1 conditions.
2. Charging of load capacitor.
3. Conduction overlap at the output when going from one state to another. This noise is an internal noise and hence can be reduced by suitable design.

Fan-in This indicates how many input terminals are there for the gate. This depends on the number of diodes for DTL logic and the number of emitters for TTL logic. Normally fan-in is less than or equal to 15.

Fan-out This indicates how many gates it can drive. This is governed by the output and input currents of an IC at logic 0 and 1.

$$\text{Fan-out} = \frac{I_{out}\ (1)\ (\min)}{I_{in}\ (1)\ (\max)} \cdots\cdots\cdots \text{for logic 1.}$$

$$\text{Fan-out} = \frac{I_{out}\ (0)\ (\min)}{I_{in}\ (0)\ (\max)} \cdots\cdots\cdots \text{for logic 0.}$$

Cost The overall cost of an IC depends on the fabrication technique, packing, shielding, etc.

Operating Temperature Range The operating range of temperature of an IC should be very wide. In general it is as follows:

(a) Consumer and Industrial applications: 0 – 70° C
(b) Military and Space applications: – 55° C to + 125° C.

Building Blocks of a Digital System

Digital systems are broadly classified as

1. Combinational system
2. Sequential system

Combinational System This is based on the combinational logic where the output of the system depends only on the inputs at that instant, e.g., binary adders, decoder, multiplexer, PLA, etc.,

Sequential System This is based on sequential logic where the output of the system depends not only on the input but also on the previous outputs, e.g., flip-flops, counters, shift registers.

5.12 STUDY OF FLIP-FLOPS

A *Flip-Flop* is a bistable multivibrator, which is capable of storing one bit of information. A flip-flop has two outputs, one for normal value and one for the complement value. The inputs to the flip-flops can be fed in a number of ways and this fact gives rise to different types of flip-flops. However, there are two characteristics shared by all flip-flops:

1. The flip-flop is a bistable device that can store a binary bit of information. If input causes it to go to the '1' state, it will remain there until some signal causes it to go to the '0' state. Similarly, once placed in the '0' state, it remains there until told to go to the '1' state.
2. The flip-flop has two output signals, one of which is the complement of the other.

5.12.1 RS Flip-Flops

The RS flip-flop can be realized using either NAND or NOR gates. The gates are cross-coupled which gives a feedback to the input from the output. The flip-flop has two inputs R and S, i.e., the Set and Reset and it has two outputs Q and $\overline{Q}$. Let us analyze the operation of the circuit.

RS Flip-Flop using NAND Gates The NAND gate gives a high output when any of its input is low and hence the gate is disabled when there is a '0' at the input. To start with, let $Q = 0$ and $\overline{Q} = 1$, i.e., the flip-flop is cleared.

1. When $R = 0$, $S = 0$: The NAND gates are disabled and the outputs of both the gates are high which is an undefined condition.
2. When $R = 0$, $S = 1$: NAND gate 1 gets '0' as input and the output of this gate is '1'. Since Q = 1 and S = 1, the NAND gate 2 gives '0' as an output. Thus when the set input is high the flip-flop is set.
3. When $R = 1$, $S = 0$: NAND gate 2 gets '0' as input and the output of this gate is '1'. The inputs to the NAND gate 1 are R and $\overline{Q}$ which are 1 and the output is low. Thus, when the reset input is high the flip-flop is reset to low.
4. When $R = 1$, $S = 1$: Since both the inputs are high both the gates are enabled and it checks for the other input to give an output. If $Q = 0$, then NAND 1 produces a high output and since the $\overline{Q}$ output is high the NAND 2 produces a low output. Thus it is understood the outputs remain unchanged.

Truth Table:

S	R	Q_{n+1}
0	0	Not used
0	1	0
1	0	1
1	1	$\overline{Q_1}$

RS Flip-Flop Using NOR Gates The NOR gates give a low output when there is a high input in any of its input terminals. Thus a NOR gate is disabled when there is a high input.

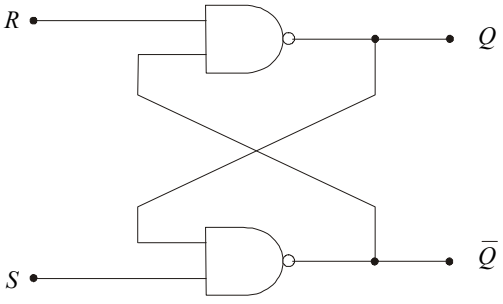


Fig. 5.46

1. $R = 0$, $S = 0$: When both the inputs are high the output of the gates are determined by the state of the outputs. If $Q = 0$ and $\overline{Q} = 1$ then the NOR 1 gets a '1' at its input and its output is '0'. The NOR 2 gets 0 at both its inputs and its output is '1'. Thus it is clear that the output remains unchanged.
2. $R = 0$, $S = 1$: Since $S = 1$, NOR 2 gives '0' as output. Hence the NOR 1 gets '0' at both its inputs and its output is '1'. Thus the flip-flop is set when the set input is high.
3. $R = 1$, $S = 0$: Since $R = 1$, the output of NOR 1 is low. The inputs to NOR 2 are low and hence its output is high. Thus when the reset input is high the flip-flop is reset to '0'.
4. $R = 1$, $S = 1$: Since both the inputs are high irrespective of the state of the outputs the NOR gate outputs are low, which is an undefined state since Q and $\overline{Q}$ cannot be the same.

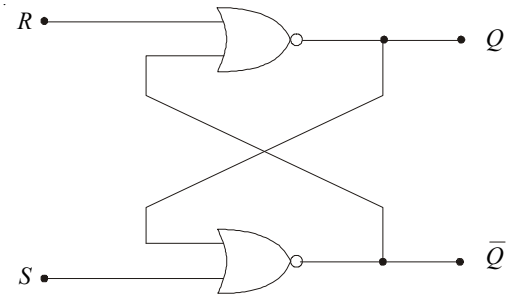


Fig. 5.47

Truth Table:

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Not used

Clocked RS Flip-Flop In this type, the F/F operates only when both the clock input and *RS* inputs are present simultaneously. Consider the *RS* F/F using NOR gates. The clock is passed

through an AND gate. The logic of an AND gate is that it produces a high output only when all its inputs are high and even if one of its input is low the output will be low. Hence to enable the AND gate, the clock input has to be high. When the clock input is low the output of both the AND gates is low which leaves S and R inputs low and hence the F/F output remains unchanged. When the clock input is high the AND gates are enabled and the AND gates responds to the *S* and *R* inputs. Depending on the state of *R* and *S* inputs the F/F is either set or reset as discussed above.

For the FF using NAND gates, the clock is passed through the NAND gate and the gate is enabled when the clock input is high. Allow at the input of the NAND gate gives a high at the output and the state of the F/F remains unchanged. With clock input being high, the NAND gates respond to the *R* and *S* inputs and perform the normal *RS* F/F operation.

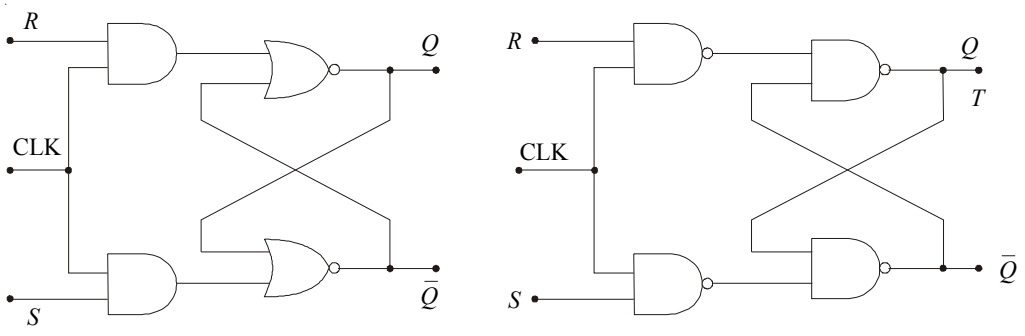


Fig. 5.48

5.12.2 JK Flip-Flop

The JK F/F has two inputs J and K apart from the clock input. It can be realized using clocked RS F/F. Here the state of the F/F is determined by the clock inputs and the previous state outputs.

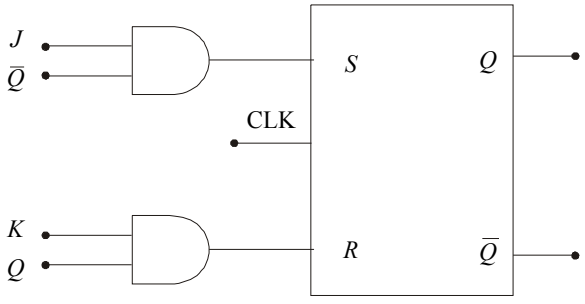


Fig. 5.49

JK FF Using NOR Gates Consider a clocked RS F/F circuit. The circuit is enabled when the clock is high. When $J = 0$, $K = 0$, the output of AND gate 1 and 2 is zero and hence the state of the F/F remains unchanged since $S = 0$ and $R = 0$.

When $J = 0$, $K = 1$: Here the output of the AND 2 gate is zero and the output of the AND 1 gate is '0' or '1' depending on whether Q is 0 or 1. If $Q = 0$, the state of the F/F is unchanged. If $Q = 1$ the output of AND 1 is '1' and hence $S = 0$ and $R = 1$ which resets the F/F.

When $J = 1$, $K = 0$: Here the output of the AND 1 is 0 and AND 2 is '0' or '1' depending on the state of $\overline{Q}$. If $\overline{Q}$ is '0' then $S = 0$, $R = 0$ and the output is unchanged. If $\overline{Q} = 1$ then AND 2 gives '1' as output and the F/F is set to '1' since $S = 1$, $R = 0$.

When $J = 1$, $K = 1$: Here the AND gate outputs depend on the state of Q and $\overline{Q}$. If $Q = 0$ the output of AND 1 is '0' and the output of AND 2 is '1'. Hence the F/F is set to '1'. If $Q =$ 1 the AND 1 gives '1' and AND 2 gives '0' thereby resetting the F/F. Thus it is clear that the output gets complemented when both the inputs are high. This condition is defined as toggle condition.

JK Flip-Flop Using NAND Gates Consider the circuit given below. Here there are two inputs clear and preset, which are defined as direct or asynchronous inputs since they change the state of the FF irrespective of the state of the inputs. Assume the clock input is '0' and hence the output of the NAND gates 1,2 is high. Let PR = 0 and CLR = 1. The NAND gate 3 has a high output and the output of NAND 4 is low since all its inputs are high. Thus the output of the F/F is set to high. When PR = 1, CLR = 0, then the output of NAND 3 is low and the output of NAND 4 is high. Thus the state of the F/F is set to low or the F/F is cleared. Thus these inputs are capable of changing the state of the F/F with the clock = 0 and $J, K = X$. ($X =$ any arbitrary input).

To enable the operation of the F/F both PR and CLR should be high. With PR = 1, CLR = 1,CLK = 1 the circuit functions as a normal *JK* F/F satisfying the below truth table.

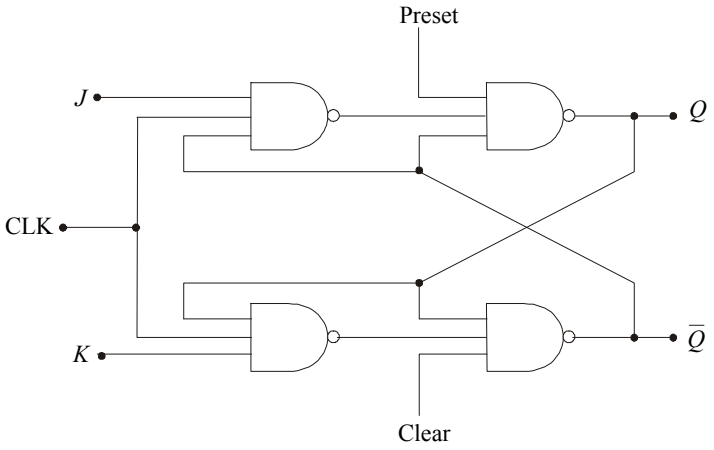


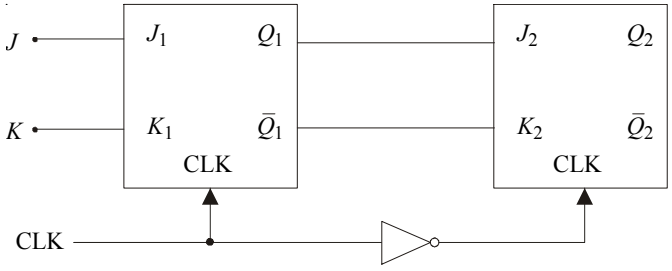
Fig. 5.50

Truth Table:

Clock	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$(\overline{Q}_n)$

Master-Slave Flip-Flop A Master-Slave F/F is constructed from two F/F, where the first F/F serves as the master and the second one serves as the slave. In this circuit, the F/Fs are not operated at the same time. The clock pulse is inverted before being sent to the slave F/F so that the master F/F is operated for the +ve clock pulse and the slave FF is operated for the –ve clock pulse. To start with, PR = 1, CLR = 1, CLK = 1. Hence depending on the state of the inputs the master F/F changes state, while the slave F/F is disabled since its clock input is low. When the clock pulse is low the master F/F is disabled while the slave F/F is enabled and it responds to

Q and $\overline{Q}$ of the master F/F. Thus the data at the input is transferred to the output after two clock pulses. During this transition even if there is a change in the data input it would not affect the output as the master F/F is disabled.



Master-slave JK flip-flop

Fig. 5.51

5.12.3 D or Delay Flip-Flop

On analyzing the above F/F operation it is clear that there is a change in the state of the F/F only when both the inputs are dissimilar. Hence a circuit was designed with a single source and an inverter in between to perform the circuit operation. This resulted in a *D* F/F, which has one input and the data at the input is transferred to the output after receiving the clock pulse. Since a clock pulse delays the data transfer, the F/F is also known as delay F/F. The *D* F/F can be realized using an *RS* F/F with an inverter in between the inputs. Consider the circuit given below. The *D* input goes directly to the *S* input and its complement goes to the *R* input. When the clock input is low the F/F remains disabled. When the clock input is high, the data at the *D* input is transferred to the output. When *D* is 0, $S = 0$ and $R = 1$ and the F/F is reset to 0. When $D = 1$, $S = 1$ and $R = 0$ and the F/F is set to '1'. Thus it is clear that the data is transferred to the output provided the clock is high.

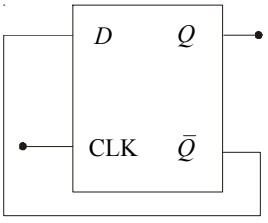


Fig. 5.52

Truth Table:

Clock	D	Q_{n+1}
0	X	Q_n
1	1	1
1	0	0

5.12.4 T or Toggle Flip-Flop

The *T* F/F produces a complementary output on receiving a clock pulse. It can be realized using a *JK*, *RS*, and *D* F/F along with some external hardware.

Consider the circuit shown in Fig. 5.52 in which a *JK* F/F is used. Here the *J* and *K* inputs are tied together and kept at logical high and so it is in toggle mode. On receiving a clock pulse the F/F toggles and gives a complementary output.

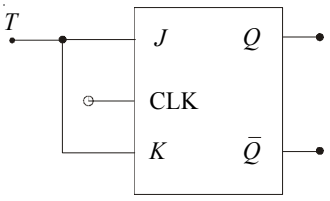


Fig. 5.53

Consider the circuit shown in Fig. 5.53 where an *RS* F/F is used. Here the Q and $\bar{Q}$ inputs are tied to *R* and *S* inputs respectively. Assume $Q = 0$, $\bar{Q} = 1$, then $R = 0$ and $S = 1$ and so the F/F sets to '1'. If $Q = 1$ and $\bar{Q} = 0$, then $S = 0$ and $R = 1$. Hence the F/F resets to '0'. Thus the F/F keeps toggling for every clock pulse.

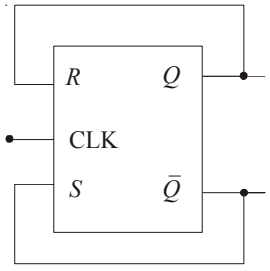


Fig. 5.54

Consider the circuit shown in Fig. 5.54. Here the inputs are passed via an AND gate along with the clock input and *T* input. If clock = 1, $T = 1$, then the circuit follows the above circuit operation.

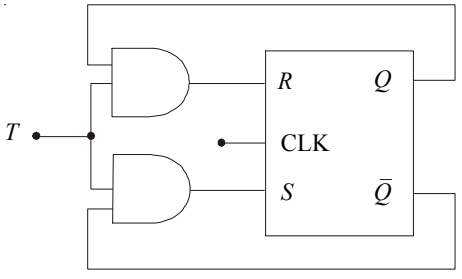


Fig. 5.55

Consider the circuit shown in Fig. 5.55. Here a *D* FF is used and the *D* input is connected to. If $Q = 0$, $\bar{Q} = 1$ then the D input gets '1' as input and on receiving a clock pulse it passes it to the output, thus complementing it. If $Q = 1$, $\bar{Q} = 0$ then *D* gets '0' as the input and the output is '0'.

Consider the circuit shown in Fig. 5.56. In this the input is connected to *D* via an AND gate along with the *T* input. If $T = 1$ and clock is '1' then it functions as the above circuit.

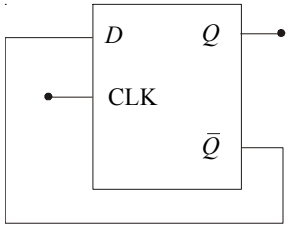


Fig. 5.56

Truth Table:

Clock	T	Q_n	Q_{n+1}
0	X	Q_n	Q_n
1	1	0	1
1	1	1	0

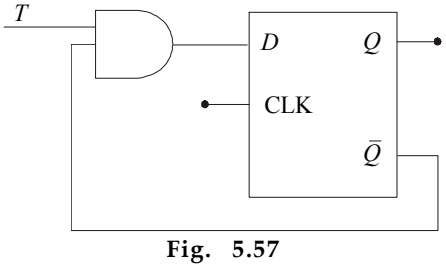


Fig. 5.57

Experiment (Study of Flip-Flop)

Aim: ***To Study the Operation of the Following Flip-Flop and Verify Their Truth Table***

1. SR flip-flop
2. JK flip-flop
3. D flip-flop
4. T flip-flop

Equipments Required:

Equipment	Quantity
Digital IC trainer kit	1
Chords	20

Components Required:

Complements	Quantity
IC 74LS00	1
IC 74LS02	1
IC 74LS73	1
IC 74LS74	1

Circuit Diagram:

SR flip-flop using NOR and NAND gates:

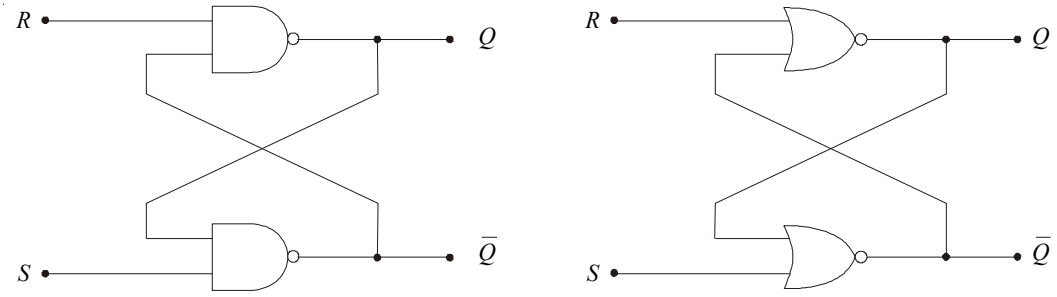


Fig. 5.58

JK flip-flop:

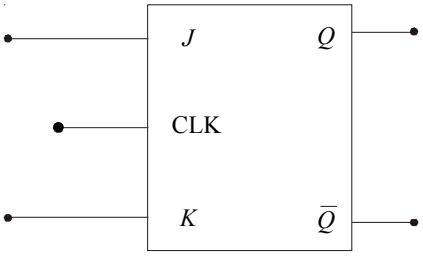


Fig. 5.59

D flip-flop and D-F/F using JK-F/F

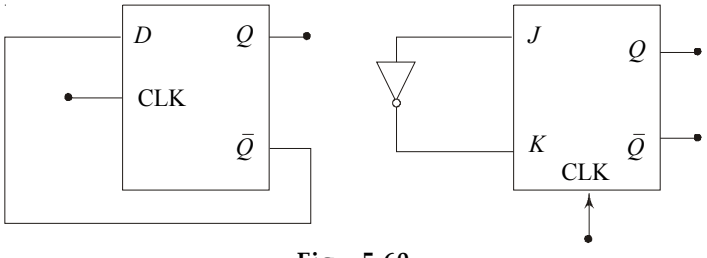


Fig. 5.60

T flip-flop: using D-F/F and JK-F/F

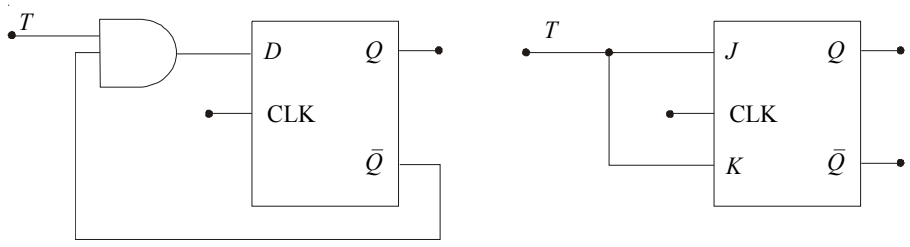


Fig. 5.61

Procedure:

1. Connect the IC as per the configuration.
2. Give the inputs as per the truth table and verify the outputs.
3. Verify it for all the flip-flops and then realize the same using logic gates.

Truth Table:

SR flip-flop (using NAND gate):

Clock	S	R	Q_{n+1}
↑	0	0	Unused
↑	0	1	1
↑	1	0	0
↑	1	1	Q_n

SR flip-flop (using NOR gate):

Clock	S	R	Q_{n+1}
↑	0	0	Q_n
↑	0	1	0
↑	1	0	1
↑	1	1	Not used

JK flip-flop:

Clock	J	K	Q_{n+1}
↑	0	0	Q_n
↑	0	1	0
↑	1	0	1
↑	1	1	$(\overline{Q_n})$

D flip-flop:

Clock	D	Q_{n+1}
↑	0	0
↑	1	1

T- flip-flop:

Clock	T	Q_{n+1}
↑	0	1
↑	1	0

Result:

The operations of the flip-flops are studied and their truth tables are verified.

Exercises:

1. Define *race around* condition.
2. Explain how *race around* condition is overcome in a master-slave flip-flop.
3. Realize T flip-flop using other flip-flops.

5.13 SHIFT-REGISTERS

A flip-flop is a one-bit register, which stores either a '0' or '1'. A shift register is an array of flip-flops which shifts data in a particular sequence and direction in response to a clock pulse. The shift register takes in the data either serially or parallelly and sends out the data either serially or parallelly. When it operates in the serial mode, it has the advantage of less hardware and disadvantage of large execution time. When operated in the parallel mode, the hardware required is more, while the execution time is less. The shift registers are another important building block of a digital system. It is used in temporary data storage, digital delay line, sequence generator, ring counter, recirculating memory, etc. Shift registers are available in both bipolar and MOS forms.

Bipolar Shift Register The shift register shifts data from one register to another on applying a clock pulse. The data can be taken either serially, i.e., one at a time or parallelly, i.e., all at the same time. Similarly, the data can be taken out either serially or parallelly. Based on these concepts the shift register can be operated in the following modes:

1. Serial in serial out.
2. Serial in parallel out.
3. Parallel in serial out.
4. Parallel in parallel out.

The data in the shift register can be shifted to the right or left and accordingly it is called right shift or left shift register. Now let us consider the circuit, which shows a universal shift register that can be operated in all the four modes.

5.13.1 Serial in Parallel Out

Clear all the F/Fs by making the clear input as '0'. Make $P_r = C_r = 1$. The serial data is entered into the F/F4 and the data is transferred to the successive stages for every clock pulse. Let the data be 1101. For the first clock the output Q_4 is '1' and the outputs of all the other F/Fs are '0'. For the second clock the second data '0' enters F/F4 and the first data is shifted to the F/F3. Likewise the shifting proceeds and after the fourth clock all the data's are available at the output.

Clock	Data	Q_4	Q_3	Q_2	Q_1
0	–	0	0	0	0
1	1	1	0	0	0
2	0	0	1	0	0
3	1	1	0	1	0
4	1	1	1	0	1

5.13.2 Serial in Serial Out

The data enters the F/Fs as explained above but they are read serially and hence it requires four more pulses to make the data available at the output of F/F1.

Clock	Data	Q_1
1	1	0
2	0	0
3	1	0
4	1	1
5	–	0
6	–	1
7	–	1

It is clear from the above table that only at the end of the fifth pulse the data is available at the output of the F/F1 and so the full data will be available only at the end of the eighth clock.

5.13.3 Parallel in Serial Out

The F/Fs are all cleared and the output of all the F/Fs are zero. The data is fed to the preset inputs through an NAND gate whose other input is preset enable, which is kept high. The least significant bit is fed to the F/F4 and the MSB is fed to the F/F1. After feeding the data the preset is disabled by making the preset enable terminal low. The data is shifted serially by giving a series of pulses as discussed in the paragraph.

5.13.4 Parallel in Parallel Out

The data is entered parallelly as discussed above. The data is available at the outputs immediately and it is read. Thus the data can be entered parallelly.

5.13.5 Right/Left Shift Register

In this the data can be either shifted to the right or to the left. If M is high the AND 1 is enabled and the AND 2 is disabled and so the data DR enters F/F1 and it is shifted to the left for every clock pulse. When $\overline{M} = 1$ the AND 2 is enabled and AND 1 is disabled and so the data DL enters F/F4 and the data is shifted to the right towards F/F1 for every clock pulse. Thus the data can be shifted to the right or left depending on the control bit M.

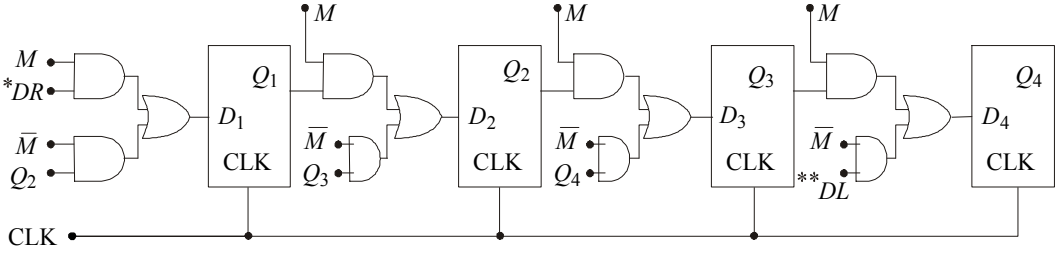


Fig. 5.62

* *DR*: Data Right
** *DL*: Data Left

MOS Shift Registers The MOS shift registers are of two types; static and dynamic. The static shift registers uses F/Fs and operates similar to the bipolar *SR*. The dynamic *SR* stores the each bit as a charge in the gate capacitance of the MOSFET and it is transferred to the next

stage through inverters or through a series connected MOSFET, which acts as a transmission gate. Appropriate clock pulses turn ON the inverters or the transmission gates. Since the data is stored as a charge the requirement of frequent replenishing of the charges is a must in case of a dynamic *SR*.

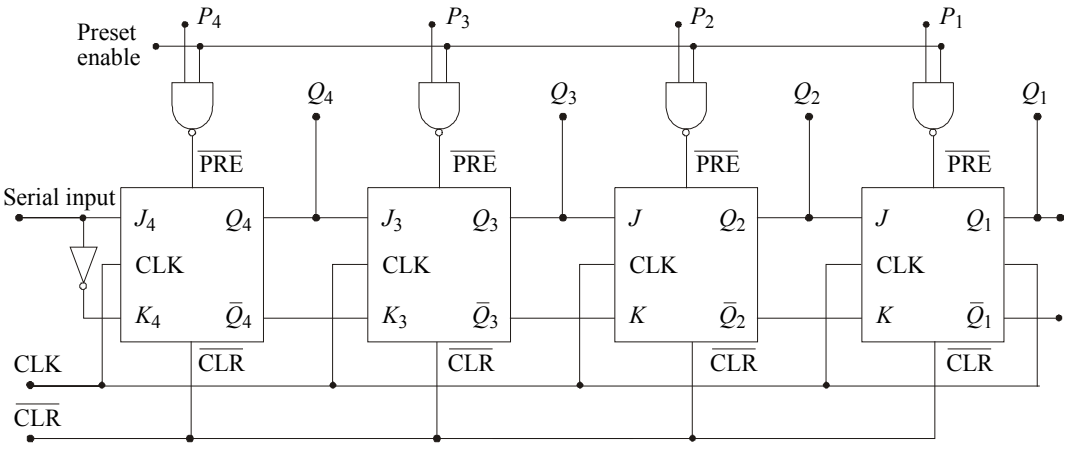


Fig. 5.63

5.14 BBD AND CCD REGISTERS

The BBD (Bucket Brigade Device) and CCD (Charge Coupled Device) are charge transfer devices useful as delay lines and shift registers. The BBDs consist of a series of MOSFETS connected along with capacitors at their nodes. Sampled values of the i/p signals are stored as charge on the capacitors and can be transferred from one stage to the other by controlling the switches using a clock train. The CCD is a three layer MOS structure making use of the creation, storage and transfer of minority carriers in potential wells near the semiconductor surface. Hence the CCDs have a higher packing density and lower power dissipation than BBDs. Moreover the CCD structure enables higher transfer efficiency than BBD making it possible to realize devices with a very high storage capacity in a single package.

BBD This consists of MOSFETs in series with capacitors across their gate-drain terminals. The input signal charges the capacitance at the output of the first MOSFET when a clock '0' turns it on. When '0' is high the drain terminal of the first MOSFET reaches V. The input signal V_i is present across the source to ground parasitic capacitance of the first MOSFET. Hence this capacitance charges from V_i to V when '0' is ON. The charge transfer from drain to source here is $Q = C\,(V - V_i)$ which leaves a voltage $V_i = [(V - (Q/C)]$ across the output capacitance of this MOSFET at the end of '0'. Thus V_i is transferred from the input to the output of the first stage. This is further transferred to the next capacitor at the second MOSFET output terminals at the end of clock input '0'. As the MOSFETs used here are of enhancement type and are worked as voltage followers there is finite transfer efficiency for each stage which limits the length of the BBD shift register. The efficiency can be improved by using amplifiers after every 10 or 15 stages.

CCD The CCD consists of an array of closely spaced metal electrodes that overlay an insulator deposited on a uniformly doped semiconductor substrate, either *n*- or *p*-type. The substrate

considered here is of *n*-type and the insulator is silicon dioxide. A high negative potential is applied to the electrodes with respect to the substrate and a depletion layer is formed near the substrate for a short duration. Thermally generated carriers later on occupy this region. The distribution of the depletion layer is continuous and its depth depends on the potential applied to the electrodes. Minority carriers are injected into the semiconductor surface following either of the methods to be discussed below and the charges gets collected in the region of minimum potential. This condition is known as storage condition. When the adjacent electrode is given a higher potential then the charge shifts to the next minimum potential region. Thus the charges are shifted within the semiconductor by creating a potential well and at the end of the semiconductor it is collected by either of the methods discussed below.

Input Scheme:

1. When a large pulse is given to the electrode it results in avalanche breakdown and fixed amount of charges are induced into the potential well. This scheme is used for digital shift registers CCDs. It requires either a high-applied voltage or the oxide layer used should be thin.
2. A *p*-layer is diffused and a *p-n* junction is created between the layer and the substrate. This junction results in a minority current, which results in accumulation of charge carriers below the next electrode, which is biased to produce a potential well. Here the charges produced depend on the applied voltage and hence this CCD can handle analog signals also.
3. In this method, the charge carriers are induced optically. Here an array of *p-n* junction diodes along with MOSFETs is used. The minority carriers drift towards the $Si\backslash SiO_2$ interface and get stored in the potential well until they are transferred to the other regions. As the charge generated is directly proportional to the optical intensity impinging on the photodiode at any location, the register forms the basis for the CCD image sensors.

Output Schemes:

1. A resistor is connected to the substrate and when the charge gets collected at the last electrode a +ve voltage causes holes to be injected into the substrate which passes a proportional current through the resistor.
2. A diode is diffused at the end of the CCD and held at the highest –ve potential. When charge enters the diode location an output current is produced at the output circuit.
3. A MOS structure is diffused and when the charge enters this region the MOS capacitor charges and the resulting output voltage gives the amount of charge.

Experiment (Study of Shift Registers)

Aim: ***To Construct and Study the Operation of a 4 Bit Shift Register in the Following Modes***

1. Serial in serial out
2. Serial in parallel out
3. Parallel in Serial out
4. Parallel in parallel out

Equipments Required:

Equipments	Quantity
Digital IC trainer kit	1
Patch Chords	20
Pulse generator	1

Components Required:

Component	Quantity
IC 74LS00	1
IC 74LS74	1

Circuit Diagram:

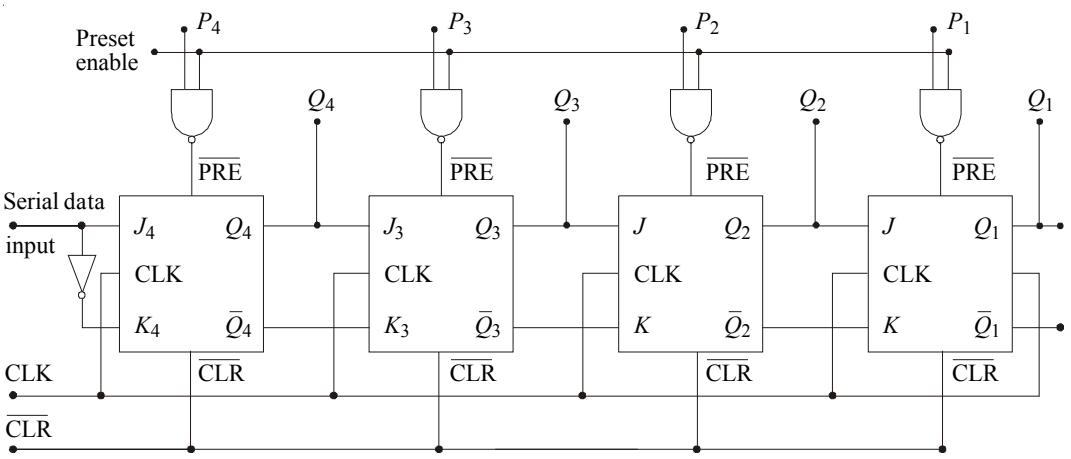


Fig. 5.64

Procedure:

(a) Serial Mode:

1. Connect the circuit as per the circuit diagram and pin configuration of the ICs.
2. Clear all the flip-flops by applying a low signal to the clear input.
3. Feed the data into the serial input one bit per clock pulse.
4. Observe the output at Q_0, if the output is taken serially.
5. Observe the output at Q_0, Q_1, Q_2, Q_3, if the output is taken parallelly.

(b) Parallel in Parallel Out:

1. Connect the circuit as per the diagram and pin configuration of the ICs.
2. Clear all the flip-flops by applying a low signal to the clear input.
3. Make the serial input low.
4. Enable the preset and clock by applying a high signal.
5. Feed in the data at P_0, P_1, P_2, and P_3.
6. Observe the outputs at Q_0, Q_1, Q_2, and Q_3.

(c) Parallel in Serial Out:

1. Repeat the above steps till point No. 5.
2. Disable the present input by connecting it to a low signal.
3. Apply clock pulses to obtain data serially at Q_0.

Tabular Column:

Serial Mode:

Mode of Operation	Clock	Serial Input	Q_4	Q_3	Q_2	Q_1
Serial in serial out	0	0	0	0	0	0
	1	1	1	0	0	0
	2	0	0	1	0	0
	3	0	0	0	1	0
	4	0	0	0	0	1
Serial in parallel out	0	0	0	0	0	0
	1	1	1	0	0	0
	2	1	1	1	0	0
	3	1	1	1	1	0
	4	1	1	1	1	1

Parallel Mode:

Mode of Operation	Clock	P_4	P_3	P_2	P_1	Q_4	Q_3	Q_2	Q_1
Parallel in parallel out	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	0	0	0	1
	2	0	0	0	0	0	1	1	1
	3	0	0	0	0	0	0	1	1
	4	0	0	0	0	0	0	0	1
	5	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1	1
	2	1	0	1	0	1	0	1	0
	3	0	1	1	0	0	1	1	0

Result:

The operations of the shift registers are studied for all the modes of operation.

Exercises:

1. Discuss about synchronous and asynchronous modes of operation.
2. What is a universal shift register? Explain its operation with a neat circuit.
3. Study the shift register using IC 5499 (parallel in parallel out).
4. Study the shift register using IC 7491 (serial in serial out).

5.15 COUNTERS

A sequential circuit that goes through a prescribed sequence of states on applying the input pulses is called a *counter*. The input pulses called the count pulses may be clock pulses or they may originate from an external source and may occur at prescribed intervals of time or at random. In a counter, the sequence of states may follow a binary count or any other sequence of states. The binary sequence is the most straightforward one and the simplest one and the

counter is called the binary counter. The counter is constructed using flip-flops connected in cascade. The counters in general can be classified as *synchronous* and *asynchronous*.

In the synchronous type, the clock pulse is common to all the F/Fs while in the asynchronous type the clock input is given from the output of the previous FF. The asynchronous type is also known as ripple counter.

Note: H: +5V (High state) L : 0V (Low state)

5.15.1 Asynchronous or Ripple Counters

The ripple counter is the simplest of all counters and it comprises of *n* F/Fs for providing a count of 2. Such a counter is also called a modulo 2 counter.

Mod-2 Counter Consider the given F/F in which the *JK* inputs are held high so that the F/F is operated in the toggle mode, i.e., the output of the F/F complements for every clock pulse. The count is taken to be the number of clock pulses allowed before the F/Fs reset back to their original state. The Mod 2 type is the simplest one. To start with, the o/p of the F/F is '0'. When the first clock pulse is given the FF toggles and the output is '1'. For the next pulse the F/F toggles again and the F/F is reset to the original value. Thus the counter has a maximum count of two clock pulses.

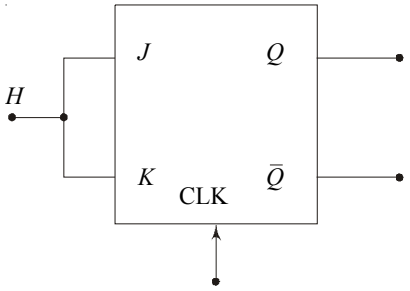


Fig. 5.65

Mod-4 Counter To count 4 pulses we require two F/Fs. To start with, the output of both F/Fs are 00. For the first pulse the F/F1 toggles and its output goes from '0' to '1'. The output of the first F/F is given as the clock to the second F/F and the F/Fs are designed to change state for a –ve pulse, i.e., when the output goes from high to low. Since the o/p goes from low to high the clock is positive and there is no change in the state of the second F/F. The o/p of the F/Fs is 01. For the second pulse, the F/F1 toggles again and the output goes from high to low thereby

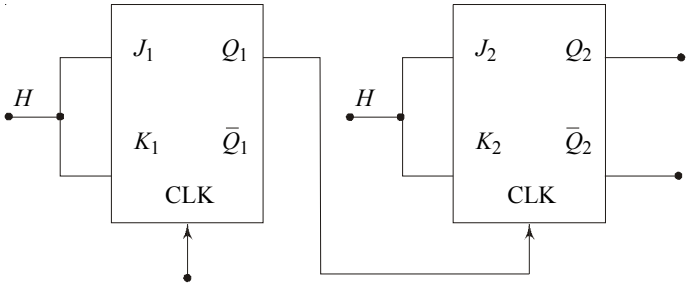


Fig. 5.66

providing a clock pulse to the F/F2. Hence the F/F2 toggles taking its output high. Thus the output of the F/Fs will be 10. For the third pulse the F/F1 toggles taking its output to high and this provides a –ve pulse to F/F2 and so there is no change in it and hence the output is 11. For the fourth pulse the F/F1 toggles and the output goes low. This provides a +ve pulse to the F/F2 and it toggles thereby taking the output to low. Thus both the F/Fs come back to their original states and the count is four.

Clock	Q_2	Q_1
0	0	0
1	0	1
2	1	0
3	1	1
4	0	0

This can be extended to any number of counts and it is clear that the first F/F changes state for every clock pulse and the second F/F changes state for every two clock pulses, the third one for every four clock pulses, the fourth one for every eight clock pulses and so on. In all these counters, the count goes up to the maximum and the F/Fs reset to '0'. There are certain counters in which the count can be stopped at an intermediate count by resetting the F/Fs to '0'. Giving a feedback through external circuitry does this.

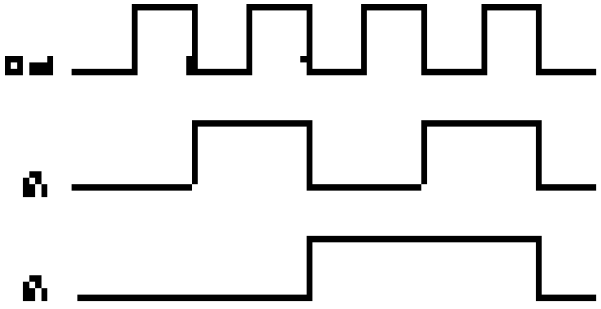


Fig. 5.67

Mod-3 Counter: Consider the circuit of a Mod-3 counter in which F/F1 and F/F2 are connected in the synchronous mode, i.e., they have a common clock. J_1 is connected to $\overline{Q_2}$ and J_2 is connected to Q_1. Both K_1 and K_2 are connected to high. To start with Q_1 and Q_2 are '0', hence $\overline{Q_2}$ is '1' and so J_1 is '1', while J_2 is '0'. When the first clock is given the F/F1 toggles and F/F2 does not undergo any change. The outputs are $Q_1 = 1$ and $Q_2 = 0$. Therefore both J_1 and J_2 are high and for the next clock both F/F1 and 2 toggle taking Q_1 to '0' and Q_2 to '1'. Now J_1 and J_2 are low and so for the third pulse the outputs are 00, i.e., the F/Fs reset. Thus the count is terminated for three clock pulses.

Clock	Q_2	Q_1
0	0	0
1	0	1
2	1	0
3	1	0

Mod*-5 *Counter In this there are three F/Fs out of which F/F1 and F/F3 are given a common clock and F/F2 gets the clock from the output of F/F1. Here, J_1 is connected to $\overline{Q}_3$ and J_3 is connected to the output of an AND gate whose inputs are Q_1 and Q_2. So only if both Q_1 and Q_2 are high there will be a change in the F/F3. J_2 and K_2 are tied together to high. K_1 and K_3 are also kept high. F/F1 and F/F3 will change state simultaneously for the clock, while F/F2 changes state when the output of the F/F1 goes from '1' to '0'. To start with, all the outputs are zero. Therefore the output $\overline{Q}_3$ is high and hence J_1 is high. For the first clock the F/F1 changes state from '0 'to '1'. This gives a +ve pulse to F/F2 and so there is no change. J_3 is 0 and so F/F3 has no change. For the second clock F/F1 toggles and the output goes from '1' to '0' thereby providing a –ve trigger for F/F2 and F/F2 toggles and its output is '1'. F/F3 does not undergo any change, as its input is '0'. For the third clock the F/F1 toggles from '0' to '1'. F/F2 and F/F3 undergo no change. For the fourth clock F/F1 and F/F3 toggle. Since F/F1 goes from '1' to '0', F/F2 also toggles and goes to '0'. F/F3 has undergone a change for the first time and its output is high. Since Q_3 is high $\overline{Q}_3$ is low and the input to J_1 is low. Q_1 is '1' but Q_2 is '0', so the output of the AND gate is low and so J_3 is '0'. Hence for the fifth clock F/F1 and F/F3 reset to '0' thereby terminating the count.

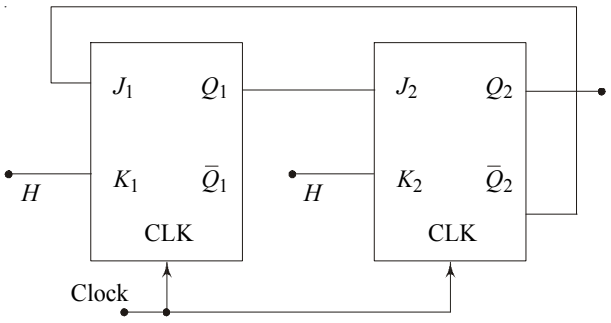


Fig. 5.68

Clock	Q_3	Q_2	Q_1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	0	0	0

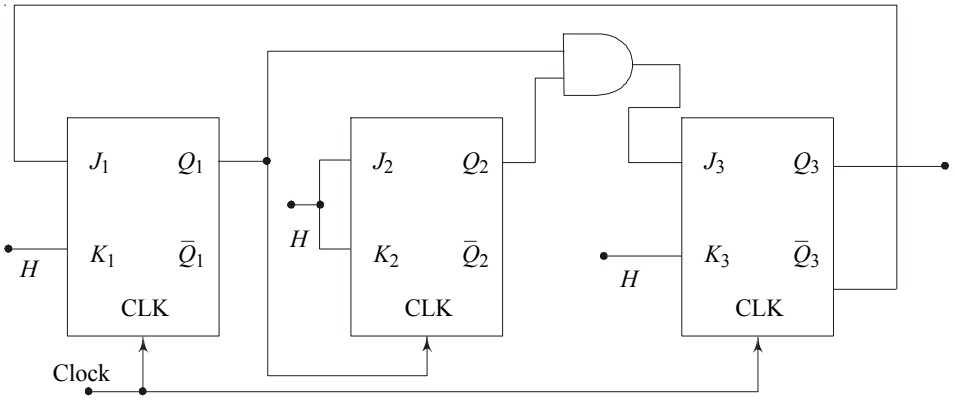


Fig. 5.69

Mod*-8 *Counter

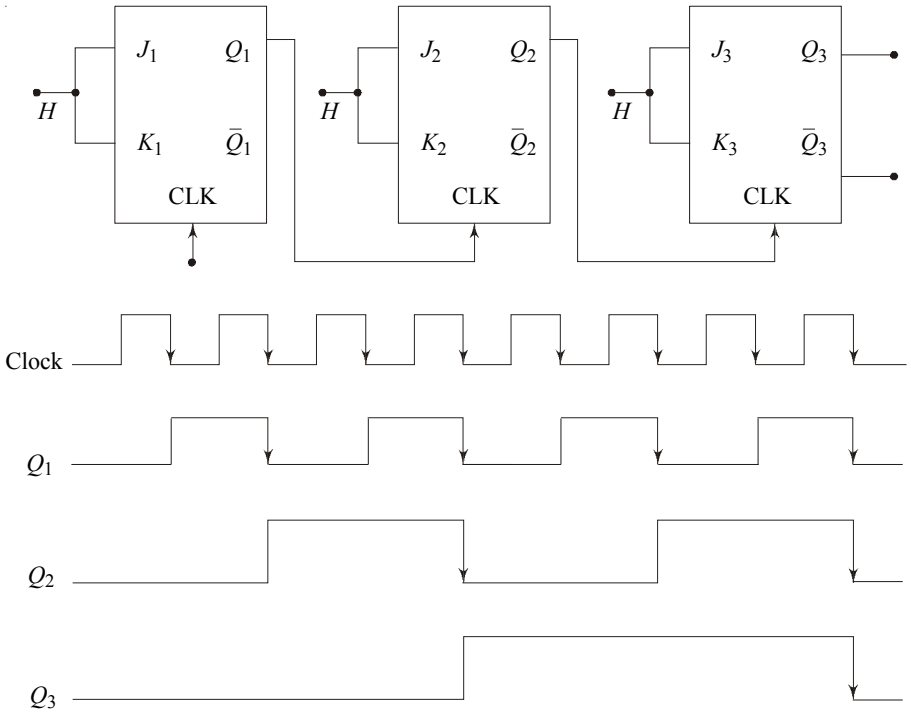


Fig. 5.70

Mod*-10 *Counter The Mod-10 counter or the decade counter is the most frequently used one. It can be implemented in different ways of which we will discuss a few. Mod-2 followed by Mod-5. Here the Mod-2 counter acts as the clock to Mod-5 counter. The Mod-5 counter changes state whenever the output of the Mod-2 counter goes from '1' to '0'. Here there are 4 F/Fs, F/F1 to F/F4. F/F1 changes state for every clock and F/F2 changes state whenever Q_1 changes state from '1' to '0'. F/F3 changes state when Q_2 goes from '1' to '0'. F/F4 undergoes a transition when both Q_2 and Q_3 are high. To start with, all the F/Fs are cleared. For the first pulse Q_1 is '1' while the other outputs remain the same. For the second pulse the output Q_1 is '0' which enables F/F2 and Q_2 goes to '1'. For the third pulse Q_1 is '1' and the other outputs remain unchanged. For the fourth pulse Q_1 is '0' and so F/F2 changes state, i.e., Q_2 is '0' and so F/F3 gets the clock and toggles making Q_3 '1'. For the fifth pulse Q_1 is '1' and the other outputs remain the same. During the sixth pulse F/F1and F/F2 toggle to make $Q_1 = 0$ and $Q_2 = 1$. For the seventh pulse F/F1 toggles to give $Q_1 = 1$ while others are unchanged. During the eighth pulse F/F1-F/F4 toggle giving Q_1 to $Q_3 = 0$ and $Q_4 = 1$. When $Q_4 = 1$, $\overline{Q}_4 = 0$ and so F/F2 will not undergo any change later. For the ninth pulse Q_1 goes high and other output remain as such. For the tenth pulse Q_1 goes low and thereby provides a clock to F/F4 and it resets to '0'. Thus at the tenth pulse all the F/Fs are cleared and the counter is reset.

Clock	Q_4	Q_3	Q_2	Q_1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

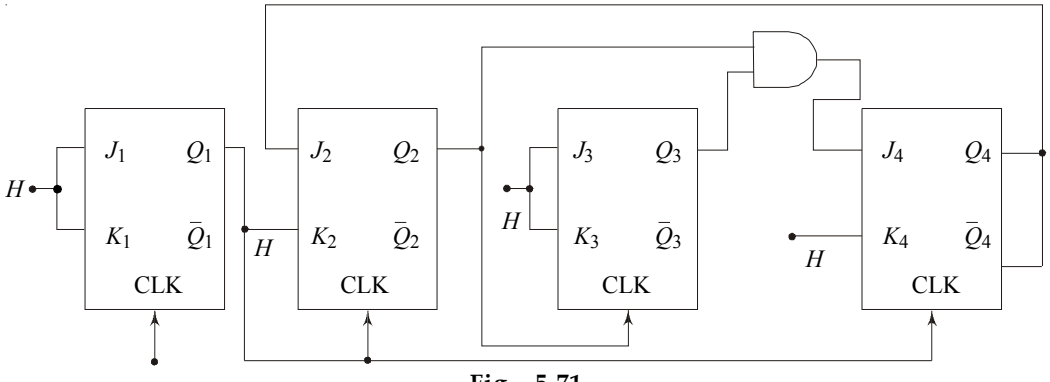
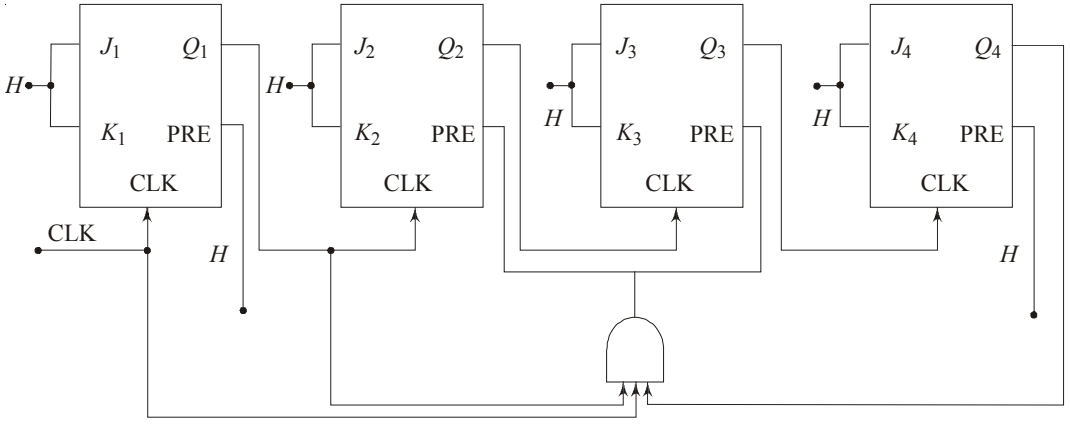


Fig. 5.71

Modulo-10 Counter Using Feedback:



(Contd.)

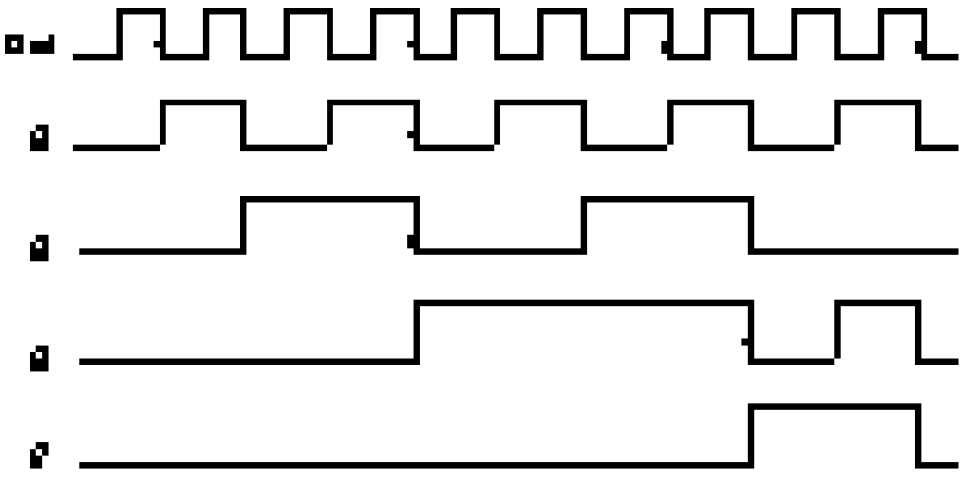


Fig. 5.72

Experiment (Asynchronous Counter)

Aim: ***To Construct Binary and Modulo-n Asynchronous Counter.***

1. Binary Counter (4-BIT)
2. Modulo-11 Counter

Equipment Required:

Equipment	Range	Quantity
Power supply	(0-5) V	1
Pulse generator		1

Circuit Diagram:

Binary Counter:

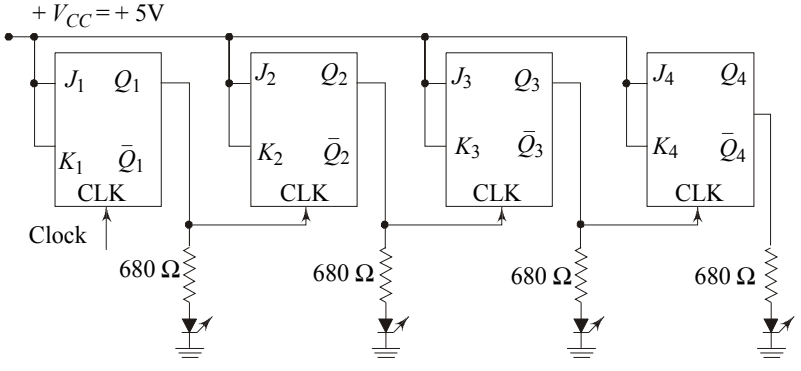


Fig. 5.73

Modulo-11 Counter:

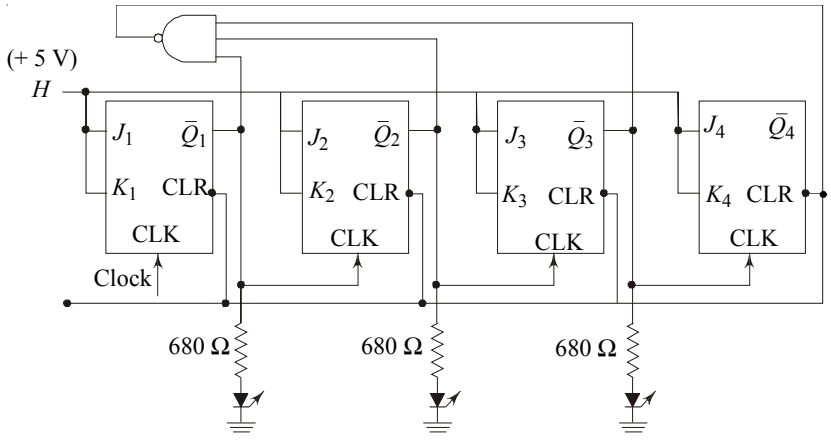


Fig. 5.74

Procedure:

1. Rig up the circuit as per the circuit diagram.
2. Connect the clock input.
3. Observe the output and verify it with its count sequence.

Design Concept:

1. Take the (n +1)th state.
2. Observe the output that are at '1' in the (n +1)th state.
3. Combine all those outputs in an NAND gate and give the output of the gate to clear the terminals of flip-flops.
4. When the (n +1)th state arrives, the output of NAND gate will be zero (low), which will clear all flip-flops.
5. Hence instead of (n + 1)th state, we get the first state (0000).

Count Sequence:

Binary Counter:

Clock	Outputs			
	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16 (0)	0	0	0	0

Modulo-11:

Clock	Outputs			
	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11 (0)	0	0	0	0

Exercises:

1. Design a Mod-9 counter.
2. Design a Mod-5 counter.
3. Design an up-down counter.
4. Study the Decade counter using IC 5490.
5. Study the Binary counter using IC 5493.

5.15.2 Synchronous Counters

Synchronous counters eliminate the cumulative propagation delays of F/Fs, which generally limit the performance of the ripple counters. All the F/Fs in this counter are under the control of the same clock pulse. Therefore the repetition rate is limited only by the propagation delay of one F and the gates. Consider the circuit1 given below. Here there are 4 F/Fs. F/F1 has both its inputs connected to high. F/F2-F/F4 have their inputs tied to the previous outputs. Thus only if the previous outputs are high these F/Fs can toggle when a clock pulse occurs. For e.g., F/F4 can toggle only if $Q_1 - Q_3$ is high. To start with, all the F/Fs are cleared. For the first clock F/F1 toggles while all the other outputs are unaltered. For the second clock both F/F1 and F/F2 toggle. This continues till all the F/F outputs are high. Once this state is reached for the next clocks all the F/Fs reset to '0'. Thus the counter counts upto 1111 and resets to 0000.

Another type of synchronous counter is given in circuit 2. This is a synchronous decade counter which resets after the tenth count. Here the count proceeds in the same manner as mentioned above till the eighth pulse. After the eighth pulse $Q_4 = 1$ and so $\overline{Q}_4 = 0$ and hence $J_2 = K_2 = 0$ irrespective of the state Q_1 and so the output of F/F2 is unaltered. Since Q_2 is low F/F3 has both of its inputs low and hence the output of Q_3 is also unaltered. During the ninth pulse the state of the inputs of all the F/Fs are as follows.

$J_1 = K_1 = 1$, $J_2 = K_2 = 0$, $J_3 = K_3 = 0$, $J_4 = K_4 = 0$. Hence the output of F/F2-F/F4 remains unchanged while the F/F1 alone toggles for the clock pulse. Thus at the end of the ninth pulse the outputs are $Q_1 = 1$, $Q_2 = 0$, $Q_3 = 0$, $Q_4 = 1$. Now the input of the F/F4 is $J_4 = 0$, $K_4 = 1$. For the tenth pulse the F/F1 toggles taking the output to '0' and F/F4 also goes to '0' as the $J_4 = 0$. The other F/Fs remain unchanged, as the inputs are '0'. Thus for the tenth count the F/Fs are reset to '0'.

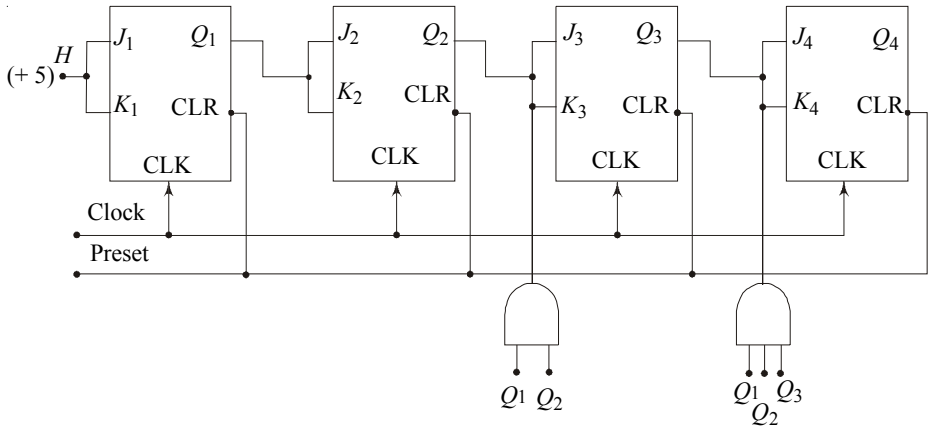


Fig. 5.75

Decade Counter Using Feedback:

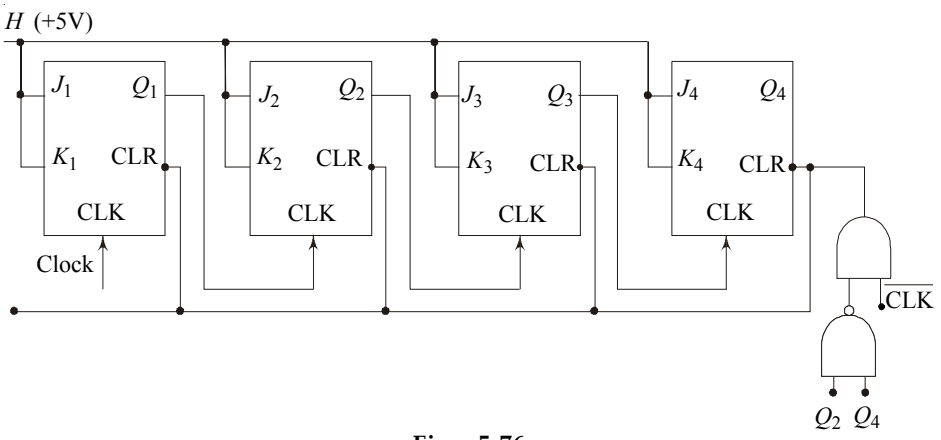


Fig. 5.76

Ring Counter Here the data is being shifted in a cyclic manner. Consider the given circuit in which the clock is common and the clear inputs of F/F2 to F/F4 and the preset input of F/F1are connected to the clear terminal. Thus when the clear input goes low all the F/Fs other than F/F1 are set to '0' while F/F1 are set to '1'. Thus $Q_1 = 1$, $Q_2 = 0$, $Q_3 = 0$, $Q_4 = 0$. Since the outputs of the F/Fs are fed as inputs to the successive F/Fs, after the first clock pulse the output of Q_2 alone is '1' while all the other outputs are '0'. For the second clock pulse Q_3 is '1' and this proceeds in a cyclic manner.

Clock	Q_4	Q_3	Q_2	Q_1
0	0	0	0	1
1	0	0	1	0
2	0	1	0	0
3	1	0	0	0
4	0	0	0	1

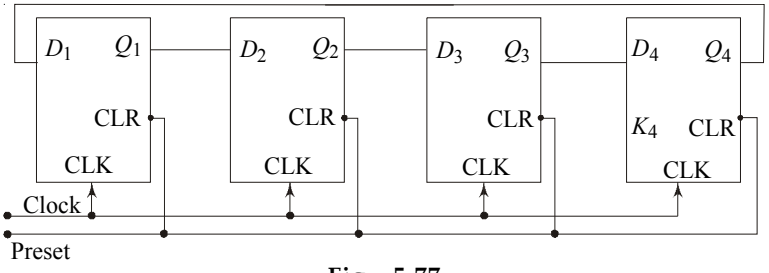


Fig. 5.77

Down Counter The Down counter counts in a descending order. Here the clock is given from the $\overline{Q}$ output of the previous F/F. To start with, $\overline{\text{PRE}}$ is low and the F/Fs are set to '1'. Make $\overline{\text{PRE}}$ high and the counter starts the count. The F/Fs are connected in the toggle mode and hence for the first clock pulse F/F1 toggles and the outputs are low. Correspondingly its $\overline{Q}$ output becomes high and hence the F/F2 does not change as it gets a +ve trigger. F/F3 and F/F4 also do not undergo any change and hence the output is 1110. For the next pulse F/F1 becomes high and $\overline{Q_1}$ becomes low thereby giving a –ve pulse for F/F2. F/F2 toggles and its output becomes low. F/F3 and F/F4 do not undergo any change and the output is 1101. This process continues till the count becomes 0000.

Clock	Q_4	Q_3	Q_2	Q_1
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0
8	0	1	1	1
9	0	1	1	0
10	0	1	0	1
11	0	1	0	0
12	0	0	1	1
13	0	0	1	0
14	0	0	0	1
15	0	0	0	0

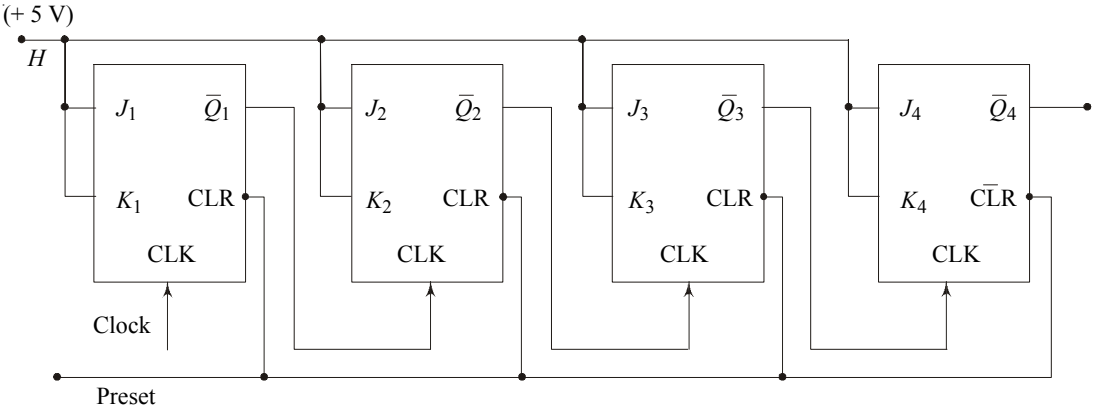


Fig. 5.78

Up-Down Counter The up-down counter can be operated to count both in the ascending and descending order. To have an up count Q is given as a clock pulse to the next F/F. Similarly to have a down count $\overline{Q}$ is given as a clock pulse to the next F/F. A control circuitry is used which passes either Q or $\overline{Q}$ for the counting process. To start with, UP is high so that the count proceeds in the ascending order. Clear all the F/Fs and make the clear input high. Q is passed through the control circuitry and the count proceeds till the output is 1111. If the UP input is made low, $\overline{Q}$ passes through the control circuitry. Make the PRE input low to set the outputs 1111. For the first clock the F/F1 changes state and $Q_1 = 0$, while the other F/Fs remain unchanged. Thus the output is 1110. This proceeds till the output is 0000.

Operation of the Control Circuit The circuit consists of two NAND gates and an OR gate. NAND 1 has Q_1 and UP as inputs. NAND 2 has $\overline{Q_1}$ and as inputs. When UP is high NAND 1 is enabled and Q_1 will be passed. Similarly if UP is low NAND 2 will be enabled and $\overline{Q_1}$ will be passed. The output of the NAND gates is passed through the Bubbled-OR gate whose output is fed to the clock inputs of the F/Fs. For e.g., let UP = 0 and $\overline{\text{CLR}}$ = 1. Then the output is 1111. After the first clock the state is $Q_1 = 0$, $Q_2 = 1$, $Q_3 = 1$, $Q_4 = 1$, i.e., 1110. This continues till the count is 0000. Similarly if UP = 1 and $\overline{\text{CLR}} = 0$, the output is 0000. For the first clock the output is 0001 and this continues till the count is 1111.

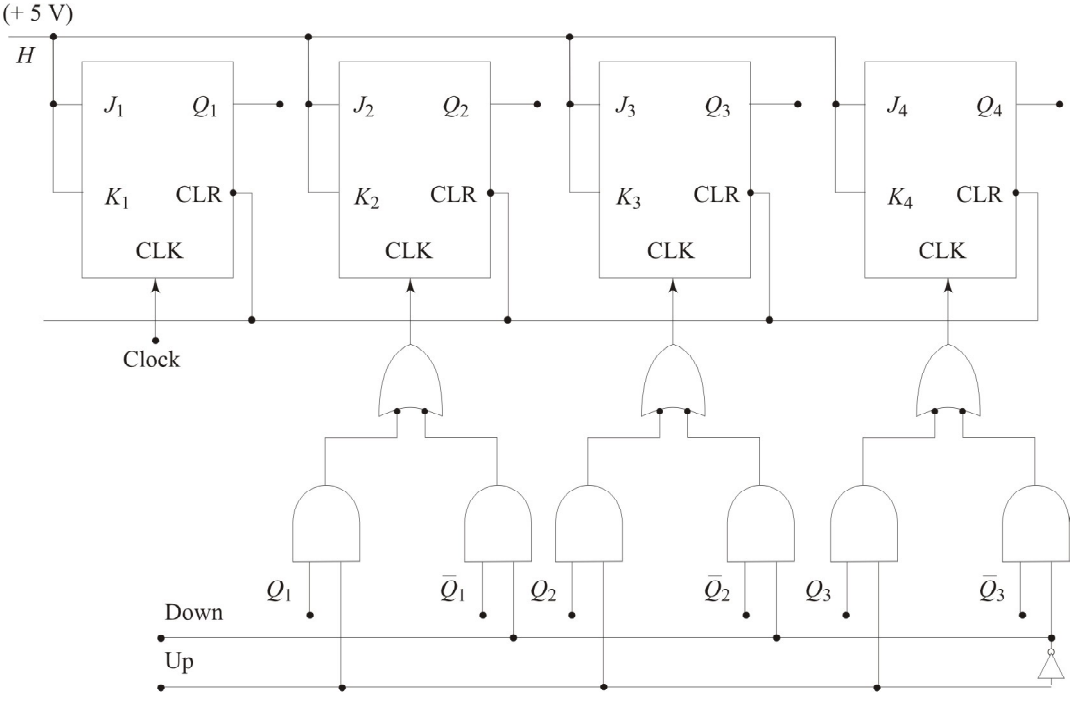


Fig. 5.79

Pre-Settable Counter The pre-settable counter can be set to any initial count and then the count proceeds in the ascending manner when the clock pulses are given. The circuit given is a asynchronous Mod-16 up counter. The initial count can be set to any desired value depending on the inputs $P_1 - P_4$. The inputs $P_1 - P_4$ are fed to the clear and preset inputs through the NAND gates. The NAND 1 gets the input from P_1 and load input. Similarly the NAND 2 gets the load and the complement of P_1 as inputs. When the load signal is high the NAND gates are enabled

and they respond to the input P_1, which is, fed to the CLR and PRE inputs of F/F1. For e.g., if P_1 is '1', the output of NAND1 is low and the output of NAND 2 is high. These outputs are taken to the preset and clear inputs of the F/F where they are inverted again and so PR = 1 and CLR = 0 sets the output of F/F1 to high. Similar analysis holds good for the other F/Fs also and the outputs of all the F/Fs are set to the desired value. For e.g., let $P_1 = 1$, $P_2 = 0$, $P_3 = 0$ and $P_4 = 1$. Then the outputs are 1001 and hence the load signal becomes low and the effect of preset and clear are removed as the output of the NAND gates remain high irrespective of the state of $P_1 - P_4$. The load signal is got from the output of an NOR gate whose inputs are $Q_1 - Q_4$. Once the preset and clear are disabled the circuit starts counting when the clock is applied. Thus the count proceeds, as 1010,1011, etc., till it resets to 0000. When it is 0000 the NOR output is high and the new values of $P_1 - P_4$ can be entered. Thus this counter can be operated starting from any desired value.

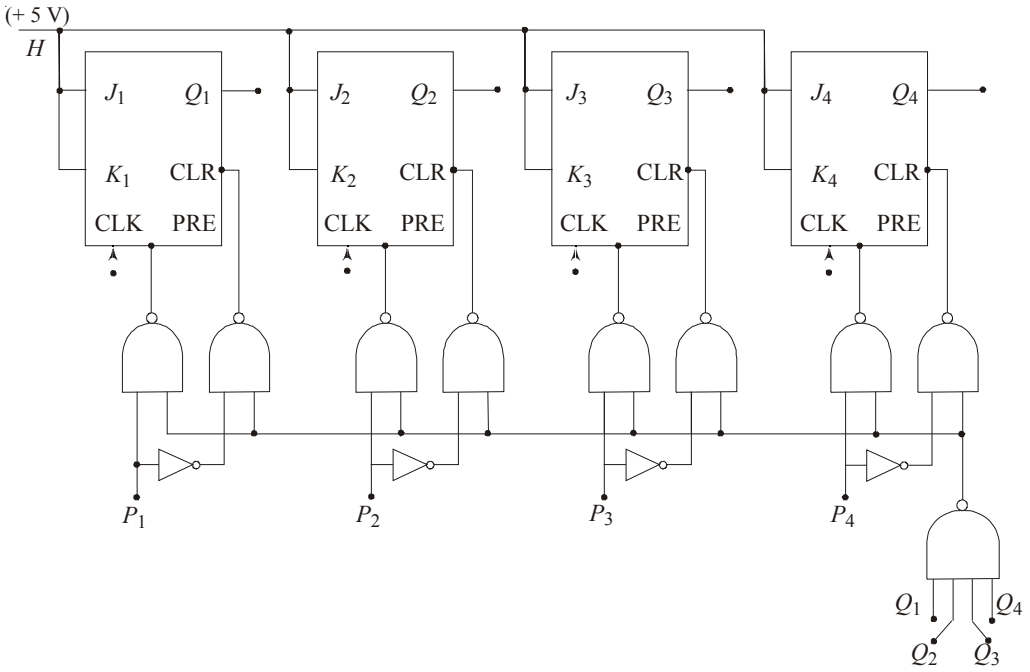


Fig. 5.80

Applications:

1. Direct counting.
2. Divide by N.
3. Measurement of frequency and time.
4. Waveform generation.
5. ADC

Experiment (Synchronous Counter)

Aim: ***To Design and Test the Count Sequences of a Synchronous Counter***

Given sequency: 0, 7, 1, 6, 2, 5, 0, 7, ———— (repeating)

Equipment Required:

Equipment	Range	Quantity
Power supply Pulse generator	(0-5) V	1

Circuit Diagram:

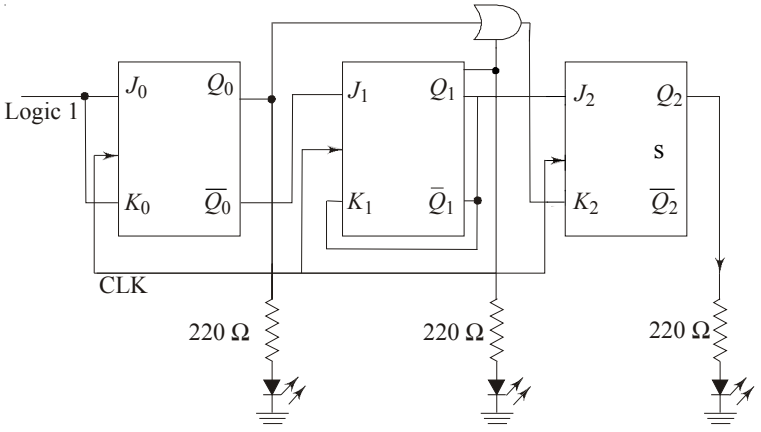


Fig. 5.81

Procedure (Circuit Design):

1. Write the count sequence in binary.
2. For each flip-flop, using excitation table, obtain the inputs for the transitions it has to make for each applied clock pulse.

Excitation Table (J-K flip-flop):

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Maximum number is 7, [i.e., $2^3 = 8$], so 3 binary bit of data is sufficient to design the counter.

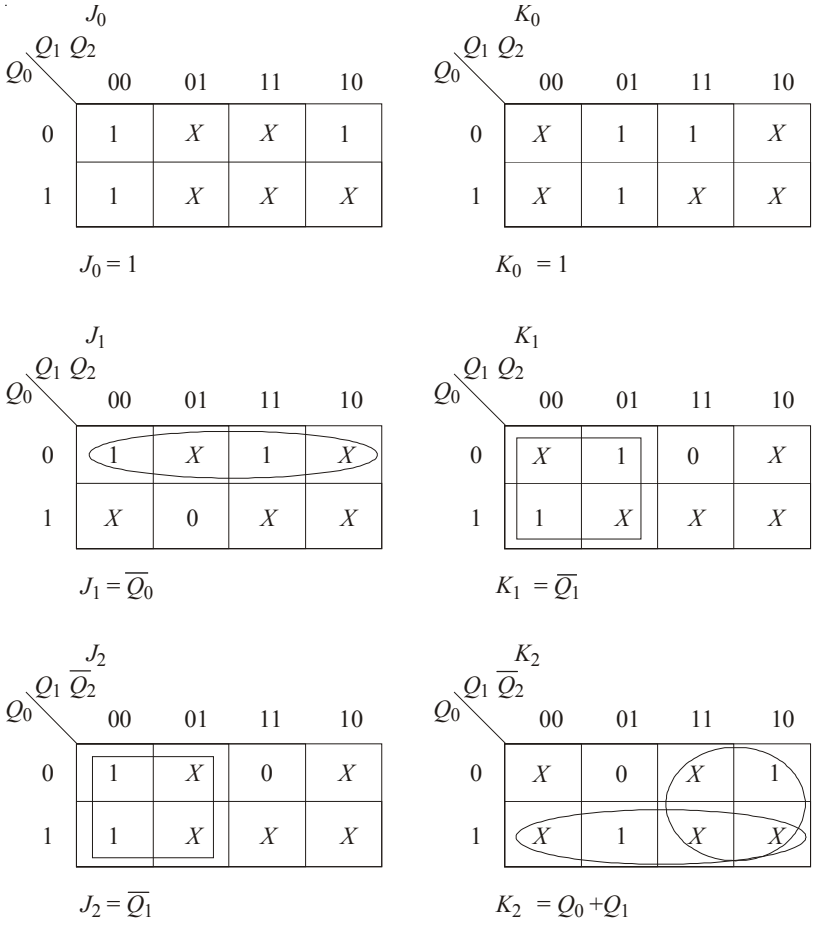
Truth Table:

Decimal number	Present state			Next state		
0	0	0	0	1	1	1
7	1	1	1	0	0	1
1	0	0	1	1	1	0
6	1	1	0	0	1	0
2	0	1	0	1	0	1
5	1	0	1	0	0	0
	J_0/K_0	J_1/K_1	J_2/K_2	J_0/K_0	J_1/K_1	J_2/K_2

Using excitation table, write the logical table.

F/F$_1$		F/F$_2$		F/F$_3$		Decimal Number	
J_0	K_0	J_1	K_1	J_2	K_2	Initial state	Final state
1	X	1	X	1	X	0	7
X	1	X	1	X	0	7	1
1	X	1	X	X	1	1	6
X	1	X	0	0	X	6	2
1	X	X	1	1	X	2	5
X	1	0	X	X	1	5	0

Draw the K-map for the inputs and implement the circuit.



Note: A synchronous counter is one in which all flip-flops are clocked simultaneously.

Exercises:

Design the following synchronous counters:

1. Count 3-bit odd number.
2. Count 3-bit even number.
3. Count Mod-5 sequence.
4. Count 4-bit binary sequence.

Synchronous Sequential Circuit

Obtain the truth table and state diagram of the synchronous sequential circuit shown.

Circuit Diagram:

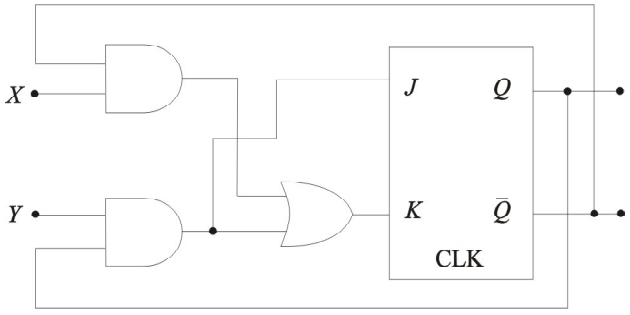


Fig. 5.82

State Transition Table:

Q_n	x	y	$J = Q_n y$	$K = x\bar{Q}_n + y Q_n$	Q_{n+1}
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	1	0
0	1	1	0	1	0
1	0	0	0	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	0

State diagram is shown below:

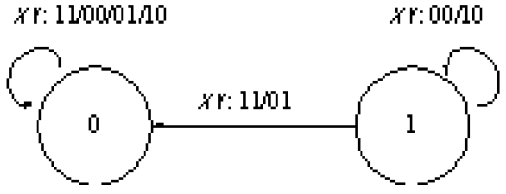


Fig. 5.83

Experiment (Synchronous Sequential Circuit)

Aim: ***To Design a Synchronous Sequential Circuit given a State Transition Diagram.***

Procedure (Design):

1. Given the state transition diagram, form the truth table.
2. Fill in the inputs to be applied to the flip-flops in order to have transitions from a previous state to the next state of output of flip-flops using excitation table.
3. With inputs to the circuit and past outputs of flip-flops, obtain an expression for the flip-flop inputs.
4. Design the circuit from equations obtained.

State Transition Diagram:

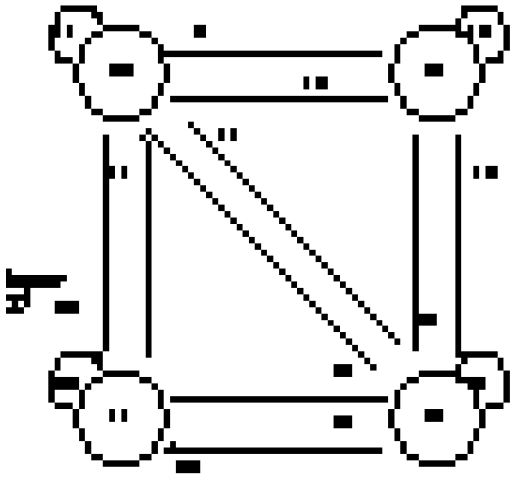


Fig. 5.84

Excitation Table (J-K flip-flop):

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Truth Table:

x	y	Q_{0n}	Q_{1n}	$Q_{0(n+1)}$	$Q_{1(n+1)}$	J_0	K_0	J_1	K_1
0	0	0	0	1	1	1	X	1	X
0	0	0	1	1	1	1	X	X	0
0	0	1	0	1	1	X	0	1	X
0	0	1	1	1	1	X	0	X	0
0	1	0	0	1	0	1	X	0	X
0	1	0	1	1	0	1	X	X	1
0	1	1	0	1	0	X	0	0	X
0	1	1	1	1	0	X	0	X	1
1	0	0	0	0	1	1	X	1	X
1	0	0	1	0	1	1	X	X	0
1	0	1	0	0	1	X	1	1	X
1	0	1	1	0	1	X	1	X	0
1	1	0	0	0	0	0	X	0	X
1	1	0	1	0	0	0	X	X	1
1	1	1	0	0	0	X	1	0	X
1	1	1	1	0	0	X	1	X	1
Combination of inputs and previous state				Next state from the state diagram		From the excitation table			

Obtain expressions for J_0, J_1, K_0 and K_1 using K-map:

XY \ Q_0Q_1	00	01	11	10
00	1	1	X	X
01	1	1	X	X
11	0	X	X	X
10	1	1		X

$J_0 = \bar{X} + \bar{Y}$

XY \ Q_0Q_1	00	01	11	10
00	X	X	0	0
01	X	X	0	0
11	X	X	1	1
10	X	X	1	1

$K_0 = X$

XY \ Q_0Q_1	00	01	11	10
00	1	X	X	1
01	0	X	X	0
11	0	X	X	0
10	1	X	X	1

$J_1 = \bar{Y}$

XY \ Q_0Q_1	00	01	11	10
00	X	0	0	X
01	X	1	1	X
11	X	1	1	X
10	X	0	0	X

$K_1 = Y$

Circuit Diagram:

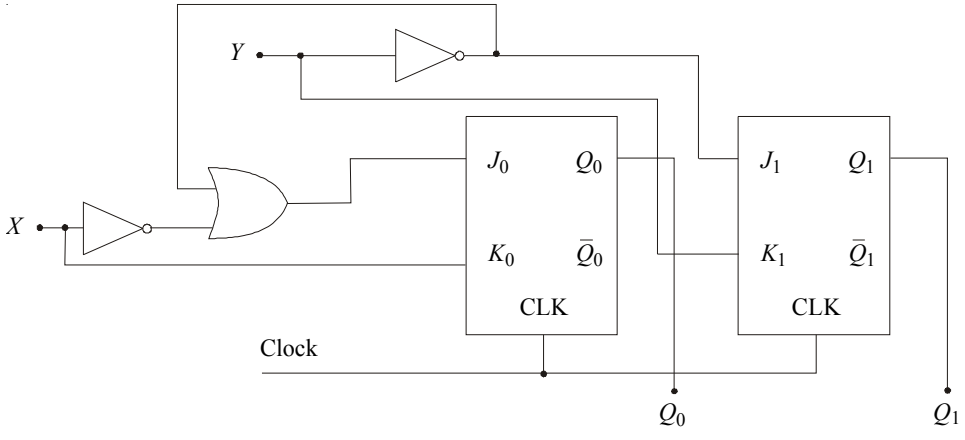


Fig. 5.85

Experiment:

Aim: ***To Obtain the State Diagram given the Synchronous Sequential Circuit.***

Circuit Diagram:

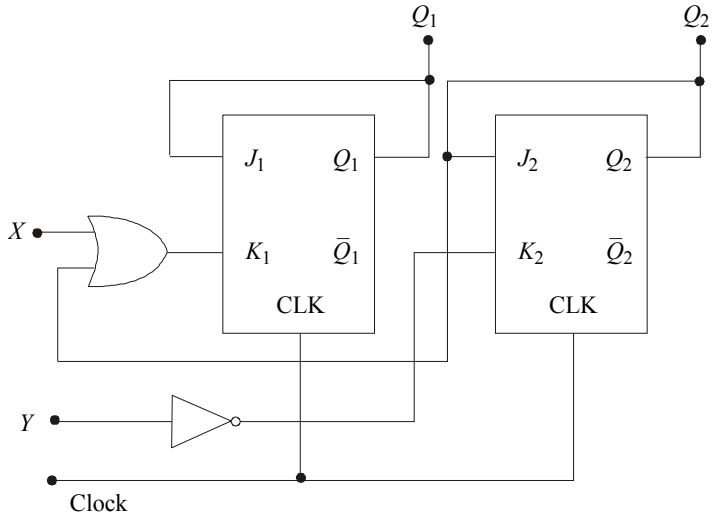


Fig. 5.86

Design Procedure:

1. From a table with all combination of inputs to the circuit (x, y, etc.,) and outputs of all flip-flops.
2. Write down the entries for the flip-flop inputs using the circuit equations.
3. Obtain the next states using the truth table of flip-flop.

Draw the state diagram.

Step I: Table with combination of all input and outputs.				Step II: Entries for flip-flop inputs				Step III: Obtain the next states using truth table.	
x	y	Q_{0n}	Q_{1n}	$J_0 = Q_0$	$K_0 = x + Q_1$	$J_1 = Q_1$	$K = \bar{y}$	$Q_{0(n+1)}$	$Q_{1(n+1)}$
0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	1	1	1	0	0
0	0	1	0	1	0	0	1	1	0
0	0	1	1	1	1	1	1	0	0
0	1	0	0	0	0	0	0	0	0
0	1	0	1	0	1	1	0	1	1
0	1	1	0	1	0	0	0	1	1
0	1	1	1	1	1	1	0	0	0
1	0	0	0	0	1	0	1	0	0
1	0	0	1	0	1	1	1	0	0
1	0	1	0	1	1	0	1	0	0
1	0	1	1	1	1	1	1	0	0
1	1	0	0	0	1	0	0	0	0
1	1	0	1	0	1	1	0	0	1
1	1	1	0	1	1	0	0	0	0
1	1	1	1	1	1	1	0	0	1

Step IV: Draw the state transition diagram.

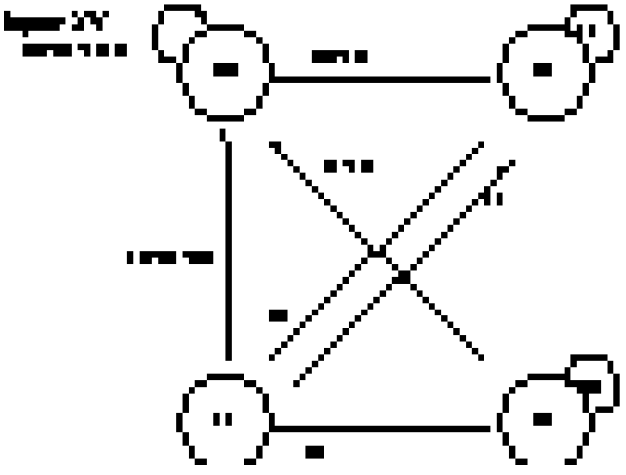


Fig. 5.87

Experiment Code Conversion: Binary to gray

Aim: ***To Design a Binary to Gray Code Converter.***

Equipments required

Equipment	Range	Quantity
logical trainer kit		1

Binary to gray code converter

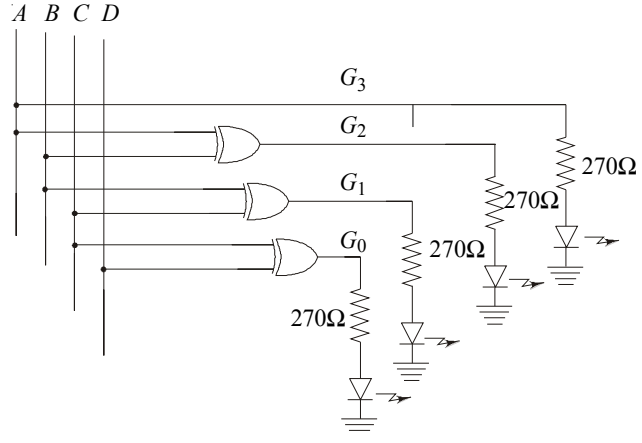


Fig. 5.88

Truth-table:

	Binary input					Gray code output			
BCD	*A*	*B*	*C*	*D*		G_3	G_2	G_1	G_0
0	0	0	0	0		0	0	0	0
1	0	0	0	1		0	0	0	1
2	0	0	1	0		0	0	1	1
3	0	0	1	1		0	0	1	0
4	0	1	0	0		0	1	1	0
5	0	1	0	1	Binary to gray code	0	1	1	1
6	0	1	1	0	⟹	0	1	0	1
7	0	1	1	1		0	1	0	0
8	1	0	0	0		0	1	0	0
9	1	0	0	1		1	1	0	0
10	1	0	1	0		1	1	1	1
11	1	0	1	1		1	1	1	0
12	1	1	0	0		1	0	1	0
13	1	1	0	1		1	0	1	1
14	1	1	1	0		1	0	0	1
15	1	1	1	1		1	0	0	0

Karnaugh map

CD \ *AB*	00	01	11	10
00				
01	1	1	1	1
11				
10	1	1	1	1

$G_0 = C\overline{D} + \overline{C}D = C \oplus D$

CD \ *AB*	00	01	11	10
00		1	1	
01		1	1	
11	1			1
10	1			1

$G_1 = B \oplus C$

CD \ *AB*	00	01	11	10
00		1		1
01		1		1
11		1		1
10		1		1

$G_2 = A \oplus B$

CD \ *AB*	00	01	11	10
00			1	1
01			1	1
11			1	1
10			1	1

$G_3 = A$

Procedure:

1. Connect the logic gate as per diagram.
2. Give the Binary input and verify the corresponding gray code output.

Experiment Code Conversion: Gray to BCD Code Converter

Aim: ***To Design a Gray to BCD Code Converter.***

Equipment required :

Equipment	Range	quantity
Digital trainer kit		1

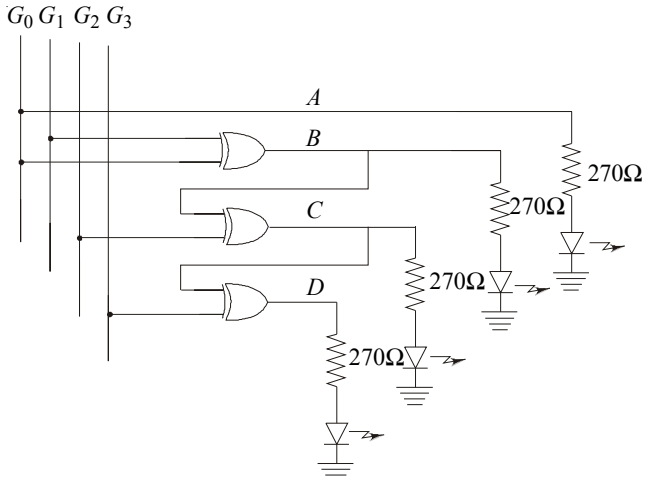


Fig. 5.89

Truth-table:

Gray code input					Binary output			
G_3	G_2	G_1	G_0		A	B	C	D
0	0	0	0		0	0	0	0
0	0	0	1		0	0	0	1
0	0	1	1		0	0	1	0
0	0	1	0		0	0	1	1
0	1	1	0		0	1	0	0
0	1	1	1		0	1	0	1
0	1	0	1		0	1	1	0
0	1	0	0	Gray to binary code ⟹	0	1	1	1
1	1	0	0		1	0	0	0
1	1	0	1		1	0	0	1
1	1	1	1		1	0	1	0
1	1	1	0		1	0	1	1
1	0	1	0		1	1	0	0
1	0	1	1		1	1	0	1
1	0	0	1		1	1	1	0
1	0	0	0		1	1	1	1

Karnaugh map

G_1G_0 \ G_3G_2	00	01	11	10
00			1	1
01			1	1
11			1	1
10			1	1

$A = G_3$

G_1G_0 \ G_3G_2	00	01	11	10
00		1		1
01		1		1
11		1		1
10		1		1

$B = G_2 \oplus G_3$

G_1G_0 \ G_3G_2	00	01	11	10
00		1		1
01		1		1
11	1		1	
10	1		1	

$C = G_3 \oplus G_2 \oplus G_1$

G_1G_0 \ G_3G_2	00	01	11	10
00		1		1
01	1		1	
11		1		1
10	1		1	

$D = G_3 \oplus G_2 \oplus G_1 \oplus G_0$

Procedure:

1. Connect the logic gates as per circuit diagram.
2. Give the gray code as input to the circuit and verify the corresponding Binary output.

Experiment Arithmetic and Logical Unit

Aim: ***To Study the Operation of ALU-74181.***

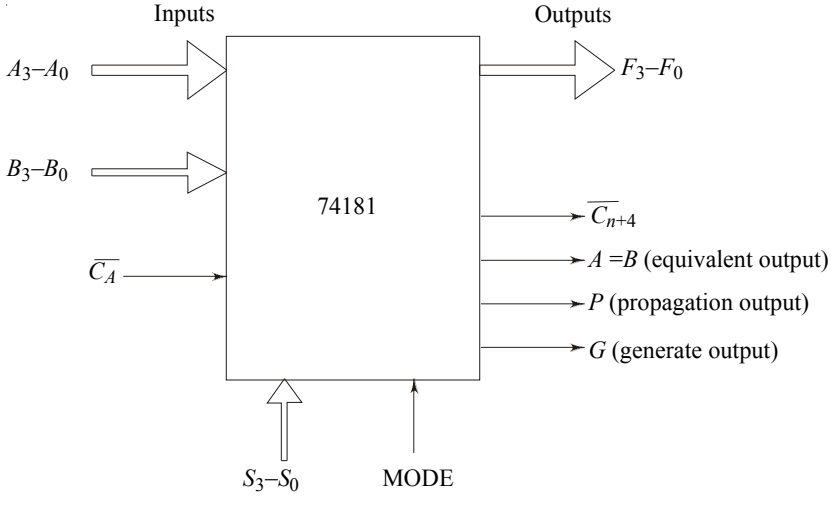
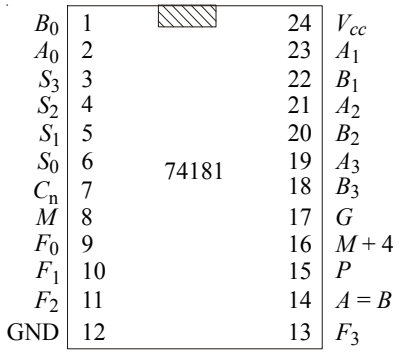


Fig. 5.90

Operation table for 74181

$S_3\ S_2\ S_1\ S_0$	$M = 1$ Logical operation	$M = 0$ Arithmetic and logical operations $\overline{C}_n = 1$ (no carry)	$\overline{C}_n = 0$ (carry)
0 0 0 0	$F = \overline{A}$	$F = A$	$F = A$ plus 1
0 0 0 1	$F = \overline{A + B}$	$F = A + B$	$F = (A + B)$ plus 1
0 0 1 0	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ plus 1
0 0 1 1	$F = 0$	$F =$ minus 1	$F = 0$
0 1 0 0	$F = \overline{AB}$	$F = A$ plus $A\ \overline{B}$	$F = A$ plus $A\ \overline{B}$ plus 1
0 1 0 1	$F = \overline{B}$	$F = (A + B)$ plus $A\ \overline{B}$	$F = (A + B)$ plus $A\overline{B}$ plus 1
0 1 1 0	$F = A \oplus B$	$F = A$ minus B minus 1	$F = A$ minus B
0 1 1 1	$F = A\ \overline{B}$	$F = A\overline{B}$ minus 1	$F = A\overline{B}$
1 0 0 0	$F = \overline{A} + B$	$F = A$ plus AB	$F = A$ plus AB plus 1
1 0 0 1	$F = A \oplus B$	$F = A$ plus B	$F = A$ plus B plus 1
1 0 1 0	$F = B$	$F = (A + \overline{B})$ plus AB	$F = (A + \overline{B})$ plus AB plus 1
1 0 1 1	$F = AB$	$F = AB$ minus 1	$F = AB$
1 1 0 0	$F = 1$	$F = A$ plus A*	$F = A$ plus A plus 1
1 1 0 1	$F = A + \overline{B}$	$F = (A + B)$ plus A	$F = (A + B)$ plus A plus 1
1 1 1 0	$F = A + B$	$F = (A + \overline{B})$ plus A	$F = (A + \overline{B})$ plus A plus 1
1 1 1 1	$F = A$	$F = A$ minus 1	$F = A$

Pin configuration of 74181



Typical Examples

Let $S = 0101$, $A = 0101$, $B = 0011$

If $M = 1$, $F = \overline{B} = 1100$

If $M = 0$ and $C_n = 1$, $F = (A + B)$ plus $A\overline{B} = 1100$

If $M = 0$ and $C_n = 0$, $F = (A + B)$ plus $A\overline{B}$ plus $1 = 1101$

Procedure:

1. Connect the IC with necessary circuit.
2. Test the each Arithmetic and logic operation for different configuration of $S_3\ S_2\ S_1\ S_0$ for the given inputs $A_3\ A_2\ A_1\ A_0$ and $B_3\ B_2\ B_1\ B_0$.

OBJECTIVE QUESTIONS

1. What is system software?
2. What do you understand by shell programming?
3. Realize the AND function using 2:1 multiplexer.
4. What is a prime implecant?
5. What is a universal shift register?
6. What is a self-complementing code?
7. Define fan-out for a logic circuit.
8. Mention the name of the logic family, which comes under the non-saturated logic system.
9. Implement the EX-OR function using only four NAND gates.
10. Draw the MOD-8 ripple counter using JK flip-flop and give the timing diagram.
11. What are DAB and MAB?
12. Name two cache memories that are in between main memory and processor.
13. What is a flip-flop?
14. What is MAR? What is its use?
15. Distinguish between weighted and non-weighted codes.
16. Explain the error detecting and correcting codes with examples.
17. Write a short note on encoder and decoder.
18. Write a short note on multiplexer and demultiplexer.
19. Distinguish between synchronous and asynchronous sequential circuit.
20. What is an up-down counter?
21. What is the need for an ADC?
22. What is the need for a DAC?
23. Describe a typical application of a delay line.
24. What are the characteristics of pulse transformer? Explain with an equivalent circuit.
25. Describe the typical application of a decode counter.
26. What is virtual memory?
27. Explain the concept of cache memory used in modern computing systems.
28. Discuss the need for parallel processing.
29. Perform (110011-100101) using 1's complement and 2's complement arithmetic.
30. Name the two problems that may arise in ripple counters.
31. The propagation delay of STTL is less than TTL gate. What could be the reason for this?
32. What is meant by wired operation?
33. How many RAM chips will be required to build a 4K byte RAM, if you are provided with nibble organized RAM chips each of capacity 4K bits?

6 BASIC COMMUNICATION CIRCUITS

6.1 INTRODUCTION TO COMMUNICATION SYSTEM

In Broad sense, the term communication refers to the transmission of information by electric means. A communication system comprises of a transistor and receiver connected by communication channel (wired channel or wireless channel).

Fig. 6.1

Need for Modulation

Modulation is required for the following reason.

1. To transmit signals over longer distance.
2. It also reduces antenna size.
3. It increases the signal to noise ratio (SNR).
4. Modulation process permits changing the signal frequency to a pre-assigned band.
5. Bandwidth of the modulated signal may be made smaller or larger than the original.

Standard Spectrum of Frequency used in Radio Communication

Carrier Frequency Range	Class	Applications
30Hz-300 KHz	Very low frequency (Audio range) (VLF)	Long distance point to point communications
30KHz-300KHz	Low frequency (LF)	Long distance point to point communication and navigation.
300KHz-3MHz	Medium frequency (MF)	Broadcasting; ship-shore communication.
3MHz-30MHz	High frequency (HF)	National and International broadcasting point to point telephone and telegraph communication; Aviation.
30MHz-300MHz	Very high frequency (VHF)	Radar, television; FM broadcasting; short distance communication.
300MHz-3GHz	Ultra high frequency (UHF)	Fascimile; Air navigation; TV Relay.
3GHz-30GHz	Super high frequency (SHF)	Radar navigation, Radio relay.

6.2 MODULATION

Modulation can be defined as the process by which the characteristics of carrier wave is varied in accordance with the modulating wave (signal). The resultant wave of modulation is called modulated wave.

Types of Modulation

Analog (Continuous Wave) Modulation

Amplitude modulation

Frequency modulation

Phase modulation

Digital Modulation

Pulse code modulation

Delta modulation

Pulse amplitude modulation

Pulse width modulation

Pulse position modulation

Demodulation

Recovery of the message signal from the modulated signal is called demodulation or signal detection.

6.2.1 Amplitude Modulation

In case of amplitude modulation, the carrier amplitude V_c is changed in accordance with the message signal (modulating wave), $m(t)$. Amplitude modulation some times referred to as "Linear modulation".

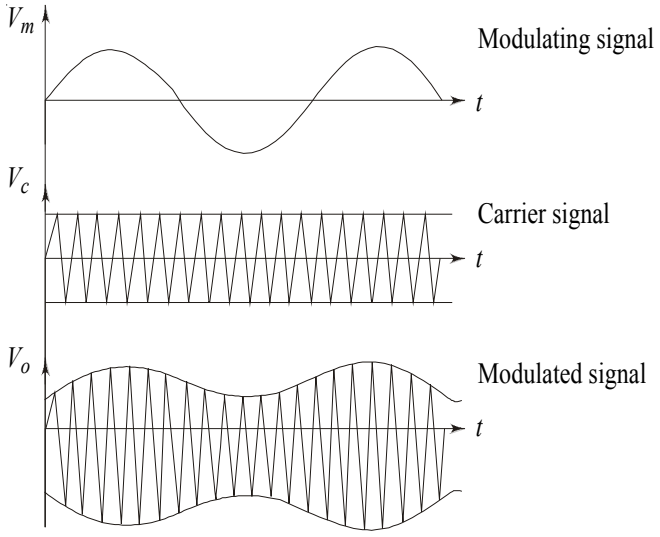


Fig. 6.2

Types of Amplitude Modulation

Amplitude modulation is broadly divided into following four types. They are,

Amplitude modulation with both side bands and carrier (AM/DSB).

Double-side band modulation with suppressed carrier (DSB/SC).

Single-side band with suppressed carrier (SSB/SC) modulation.

Vestigial-side band (VSB) modulation.

Frequency of the AM Signal (AM/DSB):

The frequency components in the AM wave is given by,

$$f_{SB} = f_c \pm nf_m$$

For the first pair $n = 0$ and $n = 1$.

where, f_{SB} = side band frequency.

f_c = carrier frequency

f_m = modulated frequency.

The actual amplitude of the AM wave (A) is given by,

$$A = V_c + V_m \sin \omega_m t$$

where, V_c = carrier signal amplitude.

V_m = modulating signal amplitude.

$V_m \sin \omega_m t$ = modulating signal.

But, modulation index, $m = V_m/V_c$

Therefore,
$$A = V_c + mV_c \sin \omega_m t$$
$$A = V_c (1 + m \sin \omega_m t)$$

The instantaneous voltage of the amplitude-modulated wave is given by,

$$V = A \sin \omega_c t$$
$$V = V_c (1 + m \sin \omega_m t) \sin \omega_c t$$

Expanding the above equation leads to,

$$V = V_c \sin \omega_c t + m (V_c/2) \cos (\omega_c - \omega_m)t - m (V_c/2) \cos (\omega_c + \omega_m)t$$

Frequency Spectrum of Amplitude Modulation

From the above equation, it is clear that the amplitude-modulated signal contain three frequency components. They are,

Carrier frequency component ($V_t \sin \omega_c t$)

Lower side band frequency component [$m (V_c/2) \cos (\omega_c - \omega_m)t$]

Upper side band frequency component [$m (V_c/2) \cos (\omega_c + \omega_m)t$]

Above three frequency components are graphically shown below:

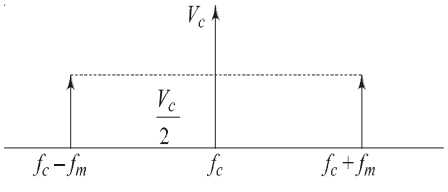


Fig. 6.3

Double-Side Band with Suppressed Carrier (DSB/SC) Modulation

DSB/SC modulation results when amplitude of the modulated wave $A(t)$ is proportional to the modulating signal $m(t)$. In case of DSB/SC, central component is suppressed using suitable filter. It contains only lower side band and upper side band.

$$X_{DSB/SC}(t) = m(t) \cos(\omega_c t)$$

The spectrum of a DSB/SC signal is given by,

$$X_{DSB/SC}(\omega) = \tfrac{1}{2} M(\omega - \omega_c) + \tfrac{1}{2} M(\omega + \omega_c)$$

Left upper side band Right lower side band

Frequency Spectrum of DSB/SC

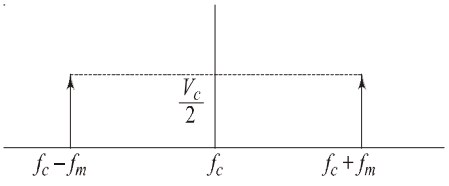


Fig. 6.4

Block diagram

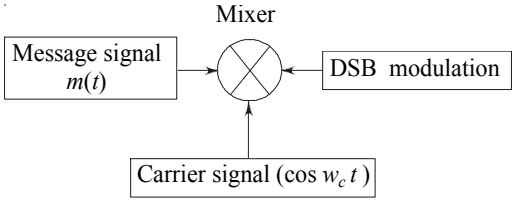


Fig. 6.5

Double-Side Band with Suppressed Carrier (DSB/SC) Demodulation

DSB/SC uses synchronous detection. Synchronous detection is the process in which the modulated signal is mixed with the carrier in a non-linear device in a manner that resembles with that of a multiplicative mixer giving sum and difference frequency components in the output.

The message signal $m(t)$ can be recovered from modulated signal $X_{DSB/SC}(t)$ by multiplying $X_{DSB/SC}(t)$ by a local carrier and the product signal is filtered using low-pass filter (LPT).

Block diagram

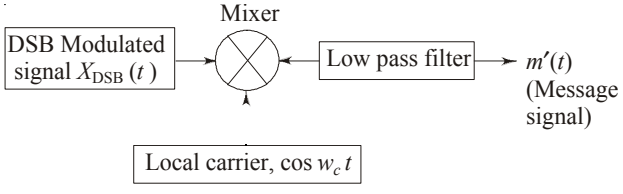


Fig. 6.6

Modulating Index

The modulation index (m) for AM is defined as the ratio of the modulating voltage (V_m) to the carrier signal voltage (V_c) i.e.,

$$m = V_m/V_c \leq 1$$

Power Relation in the AM Wave

The total power (P_t) in the modulated wave is given by the sum of the three powers. i.e., Lower side band power (P_{LSB}) plus upper side band power (P_{USB}) plus carrier power ($P_{carrier}$).

$$P_t = P_{LSB} + P_{USB} + P_{carrier}$$
$$P_t = V^2_{LSB}/R + V^2_{USB}/R + V^2_{carrier}/R$$

$$P_{carrier} = V^2_{carrier}/R = \frac{\left(V_c/\sqrt{2}\right)^2}{R} = \frac{m^2}{4}\left(\frac{V_c^2}{2R}\right)$$

$$P_{LSB} = P_{USB} = V^2_{SB}/R = \left[\frac{\left(\frac{mV_c/2}{\sqrt{2}}\right)^2}{R}\right] = \frac{m^2}{4}\left(\frac{V_c^2}{2R}\right)$$

$$P_t = 2\,\frac{m^2}{4}\left(\frac{V_c^2}{2R}\right) + \left(\frac{V_c^2}{2R}\right)$$

$$P_t = \left[\frac{m^2}{2} + 1\right]\left(\frac{V_c^2}{2R}\right)$$

$$P_t = \left[\frac{m^2}{2} + 1\right] P_{carrier}$$

Ordinary Amplitude Modulation (AM)

An ordinary AM signal is generated by adding a large carrier signal to the DSBSC signal i.e.,

$$X_{AM}(t) = X_{DSBSC}(t) + A\cos(\omega_c t)$$

where, $A\cos(\omega_c t)$ is carrier component.

$$X_{AM}(t) = m(t)\cos(\omega_c t) + A\cos(\omega_c t)$$

The spectrum of $X_{AM}(t)$ is given by

$$X_{AM}(\omega) = \tfrac{1}{2}\,M(\omega - \omega_c) + \tfrac{1}{2}\,M(\omega + \omega_c) + \pi A\,[\delta(\omega - \omega_c) + \delta(\omega + \omega_c)]$$

6.2.2 Amplitude Modulation Envelop Detector

It is a simplest form of demodulation, which consists of a diode and resistance capacitor (RC) combination network in parallel. The circuit employs the linear region of a diode characteristic, hence this detector is called linear-diode detector.

Circuit diagram

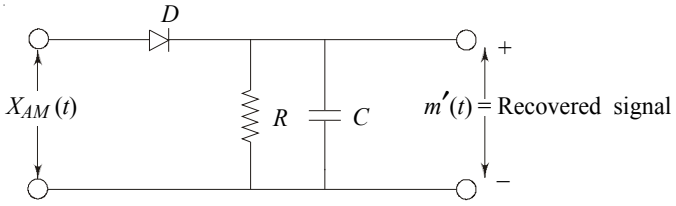


Fig. 6.7

Operation

During the positive half-cycle, the diode is forward biased and the capacitor (C) changes to the peak value of the input modulated signal. As the input signal falls below is maximum value, the diode reverse biased. This slowly discharges the capacitor through resister R until the next positive half-cycle and cycle repeats.

Waveform

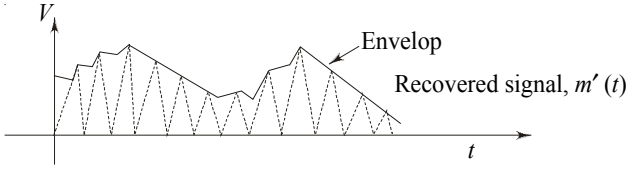


Fig. 6.8

Bandwidth

Bandwidth in AM is given by,

Bandwidth, BW = $2 \times f_m$

where, f_m = highest modulating frequency.

Single Side Band Modulation (SSB/SC)

AM and DSB modulation waste bandwidth because they both require transmission bandwidth equal to double the message bandwidth. Since either side bands (AM and DSB) contain the complete information, only one side band is sufficient for transmission. The modulation, which uses only one side band for the transmission is referred to as single side band with suppressed carrier (SSB/SC) modulation.

Types of SSB/SC Modulation

Frequency discrimination method

Phase-shift method

Frequency Discrimination Method

First generate DSB/SC modulated signal and then suppress one of the side band by using band pass filter. This method is called "Frequency discrimination method".

Block diagram

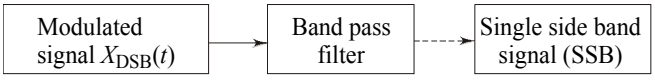


Fig. 6.9

Phase Shift Method

Circuit diagram

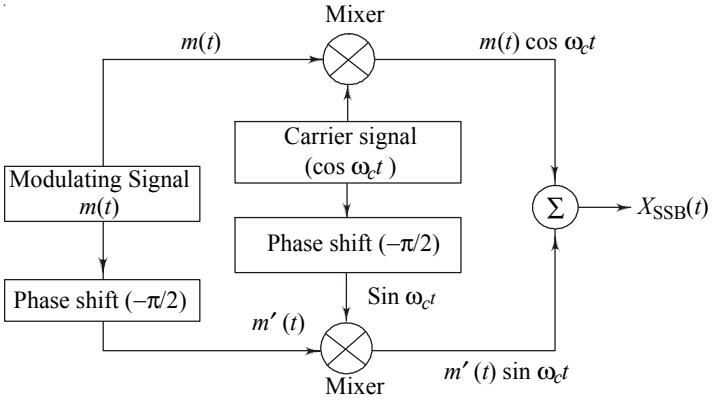


Fig. 6.10

From the figure, the SSB/SC signal $X_{SSB/SC}(t)$ can be represented by

$$X_{SSB/SC}(t) = m(t) \cos (\omega_c t) \pm m'(t) \sin (\omega_c t)$$

$$X_{SSB/SC}(t) = [m(t) \cos (\omega_c t) - m'(t) \sin (\omega_c t)] + [m(t) \cos (\omega_c t) + m'(t) \sin (\omega_c t)]$$

lower side band of SSB/SC signal

upper side band of SSB/SC signal

where, $m'(t)$ is the Hilbert Transform of $m(t)$ which offers 90° phase-shift.

Demodulation of SSB/SC Signal

Demodulation of SSB/SC signal can be achieved by using demodulation of DSB/SC signal technique.

Vestigial Side Band Modulation

In this modulation, one side band is completely passed along with a trace or vestige of the other side band is retained. The typical bandwidth required to transmit a VSB signal is about

1.25 MHz of SSB/SC. The VSB is used to transmit video signal in commercial television where audio signal is transmitted by frequency modulation technique (studying later).

Block diagram

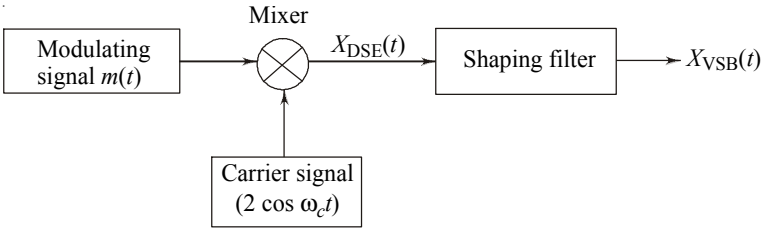


Fig. 6.11

A VSB signal can be obtained by passing DSB/SC modulated signal through a shaping filter.

Demodulation of VSB Signals

Demodulation of VSB signal can be achieved by using demodulation of DSB/SC Signal technique.

Mixer

A device that performs the frequency translation of a modulated signal is called "frequency mixer" or "heterodyning". In most commercial AM radio receiver, the received radio frequency (RF) signal (540 KHz to 1600 KHz) is shifted to the intermediate frequency (IF) (455 KHz) for processing. This IF signal can be demodulated easily.

Image Frequency

Suppose if an AM super heterodyne receiver (locally generate frequency) is chosen to be 455 KHz (IF) higher than the incoming signal. Suppose the reception of an AM station requires 600 KHz, than the locally generated signal is 1055 KHz. If there is another station at 1510 KHz, it also will be received, this second frequency, 1510 KHz = 600 KHz + 2(455KHz) is called the image frequency of the first and after the heterodyning, it is impossible to distinguish the two.

Angle Modulation

Angle modulation is broadly divided into 2 types:

Frequency Modulation (FM).

Phase Modulation (PM).

6.2.3 Frequency Modulation

In this modulation technique, the frequency (ω_c) of the carrier wave is varied according to the modulating signal. In case of FM, the amplitude of the modulated signal remains constant. As the amplitude of the FM remains constant, the noise indulged during transmission and reception can easily removed from the FM by clipping the amplitude of the FM. The clipping action is no way affect the modulating signal during recovery because, the modulating signal is characterized in frequency domain.

For angle modulation, the modulated carrier is represented by,

$$X_c(t) = A \cos [\omega_c t + \phi(t)] \tag{6.1}$$

where, A = carrier amplitude

ω_c = Carrier frequency $(2\pi f_c)$

$\phi(t)$ = Carrier phase angle.

The amount, by which the carrier frequency is varied from its unmodulated value, is called the deviation. Deviation is proportional to the instantaneous value of the modulating voltage. The rate at which their frequency changes is equal to the modulating frequency.

The instantaneous amplitude of the FM signal will be given by,

$$V = A \sin [F(\omega_c, \omega_m)] = A \sin \theta \tag{6.2}$$

But the instantaneous frequency (f) of the FM wave is given by,

$$f = f_c [1 + k V_m \cos (\omega_m t)]$$

$$\omega = \omega_c [1 + k V_m \cos (\omega_m t)]$$

(Same as AM with voltage replaced by frequency)

Therefore, $\theta = \int \omega \, dt = \int \omega_c [1 + k V_m \cos (\omega_m t)] \, dt$

On simplification,

$$\theta = \omega_c t + (\delta / f_m) \sin (\omega_m t) \tag{6.3}$$

Substitute in equation (6.2) we get,

$$V = A \sin [(\omega_c t) + (\delta / f_m) \sin (\omega_m t)] \tag{6.4}$$

where, $\delta = k V_m f_c$.

Modulation Index (m_f)

The modulation index (m_f) for FM is defined as the ratio of maximum frequency deviation to the modulating frequency.

$$m_f = (\delta / f_m) \tag{6.5}$$

Therefore modulated signal equation becomes

$$V = A \sin [(\omega_c t) + m_f \sin (\omega_m t)] \tag{6.6}$$

Bandwidth Requirement

Bandwidth, BW = $2 \times f_m \times$ highest required side bands.

The number of side band components is theoretically infinity.

Pre-Emphasis

Increasing the amplitude of the higher modulating frequencies to improve the noise immunity (SNR) at the transmitted stage in accordance with a pre-arranged curve is called pre-emphasis.

De-Emphasis

The compensation given to the pre-emphasized signal at the receiver to get back the original-modulating signal is called de-emphasis.

Let us expand the carrier signal using Fourier transformation as it gives different frequency component.

$$X_{Fm}(t) = A \sin [\omega_c t + m_f \sin (\omega_m t)]$$

Let us rewrite the above equation in exponential form,

$$X_c(t) = \text{Re}\{A \exp [j(\omega_c t + \phi(t)]\} \tag{6.7}$$

$$X_c(t) = \text{Re} \{A \exp [j(\omega_c t)\} [1 + j\phi(t) - \phi^2(t)/2! - \phi^3(t)/3! + \cdots j^n \phi^n(t)\, n! + \cdots]\}$$

$$X_c(t) = A [\cos (\omega_c t) - \phi(t) \sin (\omega_c t) - \phi^2(t)/2! \cos (\omega t) - \phi^3(t)/3! \sin (\omega_c t) + \cdots j^n \phi^n (t) n! \sin (\omega_c t) + -] \tag{6.8}$$

Diagram

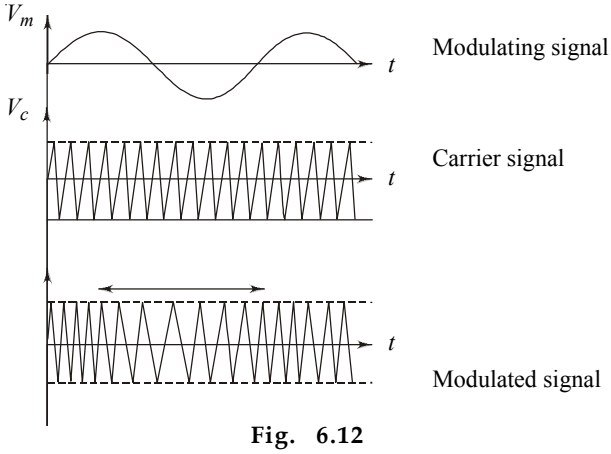


Fig. 6.12

A narrow band FM can be defined as that in which the modulation index is always less than or equal to unity. Above expanded equation contains unmodulated carrier + many different AM terms such as $\phi(t) \sin \omega_c t$, $\phi^2(t) \cos \omega_c t$, $\phi^3(t) \sin \omega_c t$, ... etc., Hence number of side bands in FM is infinity ideally.

Types of Modulation

Narrow band angle-modulated signal (NBFM)

Wide band angle-modulated signal (WBFM)

Narrow Band Angle-Modulated Signal

If $|\phi(t)_{\max}| << 1$.

Then equation (6.8) can be approximated as,

$$X_c(t) \approx A \cos (\omega_c t) - A \phi(t) \sin (\omega_c t) \tag{6.9}$$

(higher terms are neglected)

Above equation represent the narrow band angle-modulated signal.

Block diagram

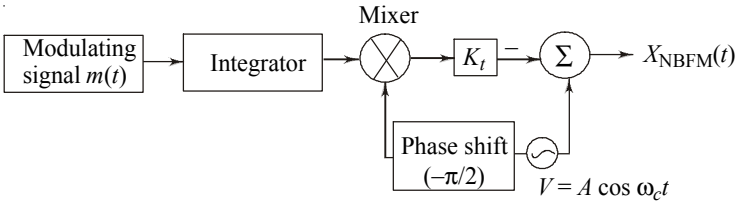


Fig. 6.13

Wide Band Angle-Modulated Signal

Wide band FM can be defined as that in which modulation index normally exceeds unity. There are two methods to generate wide band FM. They are,

Indirect Method

Direct Method

Indirect Method

In this method, NBFM signal is produced first and using frequency multiplier, NBFM signal is converted into WBFM signal.

Block diagram

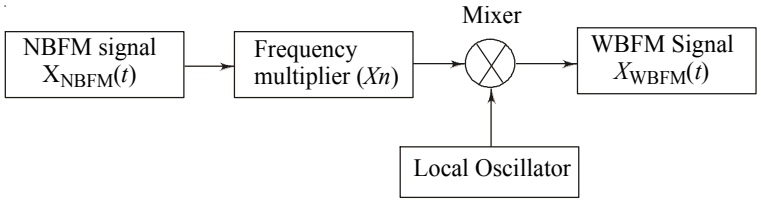


Fig. 6.14

If the NBFM signal is,

$$X_{NBFM}(t) = A \cos [\omega_c t + \phi(t)]$$

Then WBFM signal is given by

$$X_{WBFM}(t) = A \cos [n\ \omega_c(t) + n\phi(t)]$$

Since frequency multiplier increases the carrier frequency to a large value, hence local oscillator (super-heterodyning) is used to have shift in frequency.

Direct Method

In this method, the modulating signal directly controls the carrier frequency. A common method used is to vary the inductance or the capacitance of the tuned circuit. Here the frequency of the tuned circuit is controlled by the modulating signal. The main advantage of this method is large frequency duration can be obtained. The main disadvantage of this method is poor frequency stability.

The Ratio Detector

The ratio detector behaves in the same way as the phase discrimination when input frequency varies.

6.2.4 FM Demodulation Using PLL

The frequency selective property of a phase logged loop (PLL) system is responsible for its application

Block diagram: PLL

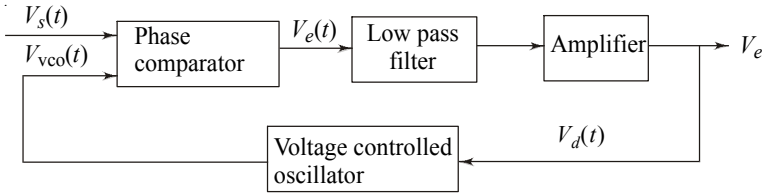


Fig. 6.15

No Signal Condition

When the input signal is zero, the error voltage $[V_e(t)]$ becomes zero and hence $V_d(t) = 0$. The voltage controlled oscillator (VCO) operates at a frequency $\omega_0 = 1/2\pi f$ (free running frequency).

Signal Condition

When the signal is applied, the phase comparator compares the frequency and the phase of the input $[V_s(t)]$ signal with the output voltage $[V_{vco}(t)]$ of the voltage controlled oscillator and generate an error voltage $[V_e(t)]$. This error signal is filtered (low pass filter), amplified and applied to the VCO. This closed loop concepts continues till the difference between input signal and the output voltage $[V_{vco}(t)]$ of the voltage controlled oscillator is closed to resonant frequency (f_o). This causes the phase locked loop (PLL) to lock with the incoming signal.

In the de-modulation technique, the linearity of the modulation output is determined by the frequency to voltage conversion characteristic of VCO. Thus the PLL can be used to detect wide band or narrow band FM signals with a high degree of linearity.

Demodulation of Angle-Modulated Signal

Frequency discrimination is used to get back the modulating signal from the modulated signal. Let us consider the modulated signal as,

$$x_e(t) = A \cos [\omega_c t + \phi(t)]$$

After frequency discrimination, the modulated signal becomes,

$$M'(t) = k_d [d\phi(t)/\mathrm{d}t]$$

where, K_d = Constant (discriminator sensitivity).

Types of De-Modulators

Balanced slope detection

Phase discriminator

Ratio detector

Slope Detection

Modulated signal fed to a tuned circuit whose resonant frequency is equal to one side of the center frequency of the FM signal. The output of this tuned circuit will have amplitude that depends on the frequency deviation of the input signal.

Disadvantages

Slope detector is linear only along a very limited frequency range.

This circuit is relatively difficult to adjust the deviation.

Balanced Slope Detector

The circuit uses two slope detectors. They are connected back to back to the opposite ends of center-tapped transformers, and hence fed 180° out of phase. The top slope detector is tuned above the IF by an amount and bottom slope detector is tuned below the IF by the same amount. Each tuned circuit is connected to a diode detector with an RC load. The output is taken across the series loads.

Disadvantages

1. Alignment problem still exists.
2. This circuit doesn't exhibit linearity.
3. Amplitude limiting is not provided.

Foster-Sally Frequency Discriminator

It employs a double-tuned transformer to convert the frequency duration in an FM signal into an amplitude variation linearly.

Circuit diagram

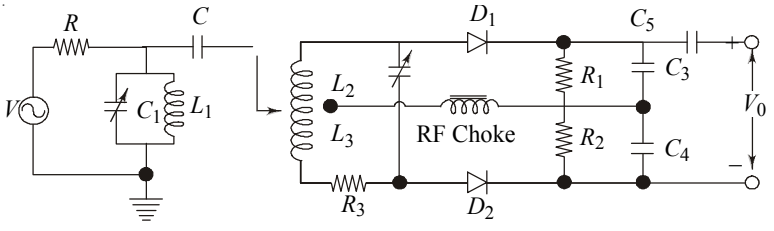


Fig. 6.16

The above circuit tuned at two different frequencies $\omega_1^2 = 1/L_1\ C_1$ and $\omega_2^2 = 1/L_2\ C_2$. If the frequency deviation is δ from the resonance. The voltage across the input resonance (ω_1) circuit is given by V_1 and the voltage across the output resonance (ω_2) is V_2. The voltage of the output tuned circuit V_2 is in phase quadrate with voltage of the input tuned circuit V_1.

The voltage across the diodes are given by V_{d1} and V_{d2},

where, $V_{d1} = V_1 + (V_2/2)$ and $V_{d2} = V_1 - (V_2/2)$

$$|(V_{d1} - V_{d2})| = f(k, q, v, L_1, L_2)$$

Hence frequency departures from resonant frequency are translated into amplitude information.

6.2.5 Distinguishable Characters: AM and FM

Amplitude modulation	Frequency modulation
1. Amplitude of the modulated wave varies accordance with the modulating signal.	1. Amplitude of the modulated wave remains constant.
2. Amplitude of the modulated wave depends on the modulation depth.	2. Amplitude of the modulated wave is independent of the modulation depth.
3. Most of the transmitted power is concentrated in carrier only.	3. All the transmitted power is useful.
4. Amplitude limiter cannot be used as it affects the signal information.	4. Amplitude limiter is used to remove the amplitude variation due to noise.
5. It is relatively poor.	5. It is more immune to noise.
6. It is not possible to exceed 100% modulation without causing severe distortion.	6. Noise level can be reduced by increasing the deviation.
7. Communication channel need not have larger bandwidth.	7. Communication channel should have larger band width.
8. AM equipments are simple.	8. FM equipments are more complex.
9. Area of reception for AM is broader.	9. Area of FM is very small.
10. Number of side band is two.	10. It has infinite number of side bands.
11. Increased depth of modulation increases the side band power and hence the total transmitted power.	11. The total transmitted power always. remains constant. But with increased depth of modulation, the required band width is increased.

Radio-Frequency Spectrum

Frequency Range	Designation	Applications
30 Hz-300 Hz	Extremely low frequency (ELF)	Telephone, audio frequency
300 Hz-3 kHz	Voice frequency (VF)	Audio frequency
3kHz-30 kHz	Very low frequency (VLF)	Audio frequency
30kHz-300 kHz	Low frequency (LF)	
300 kHz-3 MHz	Medium frequency (MF)	AM broadcast
3 MHz-30 MHz	High frequency (HF)	Aircraft radio
30 MHz-300 MHz	Very high frequency (VHF)	FM broadcast
300 MHz-3 GHz	Ultra high frequency (UHF)	
3 GHz-30 GHz	Super high frequency (SHF)	Satellite/Ground
30 GHz-300 GHz	Extremely high frequency (EHF)	Microwave

FCC Channel Bandwidth Allocations

Designation	Frequency Range	Channel	Bandwidth
AM broadcast	535-1605 kHz	106	10 kHz
Citizen band	26.965-27.405 kHz	40	10 kHz
FM broadcast	88-108 MHz	100	200 kHz
TV broadcast	54-806 MHz	67	6 MHz

6.3 Digital Communication

Data communication became very important with the advancements made in computers and data processing. Data communications depend on digital electronics, digital communication offers many advantages over analog communication such as reduced power consumption, reduced noise, increased SNR, higher efficiency, higher performance, greater versatility, higher security and greater error correction.

To transmit analog message by digital means, the signal has to be converted into digital signal. This process is called "Analog to Digital Conversion (ADC)".

Basic Definitions

Sampler

Sampler is a circuit, which samples the analog signal at discrete instants govern by the sampling theorem.

Quantization

Quantizer is a circuit, which represents the sampled values of the amplitude by a finite set of levels.

Encoder

Encoder is a circuit, which designates each quantized level by a code.

Sampling Theorem

The sampling theorem states that, if the sampling rate in any pulse modulation system exceeds twice the maximum signal frequency, the signal can be reconstructed in the receiver with minimum distortion.

$$f_s \geq 2f_m$$

The process of analog to digital conversion is sometimes referred to as "digital pulse modulation".

Basic types of digital pulse modulation.

Pulse Code Modulation

Delta Modulation

6.3.1 Pulse Code Modulation

Block diagram

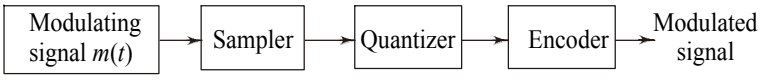


Fig. 6.17

The quantizing and encoding operations are usually performed in analog to digital converter. The combined use of quantizing and encoding distinguishes PCM from analog pulse modulation techniques.

Waveform of PCM

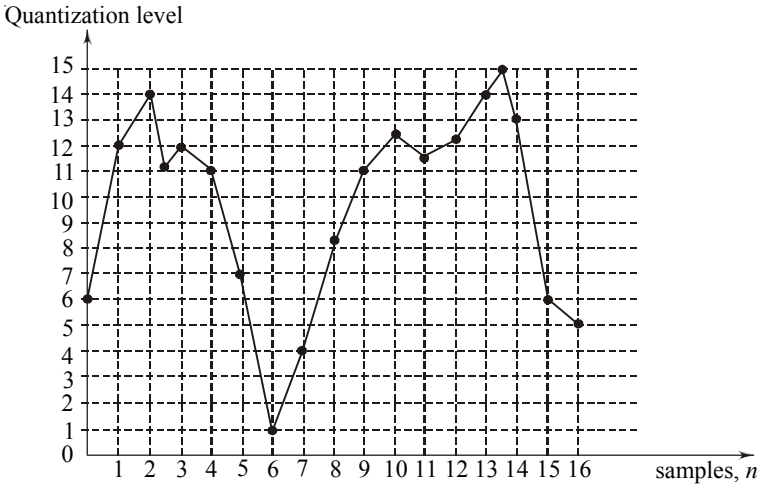
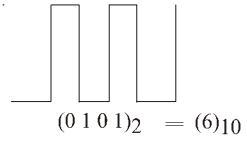


Fig. 6.18

Each sampled point is decoded in terms of digital logic "0" and "1" against quantized level. Since $2^4 = 16$ levels have been taken for the analysis, each sample point is represented by four '0'/'1' combinations, i.e. to represent point at $n = 0$,

$n = 0$,



$n = 1$,

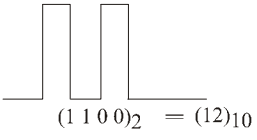


Fig. 6.18A

Advantages of PCM

Better SNR (Signal to Noise Ratio).

Better for broad band communication.

Disadvantages of PCM

It requires complex encoding and quantizing circuitry.

It requires larger bandwidth.

6.3.2 Pulse-Amplitude Modulation

In pulse modulation, the amplitude of discrete pulses varies with the instantaneous sample values of an analog message signal.

Diagram

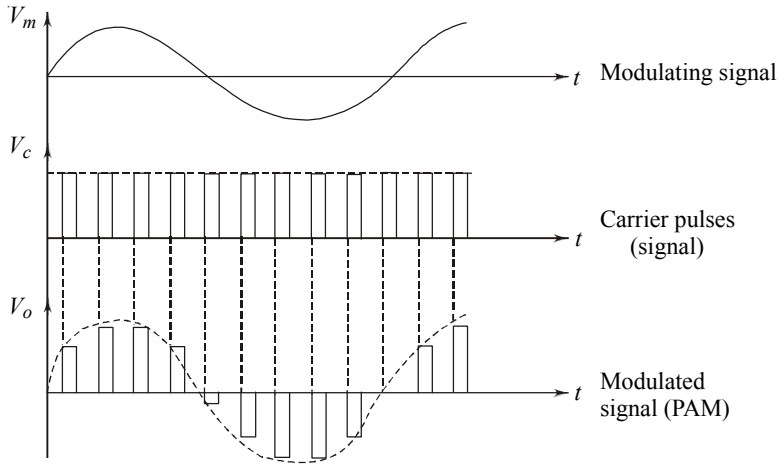


Fig. 6.19

6.3.3 Pulse Width Modulation

Circuit diagram

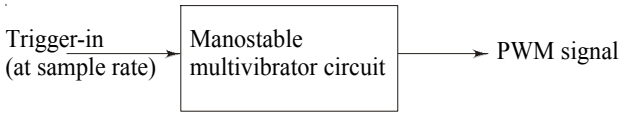


Fig. 6.20

In pulse width modulation, the width of the modulated signal varies in accordance with the amplitude of the modulating signal. Amplitude of the modulated wave remains same. In a practical pulse with modulation circuit, mano-stable multivibrator converts the voltage (trigger in) to time, since its gate width is depending on the voltage to which the capacitor is charged. The circuit does the twin jobs of sampling and converting the samples into PWM.

Demodulation

The PWM is fed to an integrating circuit from which a signal emerges whose amplitude at any time is proportional to the pulse width at that time.

Block diagram

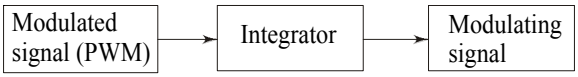


Fig. 6.21

Waveform of PWM

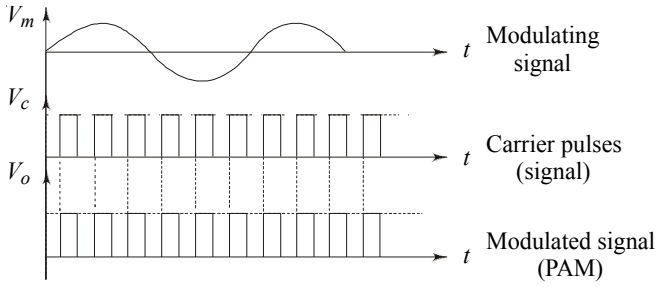


Fig. 6.22

Non-Uniform Quantization and Companding

For the signals like voice, the uniform Quantization is not efficient. It is found that smaller amplitudes predominate in speech than the larger amplitudes. An efficient scheme is to employ a non-uniform quantization method in which smaller steps are used for smaller amplitudes.

Waveform of Voice Signal

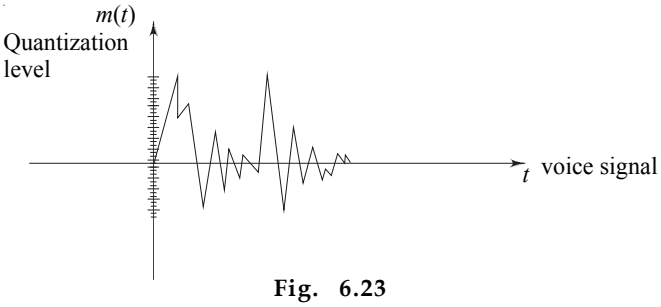


Fig. 6.23

First compressing signal samples and using a uniform Quantization can achieve the same result.

"μ-Law" is used to compress the given signal

$$v = \frac{\ln\left(1 + \mu |m/m_p|\right)}{\ln(1+\mu)} \times \text{Sgn}(m) \quad |m/m_p| \leq 1$$

$$\text{Sgn}\ (m) = +\ 1 \text{ for } m > 0$$
$$-\ 1 \text{ for } m < 0$$

where, m = signal; m/m_p = normalized signal; μ = positive constant.

To restore the signal samples to their correct relative level, an expander with a characteristic complimentary to that of the compressor is used in the receiver. The combination of compression and expansion is called "Companding".

6.3.4 Pulse-Position Modulation (PPM)

The amplitude of the width of the pulse is kept constant in this system, while the position of each pulse, in relation to the position of a recurrent reference pulse, is varied by each instantaneous sampled value of the modulating wave.

Block diagram

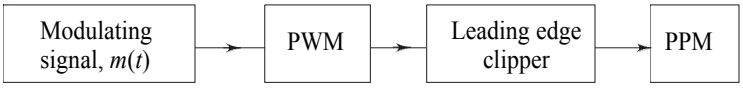


Fig. 6.24

In pulse width modulation (PWM), the leading edges are fixed, wherever those of a trailing edge are not their position depends on the pulse width, which is determined by the signal amplitude at that instant. PPM is thus obtained by "getting rid off" the leading edges of the PWM pulses. In PPM, the width of the pulses are same, whereas the position of each pulse changes depending on the modulating signal.

Waveform of PPM

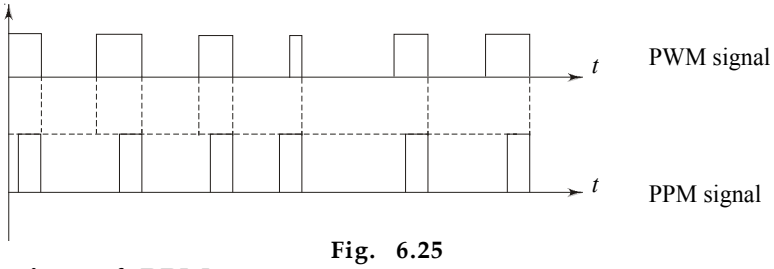


Fig. 6.25

Demodulation of PPM

A flip-flop is basically a multivibrator, which change its output depending on the input. A flip-flop has two inputs and two outputs (complement to each other). One input of the flip-flop receives trigger from a local generator, which is synchronized, by the trigger received from the transmitter, and these triggers are used to switch OFF one of the stages of the flip-flop. The period of time during which this stage is OFF depends on the time difference between the two triggers, so that the resulting pulse has a width that depends on the time displacement of each individual pulse. The resulting PWM pulse train is then demodulated as already explained.

6.3.5 Delta Modulation

In the simple form of the delta modulation, there is just '1' bit sent per sample, to indicate whether the signal is larger or smaller than the previous sample. The difference between the present and previous sample is identified. It is obvious that the bit required to represent the difference is lesser than that of the present sample itself. This system has the attraction of extremely simple coding and decoding procedures, and the quantizing process is also very simple.

Disadvantages

It cannot readily handle rapid amplitude variation, and so quantizing noise tends to be very high.

Transmission rate is very high even with Companding.

6.4 MULTIPLEXING OF SIGNALS

It is a technique whereby several signals are combined into a composite signal for the transmission over a common channel. To transmit a number of these signals over a same channel, the signals

must be kept apart so that they do not interfere with each other, and thus they can be separated at the received end.

6.4.1 The Division Multiplexing (TDM)

Time division multiplexing is commonly used to simultaneously transmit several different signals over a single channel.

Block Diagram

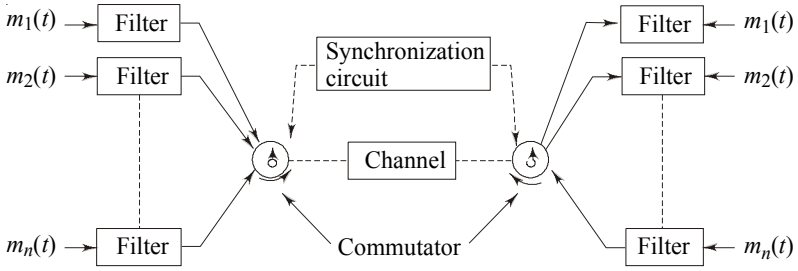


Fig. 6.26

Each input signal is band limited by using filter (like low pass filter, high pass filter or band filter) to remove the unwanted frequencies. The output of the filter is connected to the input stage commutator (electronic switch). Each signal is sampled at Nyquist rate or greater to avoid overlapping. The samples are interleaved and a single composite signal consisting of all the interleaved pulse to transmit over the channel.

At the receiving stage, these signals are collected through output stage commutator, which is synchronous with the input stage commutator. These signals are once again filtered and collected.

Applications

Used in telephony system.

Used in Telemetry system.

Used in data processing.

The minimum bandwidth of the channel required for the TDM transmission is proportional to the message signal bandwidth and the number of the multiplexed signal.

6.4.2 Frequency-Division Multiplexing (FDM)

In frequency division multiplexing, the signals are separated in frequency.

Block diagram

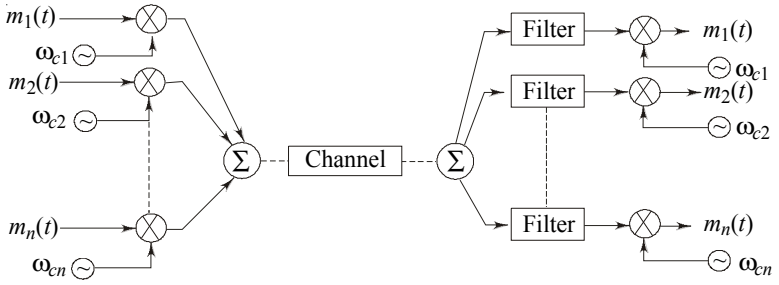


Fig. 6.27

By using frequency-division multiplexing (FDM), simultaneous transmission of multi-signal is possible. Any type of modulation can be used in FDM as long as the carrier spacing is sufficient to avoid spectral overlap. However, the mostly used method of modulation is SSB modulation. At the receiving end of the channel the three modulated signals are separated by filters and modulated.

Commercial AM broadcast stations use carrier frequency, spaced 10 KHz apart from the frequency range from 540 KHz to 1600 KHz.

Experiment : Amplitude Modulation

Aim : ***To construct an amplitude modulation circuit and to calculate the modulation index.***

Equipment Required

Equipment	Range	Quantity
CRO	(0 – 20) MHz	1
Function generator	(0 – 1) MHz	2
Power supply	(0 – 30) V	1

Components Required:

Components	Value	Quantity
Transistor	BC107	1
Capacitor	0.1 μF; 10 μF	
Resistor	22 kΩ, 10 kΩ, 1.2 kΩ	

Circuit diagram

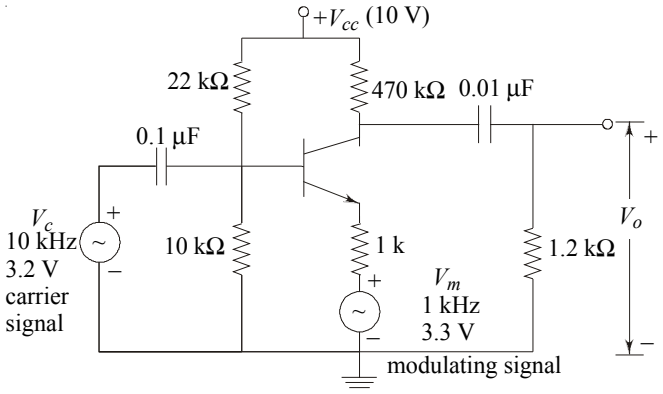


Fig. 6.28

Design

The design of amplitude modulation circuit is same as simple single stage RC coupled amplifier with function generator (V_m) replaced by its output resistance (50 Ω).

Procedure

1. Connections are made as shown in the Fig. 6.28.
2. Set the carrier signal to 3.2 V, 10 kHz using function generator.
3. Set the modulating signal frequency to 1 kHz and vary the amplitude around the carrier voltage.
4. Note down the maximum and minimum voltages from the CRO.

5. Calculate the modulation index using the formula, modulation index,

$$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \times 100\%$$

Model waveform (Observed in CRO)

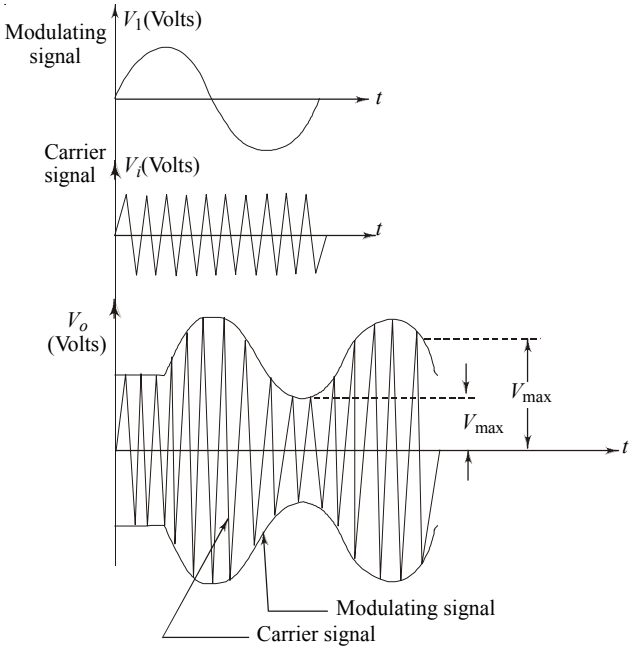


Fig. 6.29

Tabular Column

V_m(Volts)	V_{max} (Volts)	V_{min} (Volts)	m(%)

Experiment : Amplitude Demodulation

Aim : ***To construct an amplitude demodulation circuit and to plot the wave form.***

Equipment Required

Equipment	Range	Quantity
CRO	(0 – 20) MHz	1
AM kit		1

Components Required

Components	Value	Quantity
Diode	IN4001	1
Capacitor	0.01 µF; 10 µF	
Resistor	1 kΩ	

Circuit diagram

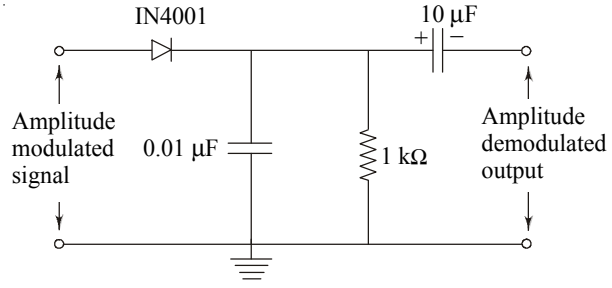


Fig. 6.30

Procedure

1. Connections are made as shown in the Fig. 6.30.
2. Apply AM signal to the given circuit.
3. Observe the amplitude demodulated output on the CRO.
4. Compare the demodulated signal with original modulating signal (Both must be same in all parameters).

Model Graph

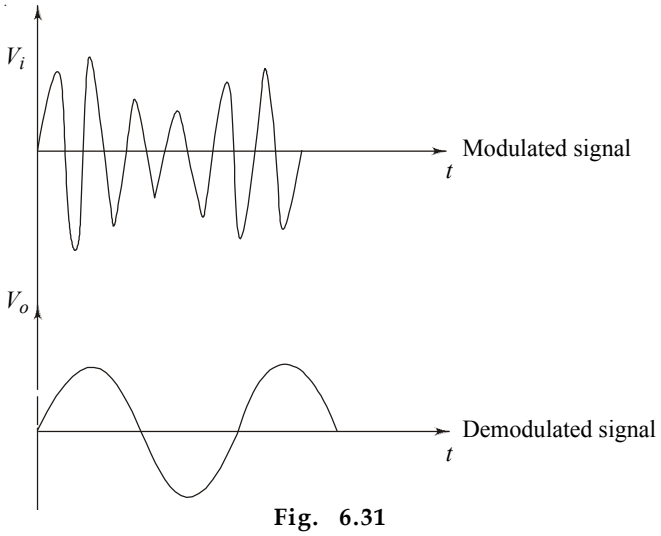


Fig. 6.31

Experiment : Frequency Modulation

Aim : ***To construct the frequency modulation circuit and to calculate the modulation index.***

Equipment Required

Equipment	Range	Quantity
CRO/Spectrum analyser	(0 – 20) MHz	1
Function generator	(0 – 1) MHz	1
Power supply	(0 – 30) V	1

Components Required

Components	Values	Quantity
Capacitors	1 μF;	1
	0.01 μF	2
	10 μF	1
Resistors	47 kΩ	2
	4.7 kΩ	1
	100 kΩ	1
	150 Ω	1
Potentiometer	100 kΩ	1

Circuit diagram

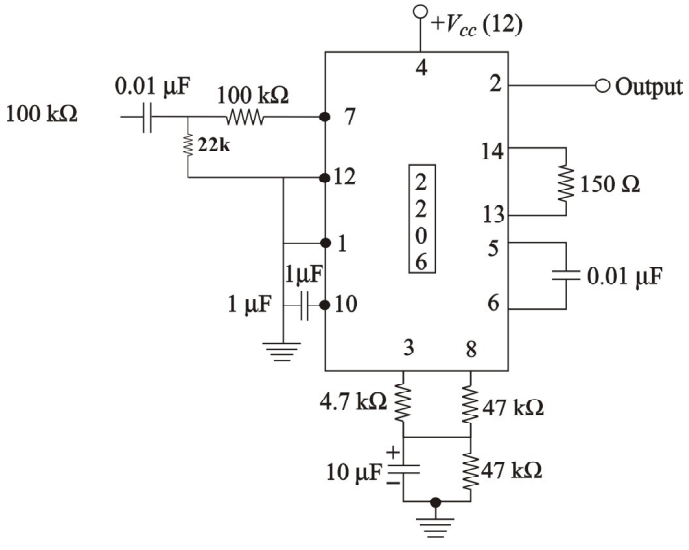


Fig. 6.32

Procedure

1. Connections are made as per circuit diagram.
2. Without signal applied, measure carrier signal at pin No. 2 of IC 2206.
3. Apply modulating AF signal at pin No. 7 of IC 2206.
4. Observe frequency modulated signal on CRO/spectrum analyser.
5. Calculate modulation index, $m_f = (\delta)/f_m$
   where, (δ) = maximum frequency deviation
   f_m = modulating frequency
6. Calculate the bandwidth, BW = 2 $(f_m + \delta)$.

Model Graph

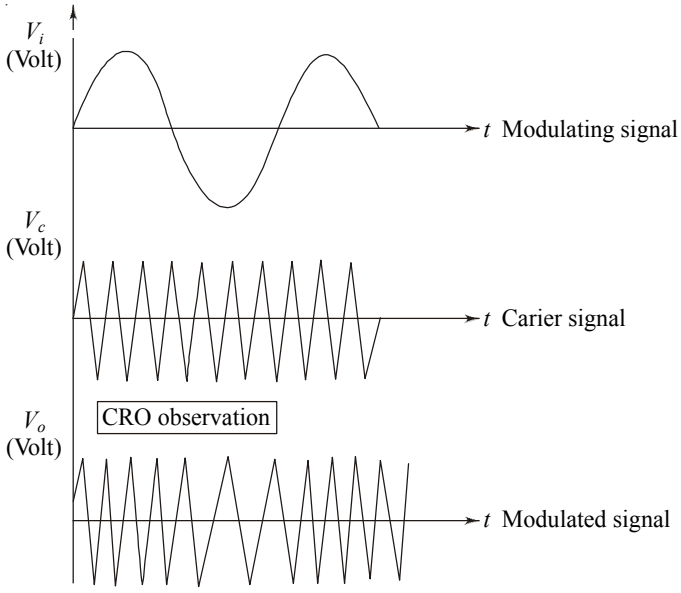


Fig. 6.33

Experiment : Frequency Demodulation

Aim : ***To construct the frequency demodulation circuits and to observe waveform.***

Equipment Required

Equipment	Range	Quantity
CRO/Spectrum analyser	(0 – 20) MHz	1
FM kit		1
Power supply	± 12 V	1

Components Required

Components	Value	Quantity
IC565		1
Capacitors	10 μF	1
	100 μF	1
	470 pF	1
Resistors	560 Ω	2
	10 kΩ	1

Circuit diagram

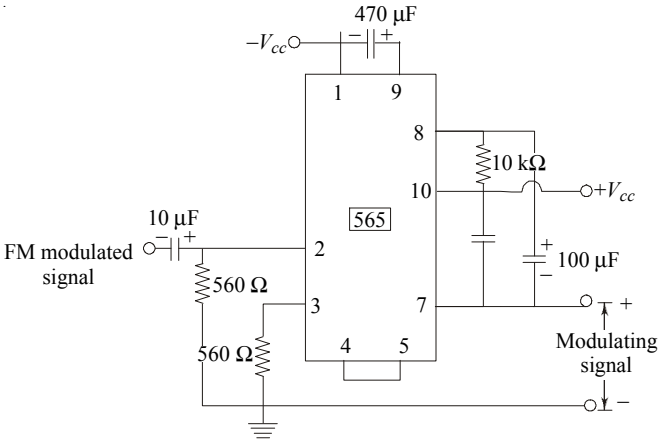


Fig. 6.34

Procedure

1. Connections are made as per circuit diagram.
2. Check if PLL (IC565) is functioning or not by giving square wave to input and observe output.
3. Frequency of input signal (square wave) is varied till input and output are locked.
4. Now frequency modulated signal is fed as input and frequency demodulated signal (modulating signal) is observed on CRO/Spectrum analyser.

Model Graph

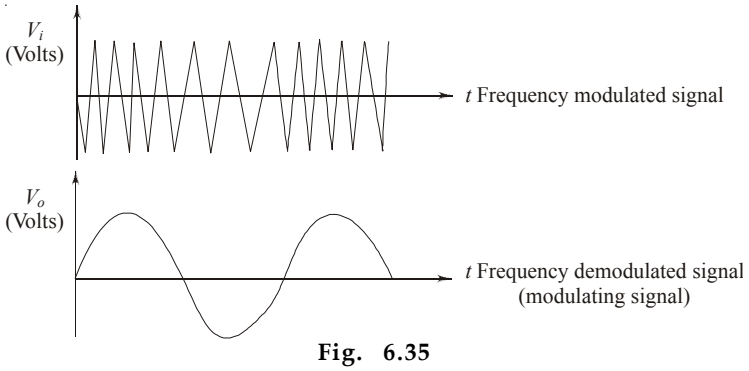


Fig. 6.35

Experiment : Pulse Position Modulator

Aim : ***To study and implement PPM using IC555 and to observe waveform.***

Equipment Required

Equipment	Range	Quantity
CRO	(0 – 20) MHz	1
Power supply	+5 (fixed)	1
	(0 – 5) V	1

Components Required

Components	Value	Quantity
TIMER IC	555	2
Resistor	10 kΩ	2
	1 kΩ	1
Capacitor	0.01 µF	3

Circuit diagram

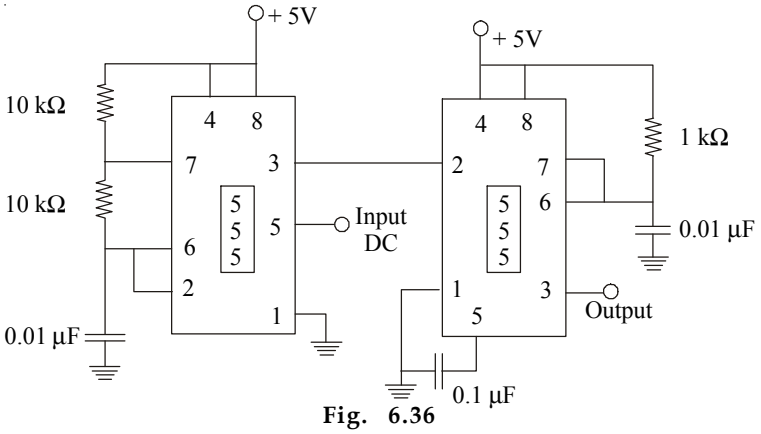


Fig. 6.36

Procedure

1. Connections are made as per the circuit diagram.
2. Vary the input (DC Voltage) from 0 – 5V at pin No. 5 of timer IC.
3. Observe the corresponding output waveform on the CRO at pin No. 3 of second timer IC.
4. Plot the observed waveform for any one reading.

Model Graph

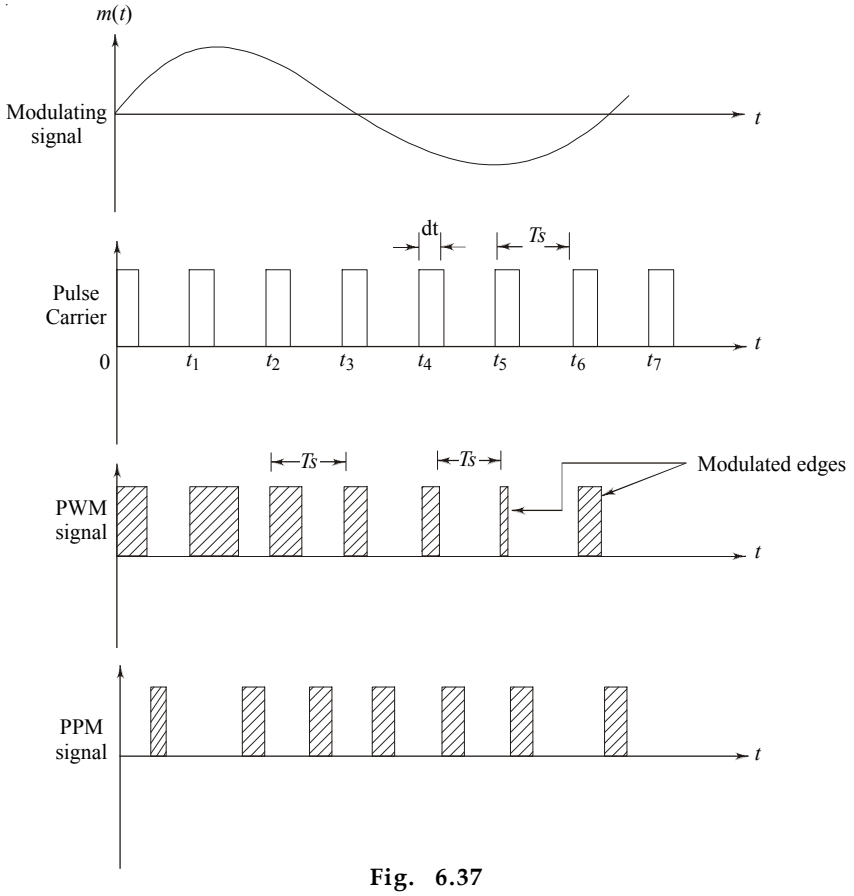


Fig. 6.37

Experiment : Pulse Amplitude Modulation (PAM)

Aim : ***To construct a pulse amplitude modulation and demodulation circuit and to observe the waveforms.***

Equipment Required

Equipment	Range	Quantity
CRO	(0 – 20) MHz	1
Function generator	(0 – 1) MHz	2
PAM kit		1

Components Required

Components	Value	Quantity
Transistor	BC107/2N2222	1
Capacitor	1.7 μF	1
Resistor	10 kΩ	2
	22 kΩ	1

Circuit diagram

Pulse Amplitude Modulation

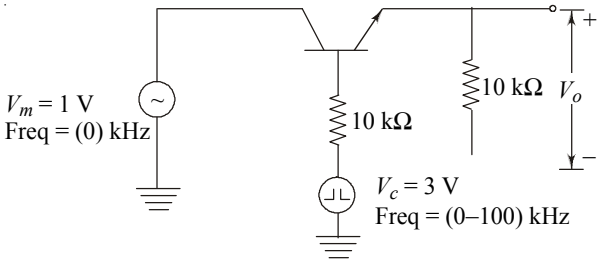


Fig. 6.38

Pulse Amplitude Demodulation

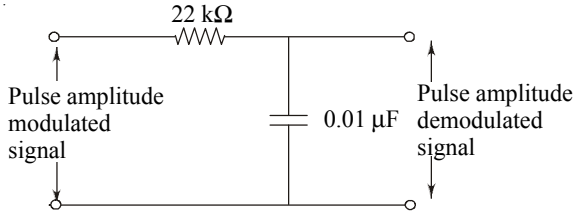


Fig. 6.39

Procedure

Pulse amplitude modulation

1. Connections are made as per the circuit diagram.
2. Modulating signal is given to collector and carrier signal (pulse signal) of high frequency is given to base of the transistor.
3. Output is taken at emitter and observe CRO.

Model Graph

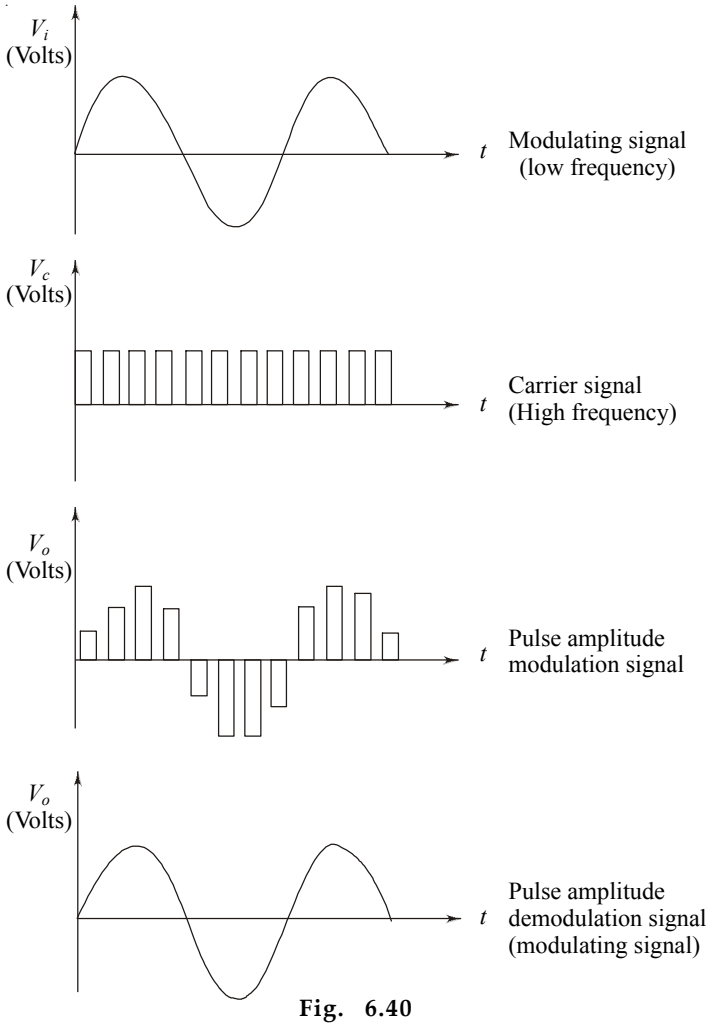


Fig. 6.40

Experiment : Pulse Width Modulation

Aim : ***To study and implement pulse width modulation using IC555.***

Equipment Required

Equipment	Range	Quantity
CRO	(0 – 20) MHz	1
Power supply	(0 – 5) V	

Components Required

Components	Value	Quantity
Timer IC	IC555	1
Capacitor	0.1 μF	1
Resistor	47 kΩ	1
	10 kΩ	1

Circuit diagram

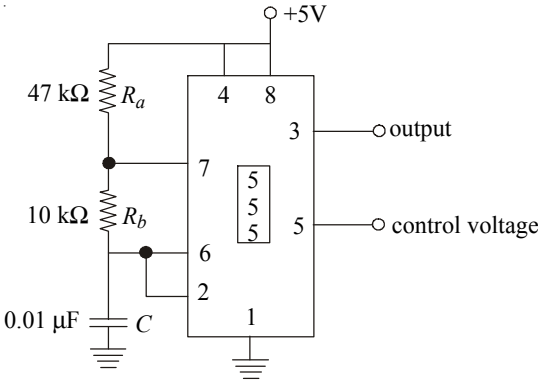


Fig. 6.41

Procedure

1. Connections are made as per circuit diagram.
2. Vary the control voltage (0 – 5) V and observe the corresponding change in output square waveform using CRO.
3. Change in control voltage changes the width of the square wave.
4. Note down the T_{ON} and T_{OFF}.
5. Plot the observed waveform.

Model Graph

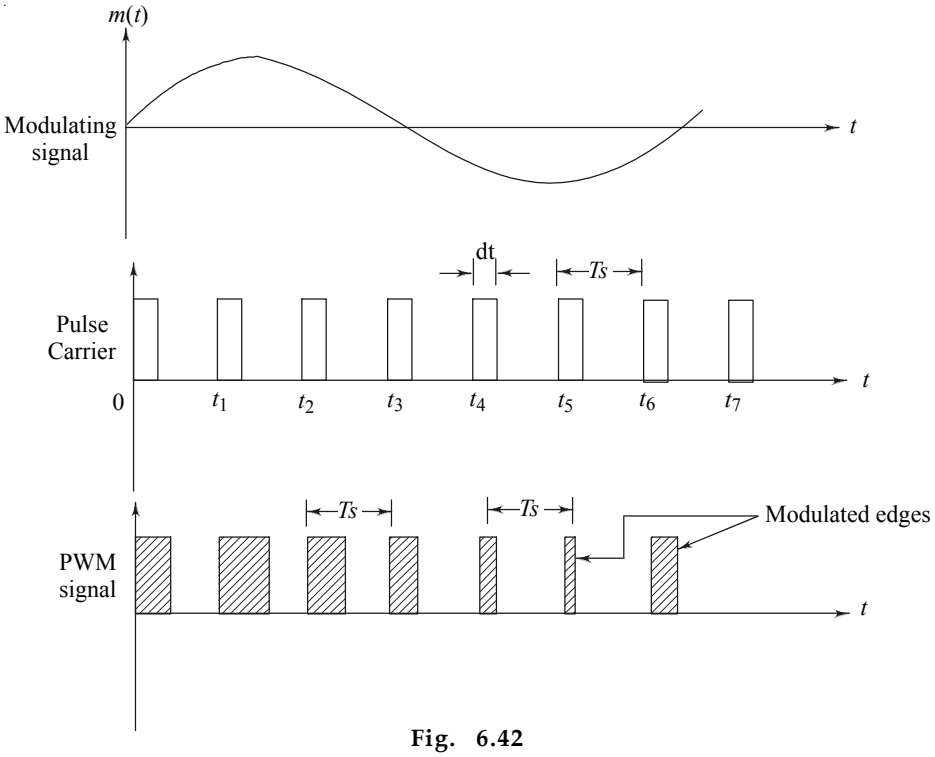


Fig. 6.42

Experiment : Pulse Width Modulation (PWM) and Pulse Position Modulation (PPM)

Aim : ***To construct and test a PWM and PPM circuit and to observe the waveforms.***

Equipment Required

Equipment	Range	Quantity
CRO	(0–20) MHz	1
Function generator	(0–1) MHz	2
Power supply	± 5V	1

Components Required

Components	Value	Quantity
PLL IC	565	1
EX-OR gate	7486	1
Resistor	390 kΩ	1
	33 kΩ	1
	10 kΩ	1
	4.7 kΩ	2
	5.6 kΩ	1
	5 kΩ (pot)	2
Capacitor	0.1 µF	3
	0.01 µF	2
	0.47 µF	1
	0.0047 µF	1

Circuit diagram

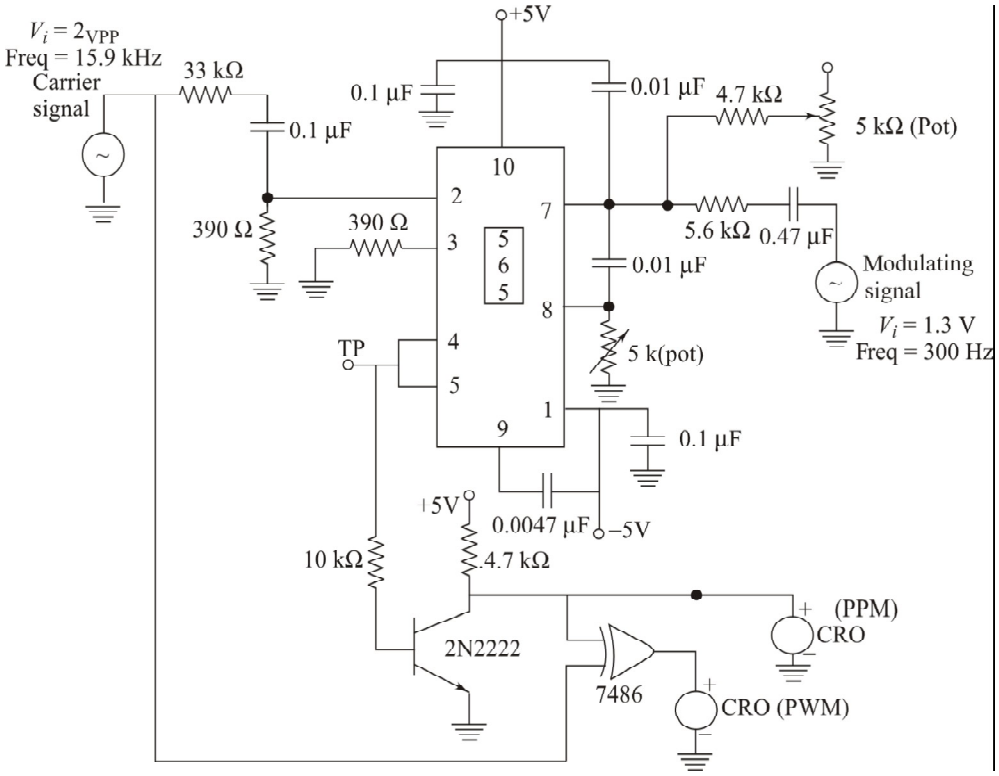


Fig. 6.43

Procedure

1. Connect the circuit as per the circuit diagram.
2. Check the free running frequency of the PLL (IC565) and adjust the potentiometer to produce 15 kHz at pin No. 4.
3. Set the carrier signal (say 2 V_{pp}, 15.9 kHz) which must be approximately in the middle of tracking range of PLL (IC565).
4. Apply modulating signal (say 1.3 V_{pp}, 300 Hz) at pin No 7.
5. Observe the PPM waveform in CRO as shown in the Fig. 6.44.
6. Observe the output of EX-OR gate (7486) using CRO adjust the frequency of the modulating signal to obtain a stable PWM output.

Model Graph

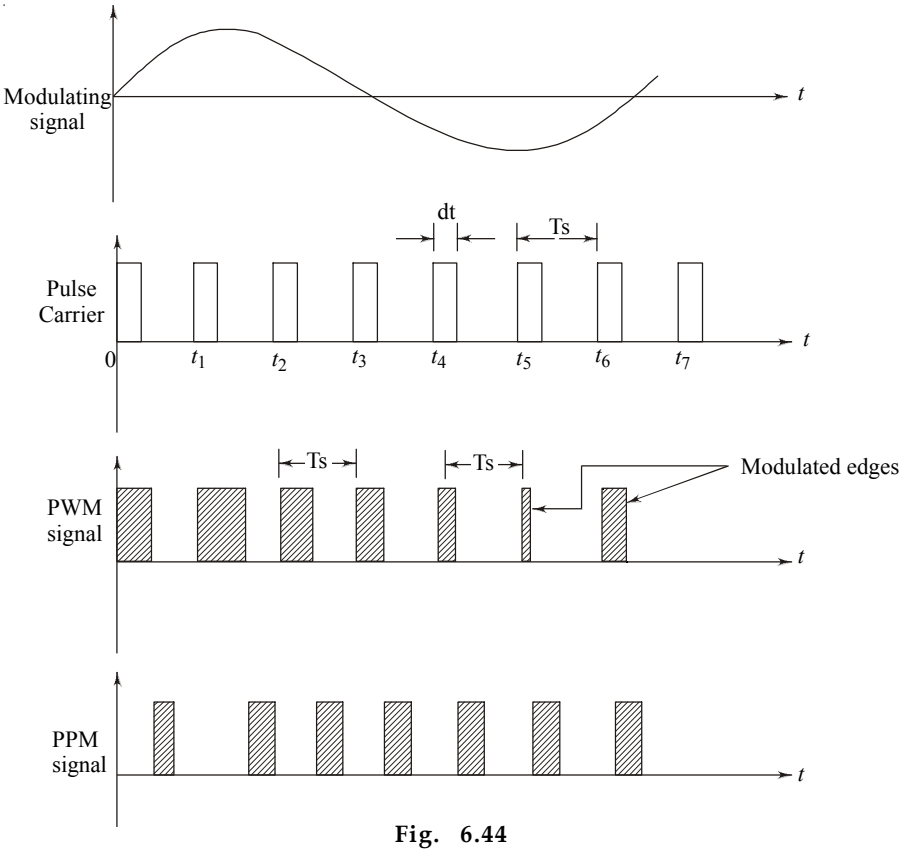


Fig. 6.44

Experiment : Amplitude Shift Keying (ASK) Modulator

Aim : ***To study and implement ASK modulator and to observe the waveform.***

Equipment Required

Equipment	Range	Quantity
CRO	(0–20) MHz	1
Function generator	(0–1) MHz	1
Power supply	(0–30) V	1
	± 12 V	1

Components Required

Components	Value	Quantity
Op-amp	µA 741	1
Transistor	BC 107	1
Resistor	1 kΩ	5
	10 kΩ (pot)	1
Capacitor	0.01 µF	2

Circuit diagram

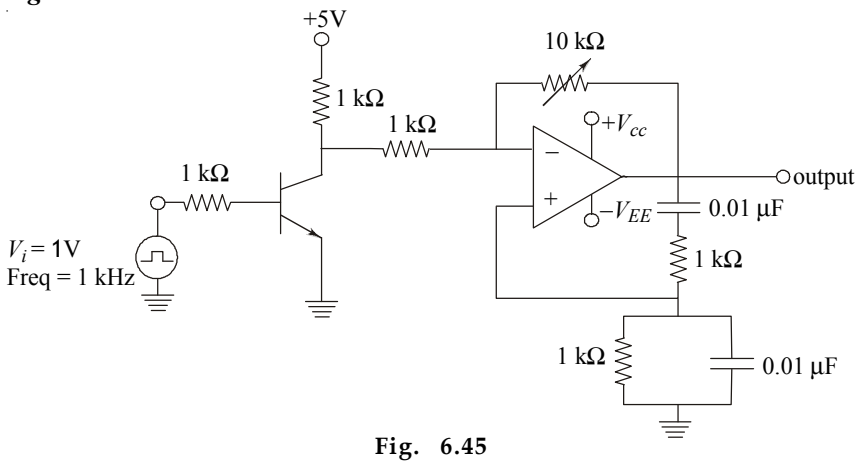


Fig. 6.45

Procedure

1. Connections are made as per the circuit diagram.
2. Set input signal (square wave) say 1 V, 1 kHz using function generator.
3. Observe the output waveform on the CRO.
4. Plot the observed waveform on the graph.

Model Graph

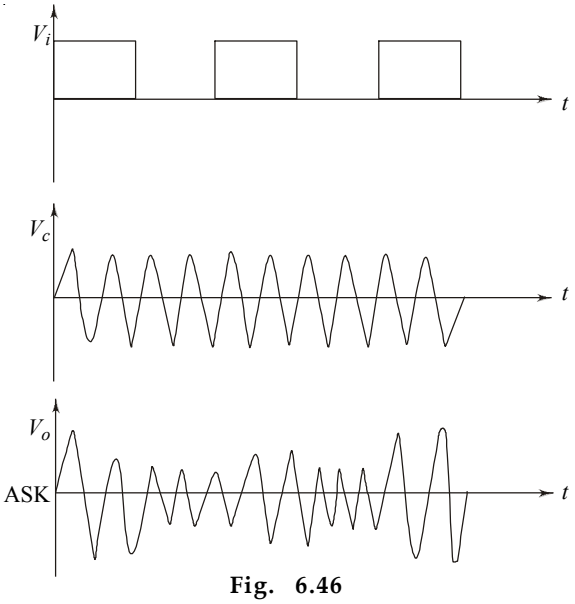


Fig. 6.46

Experiment : Amplitude Shift Keying Demodulator

Aim : ***To study and implement ASK demodulator and to observe waveform.***

Equipment Required

Equipment	Range	Quantity
CRO	(0–20) MHz	1
ASK modulator		1
Power supply	± 5 V	1
	(0–5) V	1

Components Required

Components	Value	Quantity
Op-amp	µA 741	1
Diode	IN 4001	1
Resistor	1 kΩ	1
Capacitor	1 µF	1

Circuit diagram

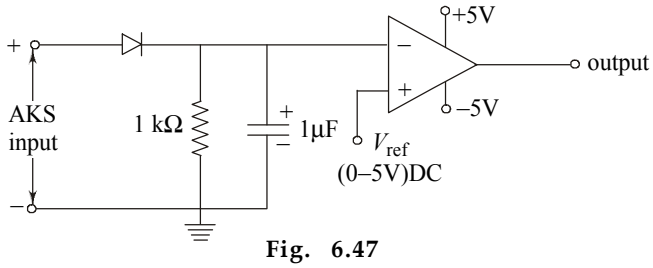


Fig. 6.47

Procedure

1. Connections are made as per the circuit diagram.
2. Give the FSK modulated signal as input the circuit.
3. Observe the output waveform on the CRO.
4. Vary the V_{ref}(0 – 5 V) and observe the corresponding waveform on the CRO.

Experiment : Pseudo Random Binary Sequence Generator

Aim : ***To study the functioning of a PRBS generator and to calculate the balance, run and correlation properties.***

Equipment Required

Equipment	Range	Quantity
Clock generator	(0–1) MHz	1
Power supply	(0–5) V	1

Components Required

Components	Value	Quantity
DF/F	7473	2
LED Resistor	330 Ω	1
EX-OR gate	7486	1
NOR gate	7404	1

Circuit Diagram

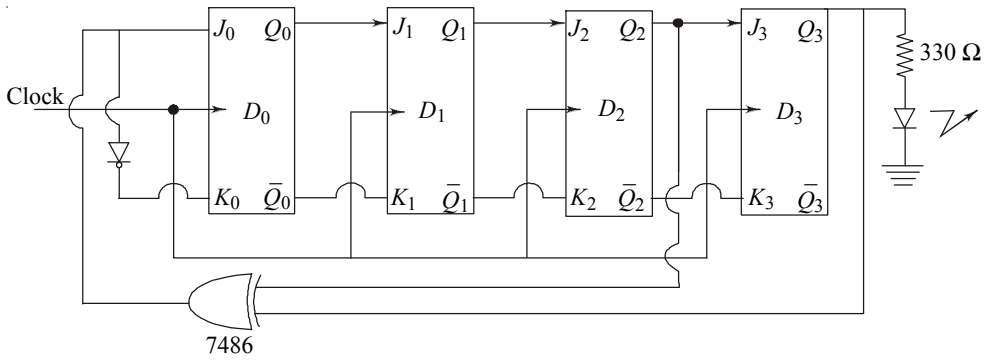


Fig. 6.48

1. Balance
2. Run property
3. Correlation property

Procedure

1. Connect the circuit as per the circuit diagram.
2. Observe the output sequence.

Experiment : Frequency Shift Keying (FSK) Modulator

Aim : ***To implement and study FSK modulator circuit.***

Equipment Required

Equipment	Range	Quantity
CRO	(0–20) MHz	1
Function generator	(0–1) MHz	1
Power supply	(0–30) V	1

Components Required

Components	Value	Quantity
	XR2206	1
Timer IC	555	1
PLL IC	565	1
Transistor	BC 107	1
Resistor	1 kΩ	2
	10 kΩ	3
	4.7 kΩ	2
	100 kΩ	1
Capacitor	1 nF	1
	22 μF	1
	0.01 μF	2

Circuit Diagram

Using PLL

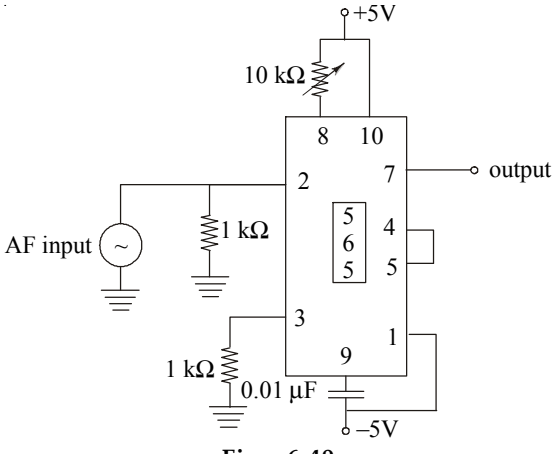


Fig. 6.49

Using Timer 555

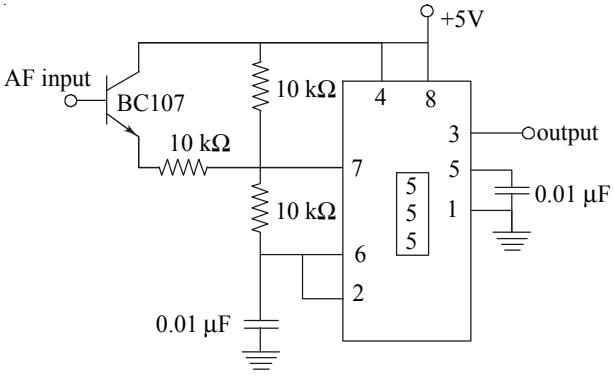


Fig. 6.50

Procedure

1. Connections are made as per the circuit diagram.
2. Set the AF input (say 1 V_{pp}, 150 Hz) using function generator.
3. Observe the output on CRO.
4. Draw the observed waveform on the graph.
5. Identify the mark frequency and space frequency.
6. Find the mark frequency (f_m) and space frequency (f_s).
7. Calculate modulation Index (MI) = $\frac{|f_m - f_s|}{f_0/2}$ where f_0 = fundamental frequency of the input signal.

Using XR2206

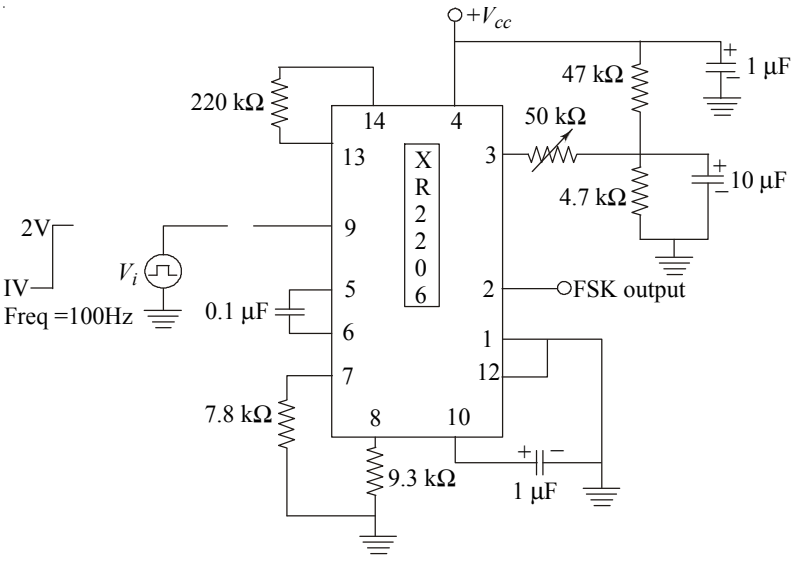


Fig. 6.51

Note: (XR2206): If voltage at pin No. 9 is less than 1 volt, only resistor R_2 is actuated. For voltage greater than 2 V resistor R_1 is actuated. Thus the output signal frequency can be keyed between two levels f_1 and f_2.

Model Graph

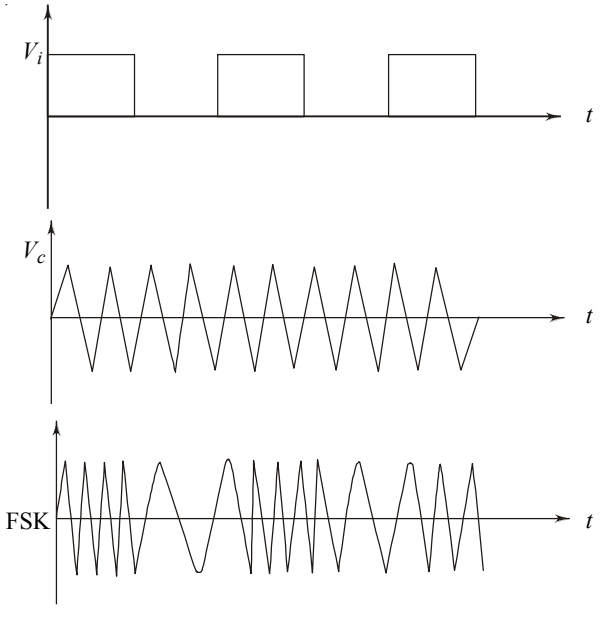


Fig. 6.52

Experiment : Frequency Shift Keying Demodulator

Aim : ***To design and implement FSK demodulator and observe the waveform.***

Equipment Required

Equipment	Range	Quantity
CRO	(0–20) MHz	1
FSK modulator		1
Power supply	(0 ± 30) V	2

Components Required

Components	Value	Quantity
PLL IC	565	1
OP-amp	µA 741	1
Resistor	10 kΩ	3
	1 kΩ	2
	33 kΩ	1
	10 k (pot)	1
Capacitor	0.02 µF	3
	0.01 µF	2

Circuit diagram

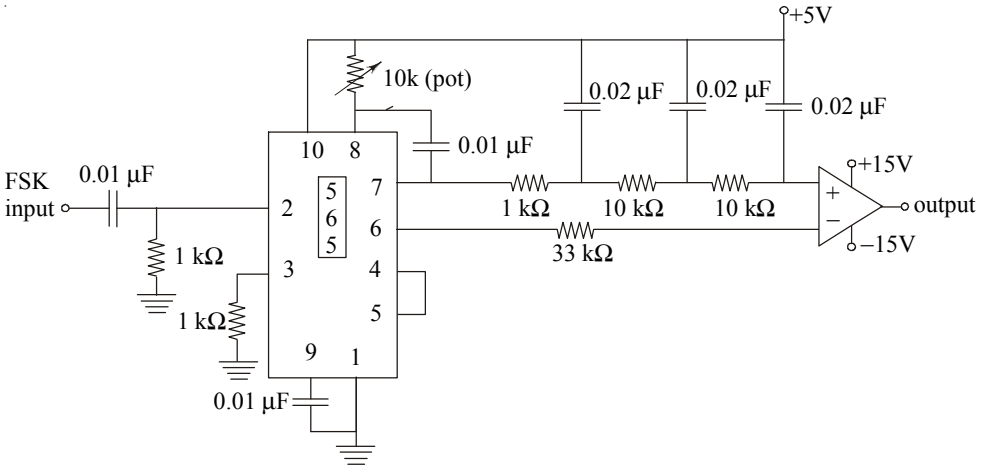


Fig. 6.53

Procedure

1. Connections are made as per the circuit diagram.
2. The FSK waveform (input signal) is given to pin No. 2.
3. The FSK demodulated output is observed on the CRO.

Experiment : Pre Emphasis

Aim : ***To construct and verify pre-emphasis network and plot the waveform.***

Equipment Required

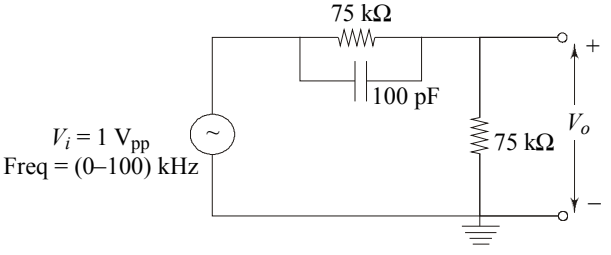
Equipment	Range	Quantity
CRO	(0–20) MHz	1
Function generator	(0–1) MHz	1
Power supply	(0–30) V	1

Components Required

Components	Value	Quantity
Transistor	BC 107/2N2222	1
	10 μF	
Capacitors	0.1 μF	1
	100 pF	1
	0.75 kH	1
Inductor	100 kΩ	1
Resistors	32 kΩ	1
	2.5 kΩ	1
	10 kΩ	1
	75 kΩ	1
		2

Circuit diagram

Pre-emphasis (passive)



Pre-emphasis (active)

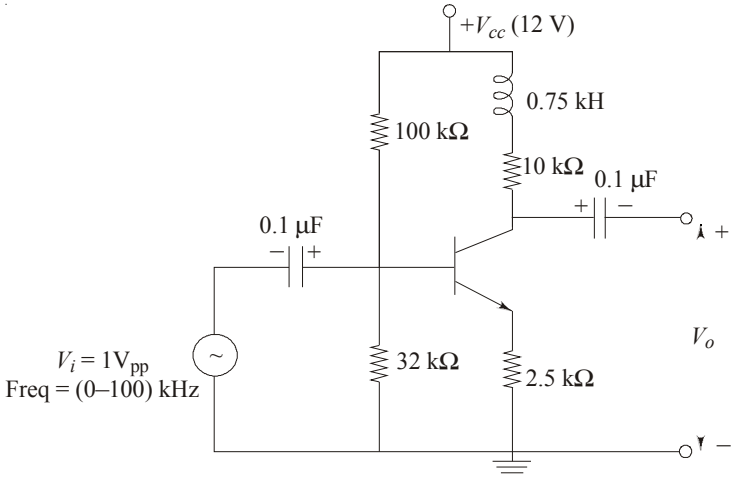


Fig. 6.54

Procedure

1. Connections are made as per circuit diagram.
2. Set input signal amplitude (say 1 V_{pp}) using function generator.
3. Vary the input signal frequency from 0 Hz to 100 kHz in regular steps.
4. Note down the corresponding output voltage.
5. Plot the graph: Gain (dB) vs Frequency (Hz).

Tabular Column

$V_i = 1\ V_{pp}$

Frequency (Hz)	Output voltage (V_o, Volts)	Gain (dB) = 20log (V_o/V_i)

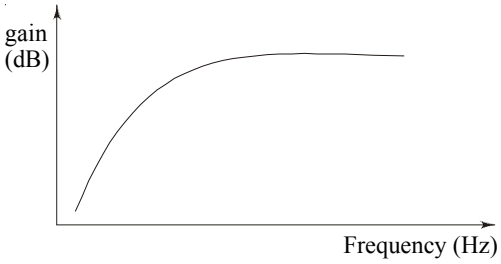


Fig. 6.55

Experiment : De-Emphasis

Aim : ***To construct and verify de-emphasis network and to plot waveform.***

Equipment Required

Equipment	Range	Quantity
CRO	(0–20) MHz	1
Function generator	(0–100) kHz	1

Components Required

Components	Value	Quantity
Capacitor	1000 pF	1
Resistors	75 kΩ	2

Circuit diagram

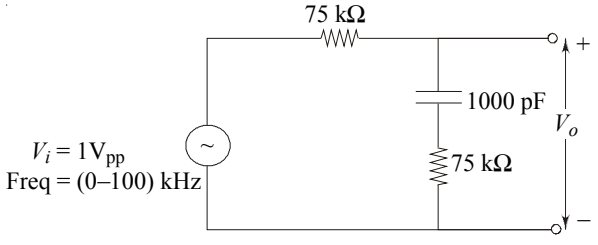


Fig. 6.56

Procedure

1. Connections are made as per circuit diagram.
2. Set input signal amplitude say 1 V_{pp}.
3. Vary the signal frequency from 0 Hz to 100 kHz in regular steps.
4. Note down the corresponding output voltage.
5. Plot the graph: Gain (dB) vs Frequency (Hz).

Tabular Column

$V_i = 1\ V_{pp}$

Frequency (Hz)	Output voltage (V_o, Volts)	Gain (dB) = 20log (V_o/V_i)

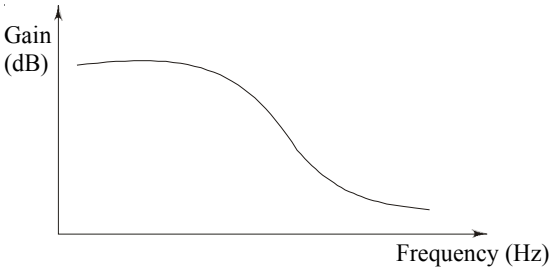


Fig. 6.57

Experiment : Digital Phase Detector

Aim : ***To construct a digital phase measurement detector and to detect phase difference between two sinusoidal waves and plot the waveforms and calculate phase angle.***

Equipment Required

Equipment	Range	Quantity
CRO	(0–20) MHz	1
Function generator	(0–1) MHz	1
Power supply	± 12 V	1
Ammeter (dc)	(0–10 mA)	1

Components Required

Components	Value	Quantity
Op-amp	µA 741	1
Ex-OR gate	IC 7486	1
Transistor	BC 107	1
Resistor	1 kΩ	1
Potentiometer	100 kΩ	1
Capacitor	0.01 µF	1

Circuit diagram

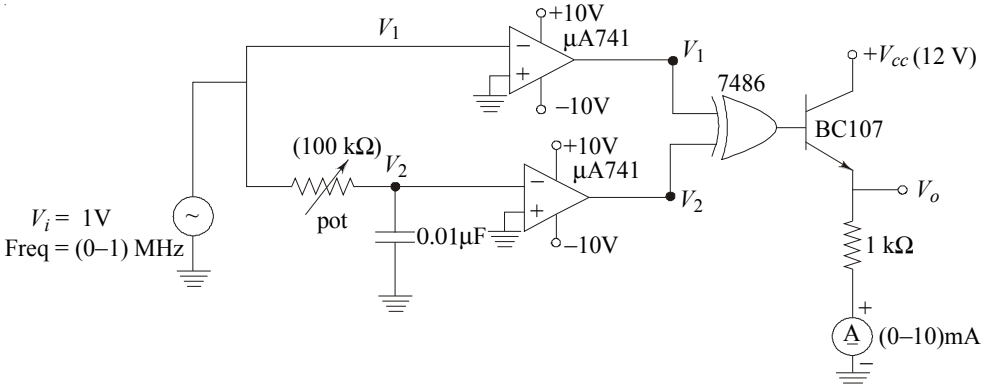


Fig. 6.58

Procedure

1. Connections are made as per the circuit diagram.
2. Set input signal (say 1 V_{pp}, 1 kHz) using function generator.
3. Observe the square waves at the output (pin No. 6) of both OP-amps.
4. Vary the resistance and note down the corresponding current using DC ammeter.
5. Also observe the output waveform across the emitter resistance of the transistor.
6. Phase angle can be calculated using the formula,

$$\phi = \tan^{-1} [\omega \text{ RC}].$$

7. Plot the graph: Phase angle (ϕ) vs Current (mA).

Tabular Columns

Resistance (kΩ)	Current (mA)	Phase angle $\phi = \tan^{-1}(\omega RC)$

Model Graph

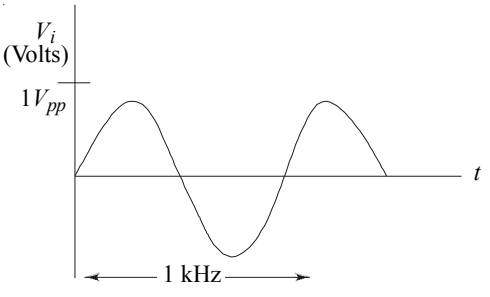


Fig. 6.59

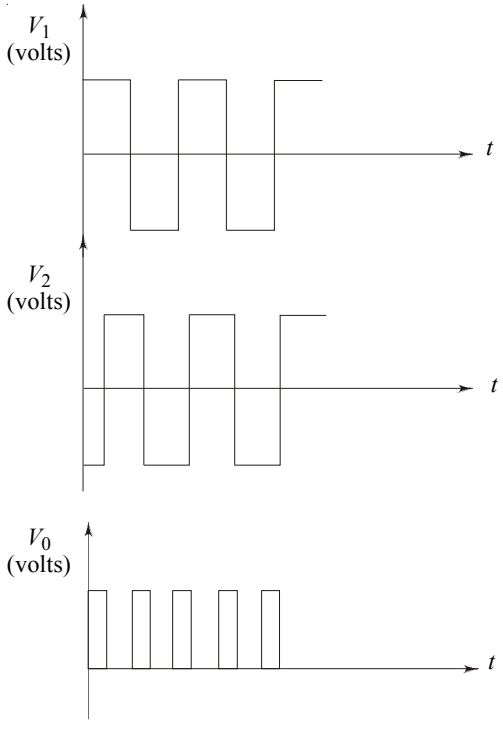


Fig. 6.60

Experiment : Mixer (Using Discrete Component)

Aim : ***To implement and study the mixer circuit.***

Equipment Required

Equipment	Range	Quantity
CRO	(0–20) MHz	1
Function generator	(0–1) MHz	2
Power supply	(0–30) V	1

Components Required

Components	Value	Quantity
Transistor	BC 107	1
Resistor	10 kΩ	4
	470 Ω	1
	1 kΩ	1
Capacitor	0.0 μF	2
	1 μF	1

Circuit diagram

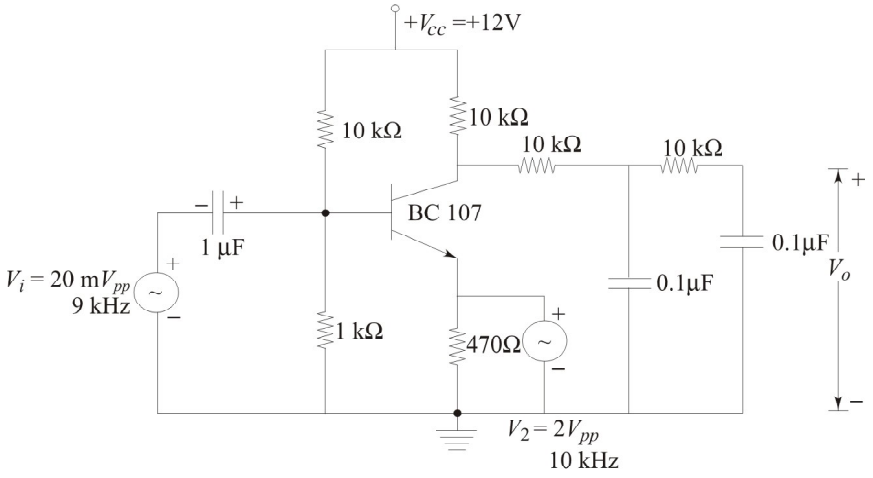


Fig. 6.61

Procedure

1. Connections are made as per the circuit diagram.
2. Apply both the input signals to the base and emitter terminal of the transistor.
3. Observe the output waveform on the CRO.

Experiment : Mixer (Using IC)

Aim : ***To construct and test a mixer circuit and study its working characteristics.***

Equipment Required

Equipment	Range	Quantity
CRO	(0–20) MHz	1
Function generator	(0–1) MHz	1
Power supply	± 5V	1

Components Required

Components	Value	Quantity
PLL	IC565	1
Resistor	33 kΩ	1
	10 kΩ	1
	1 kΩ	1
Capacitor	0.01 µF	2
	10 µF	1
	0.1 µF	1

Circuit diagram

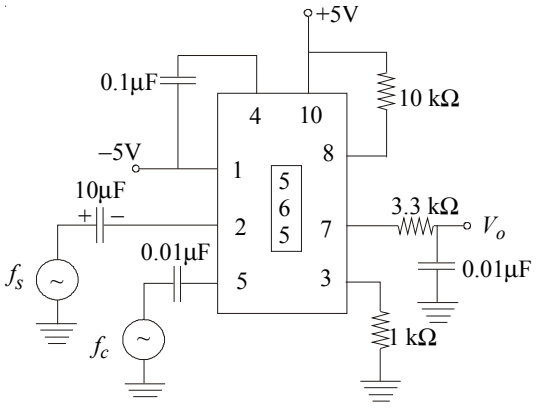


Fig. 6.62

Procedure

1. Connect the circuit as per the circuit diagram.
2. Set f_c = 100 kHz; f_s = 95 kHz and observe the output on the CRO. Note down the output frequency.

Tabular Column

f_s (kHz)	f_c (kHz)	Output Frequency (kHz)

Experiment : Auto Ranging

Aim : ***To design a circuit to perform the auto ranging operation.***

Equipment Required

Equipment	Range	Quantity
Voltmeter	(0–2) V	1
Power supply	± 15 V	1
	(0–2) V	1

Components Required

Components	Value	Quantity
OP-amp	μA 741	3
LED		3
Resistors	330 Ω	3
	10 kΩ (pot)	1

Circuit diagram

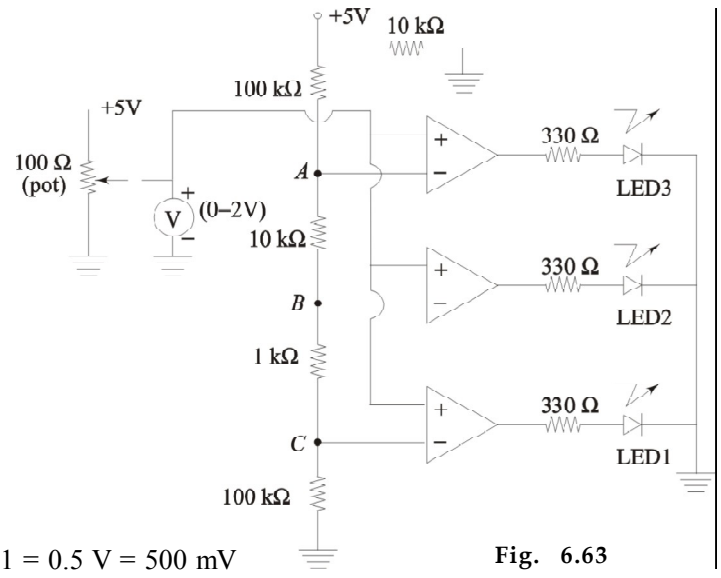


Fig. 6.63

Design

At Point A, $V_A = \dfrac{5}{111.1} \times 11.1 = 0.5 \text{ V} = 500 \text{ mV}$

Point B, $V_B = \dfrac{5}{111.1} \times 1.1 = 0.05 \text{ V} = 50 \text{ mV}$

Point C, $V_C = \dfrac{5}{111.1} \times 0.1 = 0.005 \text{ V} = 5 \text{ mV}$

Procedure

1. Connections are made as per the circuit diagram.
2. A + 5V supply is given to the voltage divider network which is connected to the inverting terminal of the OP-amps.
3. A (0–2V) variable supply is given to the non-inverting terminal of the OP-amp through a potentiometer (0–10 kΩ).
4. Vary the resistance of the potentiometer and observe the LED glow.
5. Note down the range which each LED's glows and tabulate the result.

Tabular Column

Voltage Range (mV)	LED1	LED2	LED3
	0	0	0
	1	0	0
	1	1	0
	1	1	1

Experiment : Frequency Counter

Aim : ***To design and implement a frequency counter using IC74121.***

Equipment Required

Equipment	Range	Quantity
Function generator	(0–1) MHz	1
Power supply	(0–30) V	1

Components Required

Components	Value	Quantity
IC	74121	1
AND gate	7408	2
Resistors	4.7 kΩ	1
	1.5 kΩ	1
Capacitor	1 μF	1
OR gate	7432	1

Circuit diagram

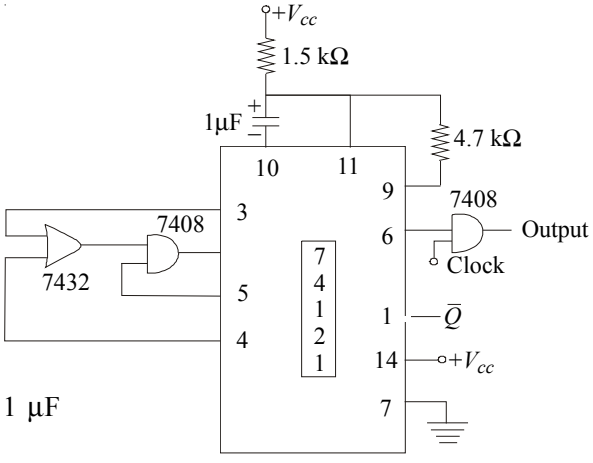


Fig. 6.64

Design

$T = 0.69\ RC$

$T = 1$ sec and $C = 1\ \mu F$

Therefore $R = 1.5\ k\Omega$

Procedure

1. Connections are made as per circuit diagram.
2. Counter display the frequency value of the signal.

Tabular Column

Frequency (Hz)	V_0 (Volt)

Experiment : Cross-Over Network

Aim : ***To design a cross-over network for a given frequency.***

Equipment Required

Equipment	Range	Quantity
CRO	(0–20) MHz	1
Function generator	(0–1) MHz	1

Components Required

Components	Value	Quantity
Inductors (DIB)	Variable	2
Capacitor (DCB)	Variable	2
Resistors	1 kΩ	2

Circuit diagram

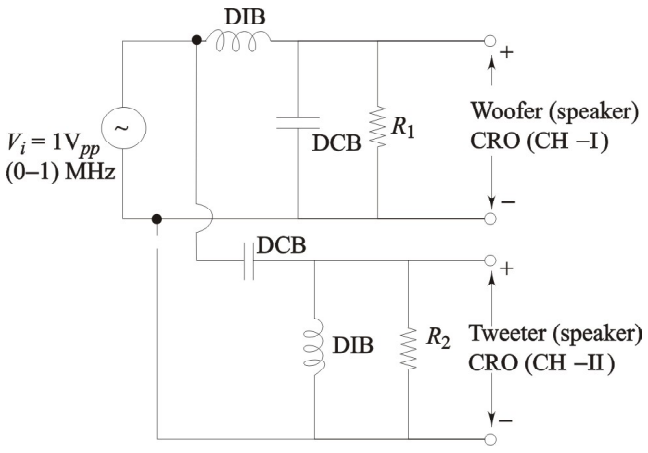


Fig. 6.65

Design

$$f_o = \frac{1}{2\pi\sqrt{LC}};\ \frac{L}{C} = 2R_0^2$$

Set $f_o = 1$ kHz; $R_o = 1\ \text{k}\Omega = R_1 = R_2$

Find L and C.

Procedure

1. Connections are made as per the circuit diagram.
2. Set the input signal say 1 V_{pp} using function generator.
3. Vary the frequency from 10 Hz in a regular step.
4. Note down the corresponding output voltages across both woofer and tweeter terminals or CH–I and CH–II of CRO.
5. Plot the graph: Gain (dB) vs. Frequency (Hz).

Tabular Column

$V_i = 1\ V_{pp}$

Frequency (Hz)	Output voltage (V_o)	Gain (dB) = 20log (V_o/V_i)

Model Graph

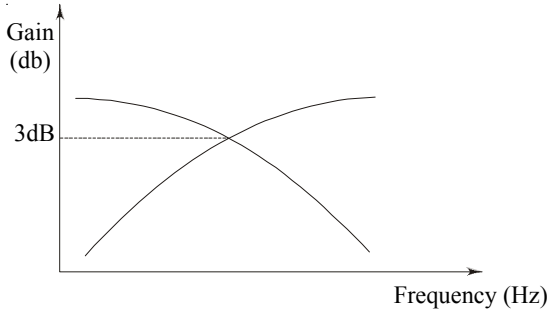
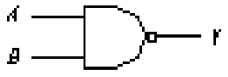


Fig. 6.66

APPENDIX

Quadruple 2-input positive – NAND gate (7400)

A1	1	14	V_{CC} (+ 5V)
B1	2	13	4B
Y1	3	12	4A
A2	4	11	Y4
B2	5	10	A3
Y2	6	9	A3
GND	7	8	Y3



Quadruple 2-input positive – NOR gate (7402)

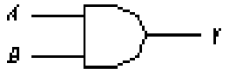
1Y	1	14	V_{CC} (+ 5V)
1A	2	13	4Y
1B	3	12	4B
2Y	4	11	4A
2A	5	10	3Y
2B	6	9	3B
GND	7	8	3A

HEX inverter (7404)

1A	1	14	V_{CC} (+ 5V)
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

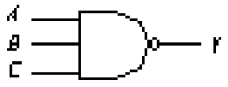
Quadruple 2-input positive – AND gate (7408)

1A	1	14	V_{CC} (+ 5V)
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y



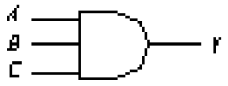
Triple 3-input positive—NAND gate (7410)

1A	1	14	V_{CC} (+ 5V)
1B	2	13	1C
2A	3	12	1Y
2B	4	11	3C
2C	5	10	3B
2Y	6	9	3A
GND	7	8	3Y



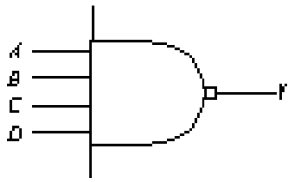
Triple 3-input positive—AND gate (7411)

1A	1	14	V_{CC} (+ 5V)
1B	2	13	1C
2A	3	12	1Y
2B	4	11	3C
2C	5	10	3B
2Y	6	9	3A
GND	7	8	3Y



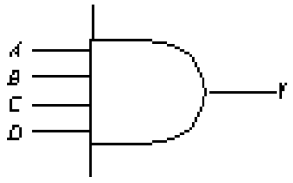
Dual 4-input positive—NAND gates (7420)

1A	1	14	V_{CC} (+5)
1B	2	13	2D
NC	3	12	2C
1C	4	11	NC
1D	5	10	2B
1Y	6	9	2A
GND	7	8	2Y



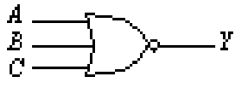
Dual 4-input positive—AND gate (7421)

1A	1	14	V_{CC} (+ 5V)
1B	2	13	2D
NC	3	12	2C
1C	4	11	NC
1D	5	10	2B
1Y	6	9	2A
GND	7	8	2Y



Triple 3-input positive—NOR gate (7427)

1A	1	14	V_{CC} (+ 5V)
1B	2	13	1C
2A	3	12	1Y
2B	4	11	3C
2C	5	10	3B
2Y	6	9	3A
GND	7	8	3Y



Quadruple 2-input positive–OR gate (7432)

1A	1	14	V_{CC} (+ 5V)
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

Dual D-Type positive edge triggered flip-flops with preset and clear (7474)

$1\overline{CLR}$	1	14	V_{CC} (+ 5V)
1D	2	13	$2\overline{CLR}$
1 CLK	3	12	2D
$1\overline{PRE}$	4	11	2CLK
1Q	5	10	$2\overline{PRE}$
$1\overline{Q}$	6	9	2Q
GND	7	8	$2\overline{Q}$

Input				Output	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Dual J-K Flip-flop with preset and clear (7476)

1CLK	1	16	1K
$1\overline{PRE}$	2	15	1Q
$1\overline{CLR}$	3	14	$1\overline{Q}$
1 J	4	13	GND
V_{CC}	5	12	2K
2CLK	6	11	2Q
$2\overline{PRE}$	7	10	$2\overline{Q}$
$2\overline{CLR}$	8	9	2J

Input					Output	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q_0	$\overline{Q}_0$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	Toggle	

* This configuration is nonstable

Quadruple 2-input EXCLUSIVE–OR gate (7486)

1A	1	14	V_{CC} (+ 5V)
1B	2	13	4B
1Y	3	12	4A
2A	4	11	4Y
2B	5	10	3B
2Y	6	9	3A
GND	7	8	3Y

4 line to 4-line Decoders (7442)

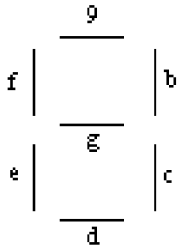
0	1	16	V_{CC} (+ 5V)
1	2	15	A
2	3	14	B
3	4	13	C
4	5	12	D
5	6	11	9
6	7	10	8
GND	8	9	7

BCD to Decimal Decoder (7445)

0	1	16	V_{CC} (+ 5V)
1	2	15	A
2	3	14	B
3	4	13	C
4	5	12	D
5	6	11	9
6	7	10	8
GND	8	9	7

BCD to Seven Segment Decoder/Driver (7449)

B	1	14	V_{CC} (+ 5V)
C	2	13	f
$+\overline{BI}$	3	12	g
D	4	11	9
A	5	10	b
E	6	9	c
GND	7	8	d



*$\overline{BI}$: Blanking input which can be used to control the lamp intensity by pulse or to inhibit the output.

Dual J-K Flip-flops with clear (7473)

1 CLK	1	14	1 J
$1\overline{CLR}$	2	13	$1\overline{Q}$
1K	3	12	1Q
VCC	4	11	GND
2 CLK	5	10	2K
$2\overline{CLR}$	6	9	2Q
2J	7	8	$2\overline{Q}$

Input				Output	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q_0	$\overline{Q}_0$
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	Toggle	

DATA Selector/Multiplexer (74150/74151/74152)

74150

E7	1	24	V_{CC}
E6	2	23	E8
E5	3	22	E9
E4	4	21	E10
E3	5	20	E11
E2	6	19	E12
E1	7	18	E13
E0	8	17	E14
$\overline{G}$	9	16	E15
W	10	15	A
D	11	14	B
GND	12	13	C

74151

D3	1	16	V_{CC}
D2	2	15	D4
D1	3	14	D5
D0	4	13	D6
Y	5	12	D7
W	6	11	A
$\overline{G}$	7	10	B
GND	8	9	C

74152

D4	1	14	V_{CC}
D3	2	13	D5
D2	3	12	D6
D1	4	11	D7
D0	5	10	A
W	6	9	B
GND	7	8	C

Function table (74150)

Input			Output
	Select	Stroke	W
D	CBA	$\overline{G}$	
X	XXX	H	H
L	LLL	L	$\overline{E}$
L	LLH	L	$\overline{E}_1$
L	LHL	L	$\overline{E}_2$
L	LHH	L	$\overline{E}_3$
L	HLL	L	$\overline{E}_4$
L	HLH	L	$\overline{E}_5$
L	HHL	L	$\overline{E}_6$
L	HHH	L	$\overline{E}_7$
H	LLL	L	$\overline{E}_8$
H	LLH	L	$\overline{E}_9$
H	LHL	L	$\overline{E}_{10}$
H	LHH	L	$\overline{E}_{11}$
H	HLL	L	$\overline{E}_{12}$
H	HLH	L	$\overline{E}_{13}$
H	HHL	L	$\overline{E}_{14}$
H	HHH	L	$\overline{E}_{15}$

(74151)

Input		Output	
Select	Stroke	Y	W
CBA	$\overline{G}$	•	•
XXX	H	L	H
LLL	L	D_0	$\overline{D}_0$
LLH	L	D_1	$\overline{D}_1$
LHL	L	D_2	$\overline{D}_2$
LHH	L	D_3	$\overline{D}_3$
HLL	L	D_4	$\overline{D}_4$
HLH	L	D_5	$\overline{D}_5$
HHL	L	D_6	$\overline{D}_6$
HHH	L	D_7	$\overline{D}_7$

(74152)

Input			Output
C	B	A	W
L	L	L	D_0
L	L	H	$\overline{D}_1$
L	H	L	$\overline{D}_2$
L	H	H	$\overline{D}_3$
H	L	L	$\overline{D}_4$
H	L	H	$\overline{D}_5$
H	H	L	$\overline{D}_6$
H	H	H	$\overline{D}_7$

μA 741

OFFSET NULL	1	8	NC
INVERTING	2	7	+ V_{CC}
NON-INV	3	6	OUT
$-V_{CE}$	4	5	+ OFFSET NULL

555 -TIMER

GROUN	1	8	+ V_{CC}
TRIGGER	2	7	DISCHARGE
OUTPUT	3	6	THRESHOLD
RESET	4	5	CONTROL VOLTAGE

NE/SE 565 PLL IC

– V	1	14	NC
INPUT	2	13	NC
INPUT	3	12	NC
VCO o/p	4	11	NC
Phase comparator VCO i/p	5	10	
Reference o/p	6	9	External capacitor for VCO
Demodulated o/p	7	8	External resistor for VCO

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